

3.3V 10-Bit Flip-Flop with Dual Outputs and 3-State Outputs

Product Features

- PI74ALVCH16820 is designed for low-voltage operation
- $V_{CC}=2.3V$ to $3.6V$
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) $<0.8V$ at $V_{CC}=3.3V$, $T_A=25^{\circ}C$
- Typical V_{OHV} (Output V_{OH} Undershoot) $<2.0V$ at $V_{CC}=3.3V$, $T_A=25^{\circ}C$
- Bus Hold retains last active bus state during 3-state eliminating the need for external pullup resistors
- Industrial operation: $-40^{\circ}C$ to $+85^{\circ}C$
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCH16820, a 10-bit flip-flop designed for 2.3V to 3.3V V_{CC} operation, features edge-triggered D-type flip-flops. On the positive transition of clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the ten outputs in either a normal logic state (HIGH or LOW level) or a high-impedance state. In high-impedance state, outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive are able to drive bus lines without interface or pullup components.

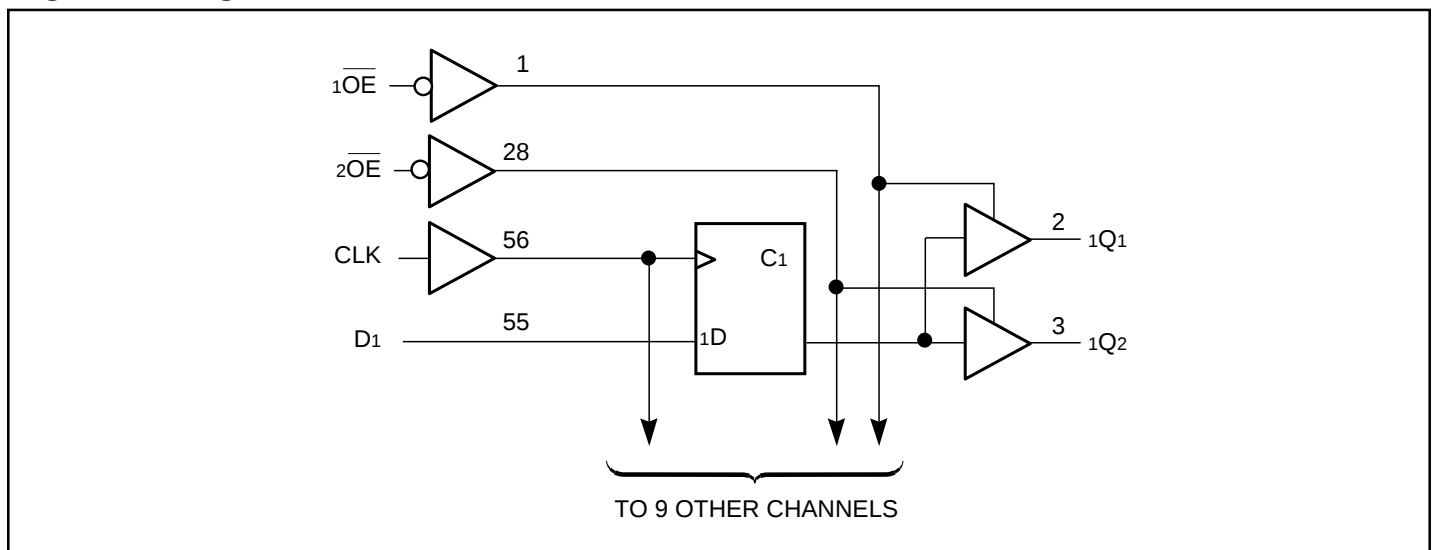
$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor whose minimum value is determined by the current sinking capability of the driver.

To prevent "floating" inputs and to eliminate the need for pullup/down resistors, the PI74ALVCH16820 has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
V _{CC}	Power

Truth Table⁽¹⁾

Inputs			Outputs
$\overline{OE}_n$	CLK	D	Q _n
L	—	H	H
L	—	L	L
L	L	X	Q ₀
H	X	X	Z

Note:

1. H = High Signal Level
L = Low Signal Level
X = Irrelevant
Z = High Impedance
↑ = LOW-to-HIGH Transition
n = 1,2

Maximum Ratings

(Above which the useful life may be impaired.
For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied ...	–40°C to +85°C
Input Voltage Range, V _{IN}	–0.5V to V _{CC} +0.5V
Output Voltage Range, V _{OUT}	–0.5V to V _{CC} +0.5V
DC Input Voltage	–0.5V to +5.0V
DC Output Current	100mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Product Pin Configuration

$\overline{1OE}$	1	56	CLK
1Q1	2	55	D1
1Q2	3	54	NC
GND	4	53	GND
2Q1	5	52	D2
2Q2	6	51	NC
V _{CC}	7	50	V _{CC}
3Q1	8	49	D3
3Q2	9	48	NC
4Q1	10	47	D4
GND	11	46	GND
4Q2	12	45	NC
5Q1	13	44	D5
5Q2	14	43	NC
6Q1	15	42	D6
6Q2	16	41	NC
7Q1	17	40	D7
GND	18	39	GND
7Q2	19	38	NC
8Q1	20	37	D8
8Q2	21	36	NC
V _{CC}	22	35	V _{CC}
9Q1	23	34	D9
9Q2	24	33	NC
GND	25	32	GND
10Q1	26	31	D10
10Q2	27	30	NC
$\overline{2OE}$	28	29	NC

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
$V_{IH}^{(3)}$	Input HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 2.7V	1.7			
		$V_{CC} = 2.7\text{V}$ to 3.6V	2.0			
$V_{IL}^{(3)}$	Input LOW Voltage	$V_{CC} = 2.3\text{V}$ to 2.7V			0.7	
		$V_{CC} = 2.7\text{V}$ to 3.6V			0.8	
$V_{IN}^{(3)}$	Input Voltage		0		V_{CC}	
$V_{OUT}^{(3)}$	Output Voltage		0		V_{CC}	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu\text{A}$, $V_{CC} = \text{Min. to Max.}$	$V_{CC} - 0.2$			
		$V_{IH} = 1.7\text{V}$, $I_{OH} = -6\text{mA}$, $V_{CC} = 2.3\text{V}$	2.0			
		$V_{IH} = 1.7\text{V}$, $I_{OH} = -12\text{mA}$, $V_{CC} = 2.3\text{V}$	1.7			
		$V_{IH} = 2.0\text{V}$, $I_{OH} = -12\text{mA}$, $V_{CC} = 2.7\text{V}$	2.2			
		$V_{IH} = 2.0\text{V}$, $I_{OH} = -12\text{mA}$, $V_{CC} = 3.0\text{V}$	2.4			
		$V_{IH} = 2.0\text{V}$, $I_{OH} = -24\text{mA}$, $V_{CC} = 3.0\text{V}$	2.0			
V_{OL}	Output LOW Voltage	$I_{OL} = 100\mu\text{A}$, $V_{IL} = \text{Min. to Max.}$			0.2	mA
		$V_{IL} = 0.7\text{V}$, $I_{OL} = 6\text{mA}$, $V_{CC} = 2.3\text{V}$			0.4	
		$V_{IL} = 0.7\text{V}$, $I_{OL} = 12\text{mA}$, $V_{CC} = 2.3\text{V}$			0.7	
		$V_{IL} = 0.8\text{V}$, $I_{OL} = 12\text{mA}$, $V_{CC} = 2.7\text{V}$			0.4	
		$V_{IL} = 0.8\text{V}$, $I_{OL} = 24\text{mA}$, $V_{CC} = 3.0\text{V}$			0.55	
$I_{OH}^{(3)}$	Output HIGH Current	$V_{CC} = 2.3\text{V}$			-12	mA
		$V_{CC} = 2.7\text{V}$			-12	
		$V_{CC} = 3.0\text{V}$			-24	
$I_{OL}^{(3)}$	Output LOW Current	$V_{CC} = 2.3\text{V}$			12	mA
		$V_{CC} = 2.7\text{V}$			24	
		$V_{CC} = 3.0\text{V}$			24	
I_{IN}	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6\text{V}$			± 5	μA
$I_{IN}(\text{HOLD})$	Input Hold Current	$V_{IN} = 0.7\text{V}$, $V_{CC} = 2.3\text{V}$	45			
		$V_{IN} = 1.7\text{V}$, $V_{CC} = 2.3\text{V}$	-45			
		$V_{IN} = 0.8\text{V}$, $V_{CC} = 3.0\text{V}$	75			
		$V_{IN} = 2.0\text{V}$, $V_{CC} = 3.0\text{V}$	-75			
		$V_{IN} = 0$ to 3.6V , $V_{CC} = 3.6\text{V}$			± 500	
I_{OZ}	Output Current (3-State Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6\text{V}$			± 10	pF
I_{CC}	Supply Current	$V_{CC} = 3.6\text{V}$, $I_{OUT} = 0\mu\text{A}$, $V_{IN} = \text{GND}$ or V_{CC}			40	
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.0\text{V}$ to 3.6V One Input at $V_{CC} - 0.6\text{V}$ Other Inputs at V_{CC} or GND			750	
C_I	Control Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3\text{V}$		3.5		
	Data Inputs			6		pF
C_O	Outputs	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3\text{V}$		7		

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient and maximum loading.
- Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

Timing Requirements over Operating Range

Parameters	Description	PI74ALVCH16820						Units
		V _{CC} = 2.5 V ±0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ±0.3 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{CLOCK}	Clock Frequency	0	150	0	150	0	150	MHz
t _W	Pulse duration CLK high or low	3.3		3.3		3.3		ns
t _{SU}	Setup time data before CLK↑	1.7		1.8		1.4		
t _H	Hold time data after CLK↑	1.1		1.1		1.0		
Δ _t /Δ _v ⁽³⁾	Input Transition Rise or Fall					0	10	ns/V

Switching Characteristics over Operating Range⁽¹⁾

Parameters	From (Input)	To (Output)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		Units
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
f_{MAX}			150		150		150		MHz
t_{PD}	CLK	Q	1.0	6.5		5.5	1.0	4.8	ns
t_{EN}	$\overline{\text{OE}}$	Q	1.0	6.9		6.1	1.0	5.0	ns
t_{DIS}	$\overline{\text{OE}}$	Q	1.3	5.9		5.0	1.0	4.5	ns

Notes:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Recommended operating condition.

Operating Characteristics, $T_A = 25^\circ\text{C}$

Parameters		Test Conditions	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	Units
			Typical	Typical	
C_{PD} Power Dissipation Capacitance	Outputs Enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	60	63	pF
	Outputs Disabled		38	46	