NAND Flash Memory

MT29F1G08AACWP, MT29F1G08AACH4 MT29F1G08ABCHC, MT29F1G16ABCHC, MT29F1G08ABCH4, MT29F1G16ABCH4

Features

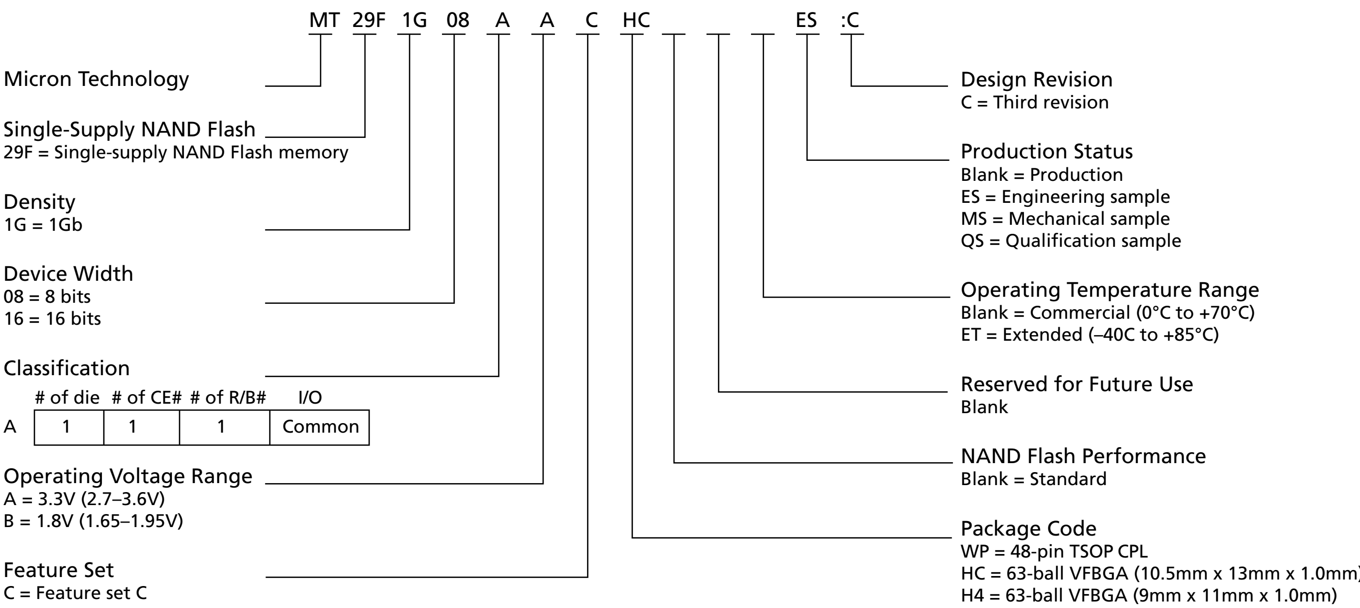
- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 2112 bytes (2048 + 64 bytes)
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 1Gb: 1024 blocks
- Asynchronous I/O performance
  - $^tRC/^tWC$: 25ns (3.3V), 35ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 250µs (TYP, 3.3V)
  - Program page: 250µs (TYP, 1.8V)
  - Erase block: 500µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Block lock (1.8V only)
  - Boot block (1.8V only)
  - Programmable drive strength
  - Read unique ID
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Internal data move operations supported within the device from which data is read
- Ready/busy# (R/B#) signal provides a hardware method for detecting operation completion
- WP# signal: write protect entire device
- Blocks 0–7 (block address 00h-07h) guaranteed to be valid with ECC when shipped from factory (3.3V only); see Error Management (page 83).
- Blocks 0–3 (block address 00h-03h) guaranteed to be valid with ECC when shipped from factory (1.8V only); see Error Management (page 83).
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization (Nand_Init) after power up[3] (contact factory)
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles
- Operating Voltage Range
  - V_{CC}: 2.7–3.6V
  - V_{CC}: 1.65–1.95V
- Operating temperature:
  - Commercial: 0°C to +70°C
  - Extended (ET): –40ºC to +85ºC
- Package
  - 48-pin TSOP type 1, CPL[2]
  - 63-ball VFBGA

Notes:
1. The ONFI 1.0 specification is available at www.onfi.org.
2. CPL = Center parting line.
3. Available only in 1.8V VFBGA package.

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Marketing Part Number Chart



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General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization.

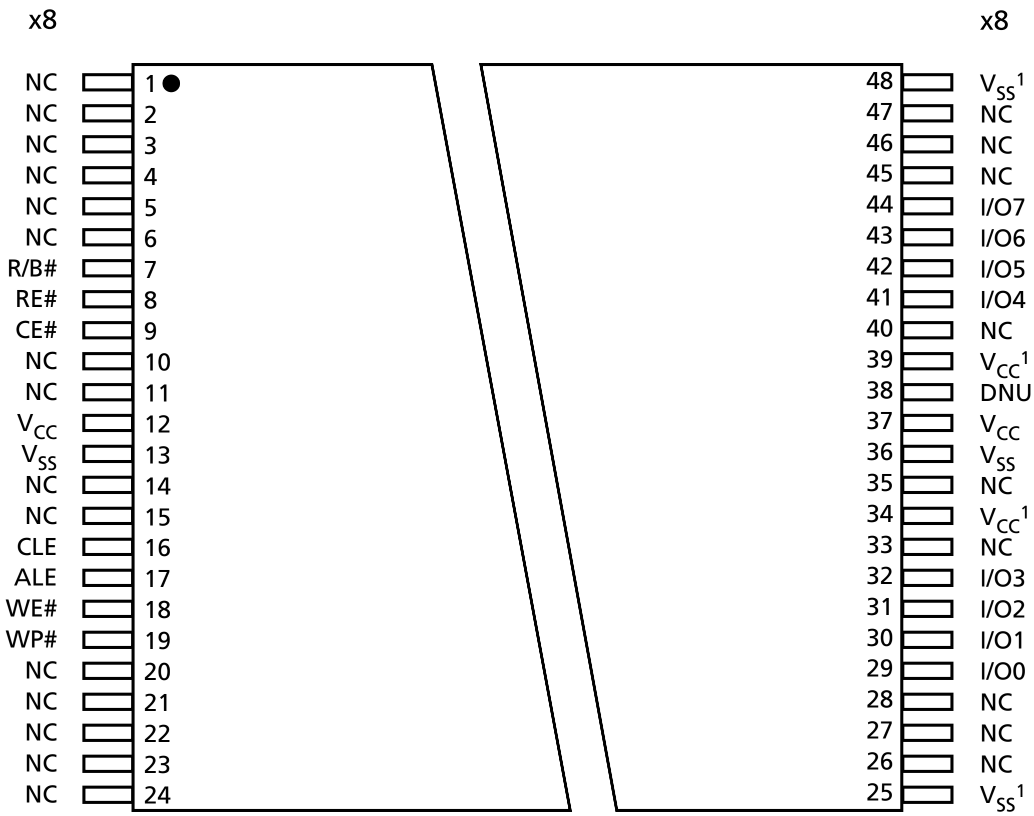
Signal Descriptions and Assignments

Table 1: Asynchronous Signal Definitions

Signal[1]	Type	Description[2]
ALE	Input	**Address latch enable:** Loads an address from I/O[7:0] into the address register.
CE#	Input	**Chip enable:** Enables or disables one or more die (LUNs) in a target.
CLE	Input	**Command latch enable:** Loads a command from I/O[7:0] into the command register.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable the BLOCK LOCK, connect LOCK to Vss during power-up, or leave it disconnected (internal pull-down).
RE#	Input	**Read enable:** Transfers serial data from the NAND Flash to the host system.
WE#	Input	**Write enable:** Transfers commands, addresses, and serial data from the host system to the NAND Flash.
WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
I/O[7:0] (x8) I/O[15:0] (x16)	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	Supply	**V_{CC}:** Core power supply
V_{SS}	Supply	**V_{SS}:** Core ground connection
NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	–	**Do not use:** DNUs must be left unconnected.

Notes:
1. See Device and Array Organization for detailed signal connections.
2. See Asynchronous Interface Bus Operations for detailed asynchronous interface signal descriptions.

Figure 2: 48-Pin TSOP – Type 1, CPL (Top View)



Note: 1. These pins might not be bonded in the package; however, Micron recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

Figure 3: 63-Ball VFBGA, x8 (Balls Down, Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	V_{SS}	CE#	WE#	R/B#		
D			V_{CC}[1]	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	V_{SS}[1]	NC		
G			DNU	V_{CC}[1]	LOCK	NC	NC	NC		
H			NC	I/O0	NC	NC	NC	V_{CC}		
J			NC	I/O1	NC	V_{CC}	I/O5	I/O7		
K			V_{SS}	I/O2	I/O3	I/O4	I/O6	V_{SS}		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

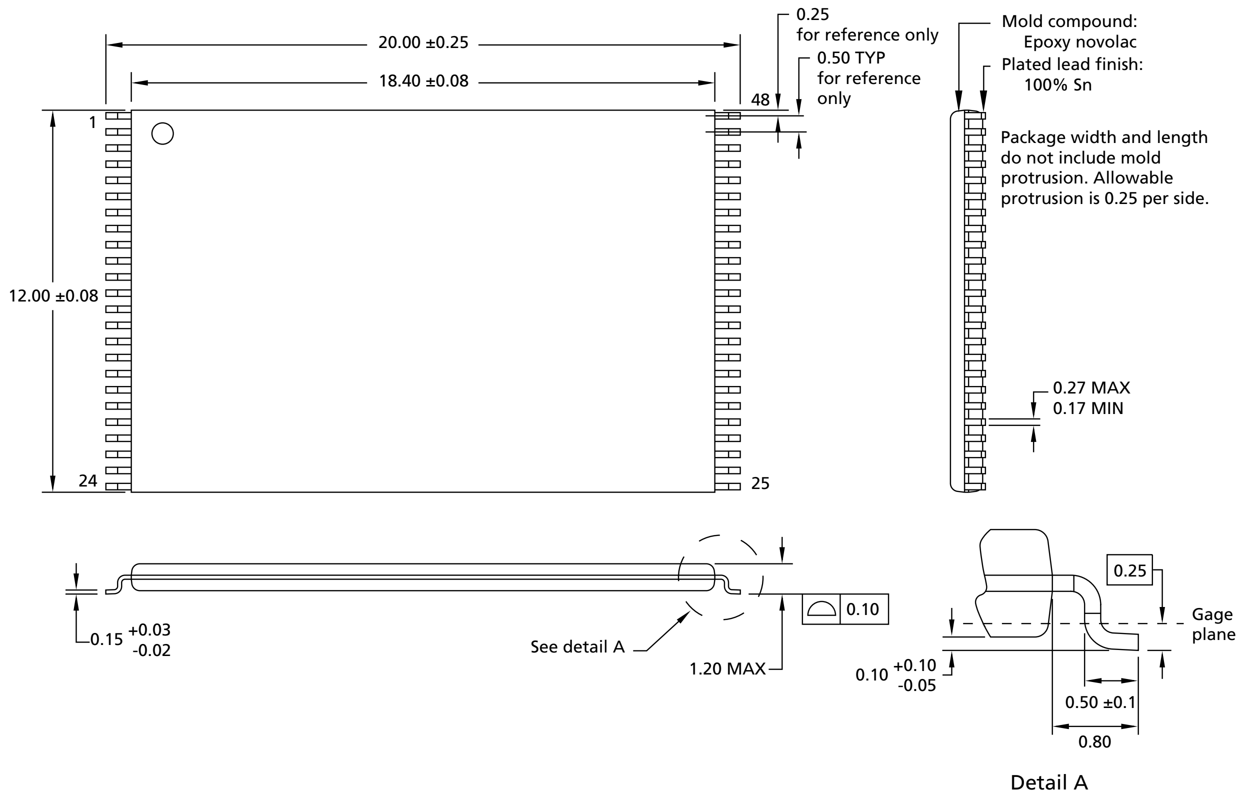
Note: 1. These pins might not be bonded in the package; however, Micron recommends that the customer connect these pins to the designated external sources for ONFI compatibility.

Figure 4: 63-Ball VFBGA, x16 (Balls Down, Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	Vss	CE#	WE#	R/B#		
D			V_{CC}	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	V_{SS}	NC		
G			DNU	V_{CC}	LOCK	I/O13	I/O15	NC		
H			I/O8	I/O0	I/O10	I/O12	I/O14	V_{CC}		
J			I/O9	I/O1	I/O11	V_{CC}	I/O5	I/O7		
K			V_{SS}	I/O2	I/O3	I/O4	I/O6	V_{SS}		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

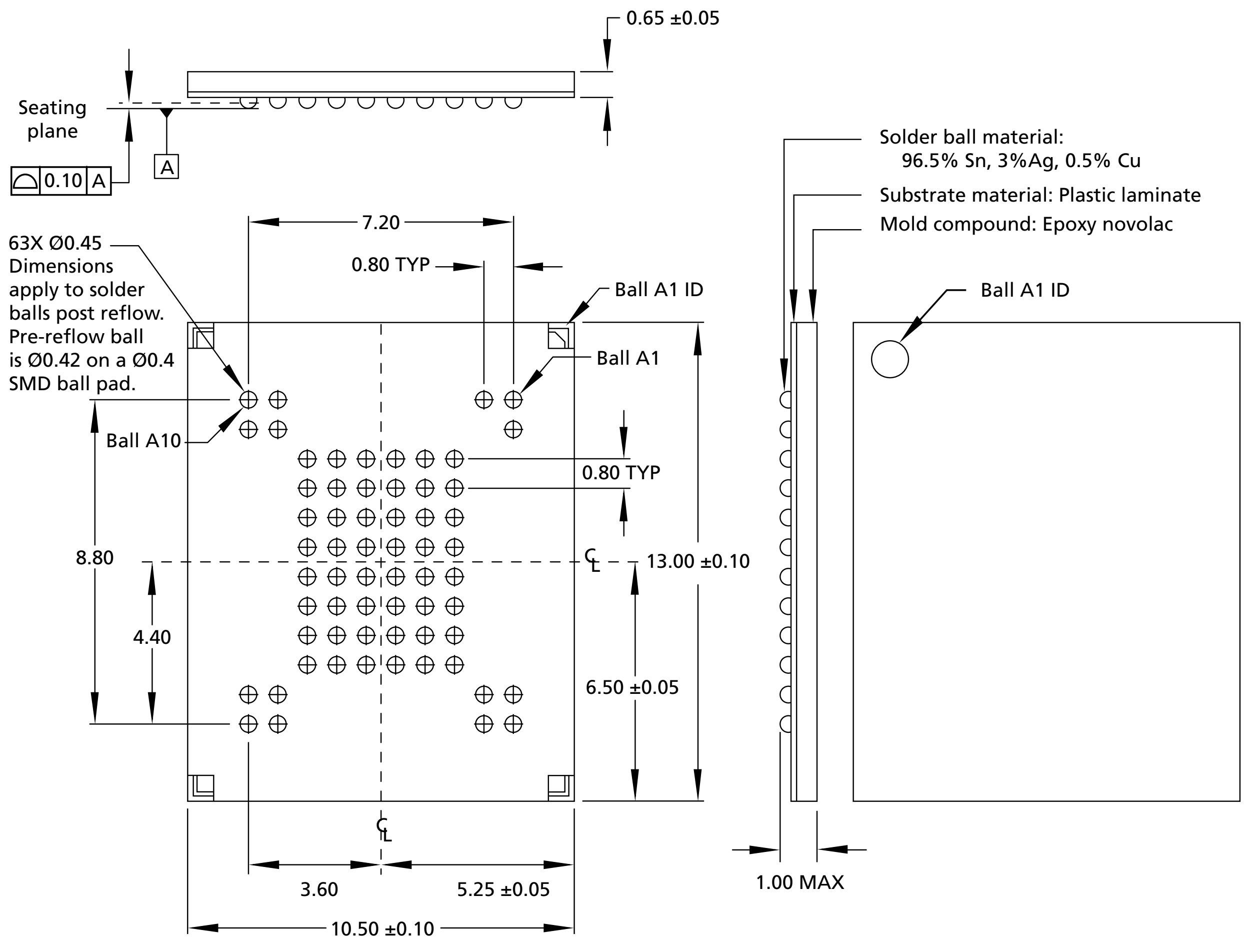
Package Dimensions

Figure 5: 48-Pin TSOP – Type 1, CPL



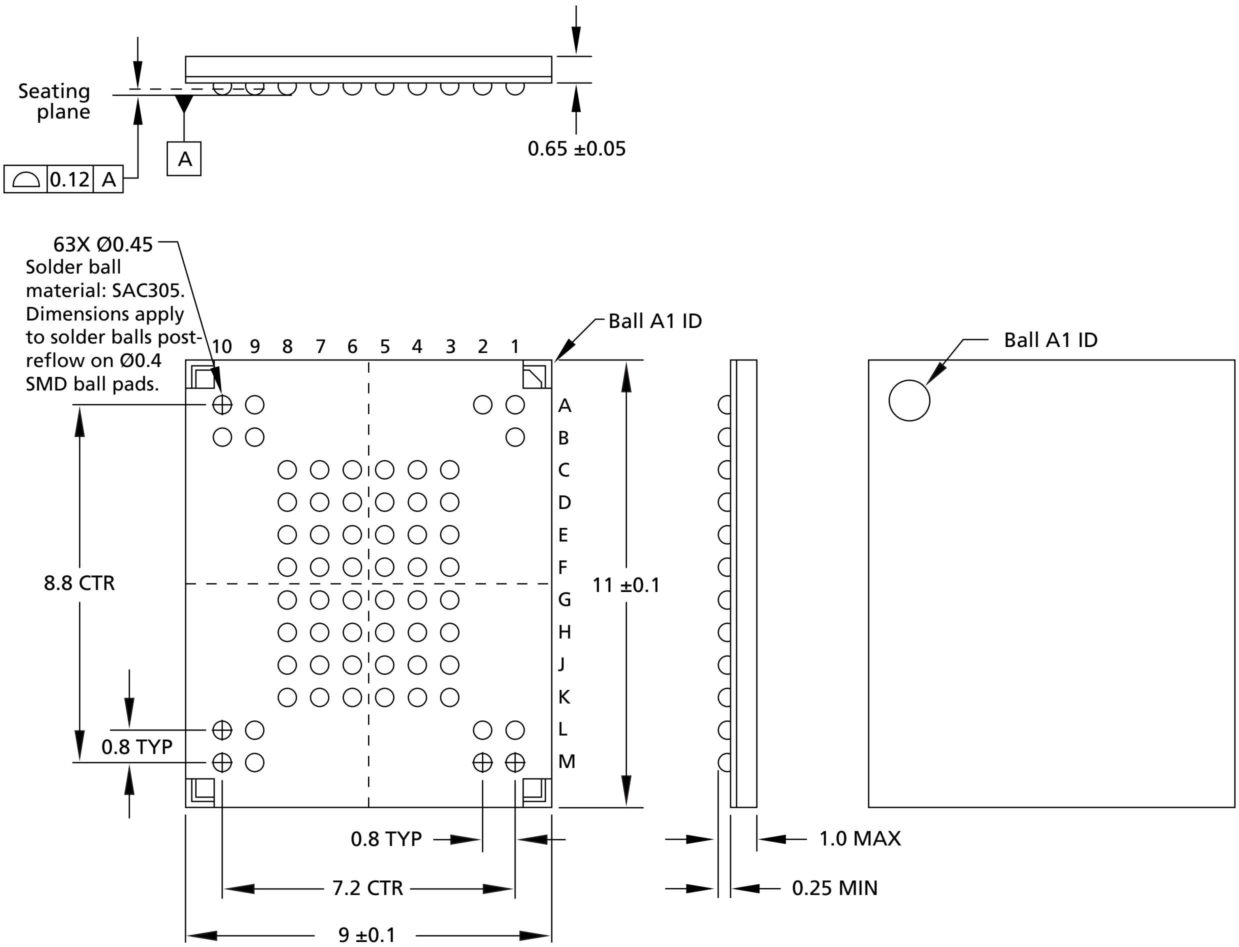
Note: 1. All dimensions are in millimeters.

Figure 6: 63-Ball VFBGA (HC)



Note: 1. All dimensions are in millimeters.

Figure 7: 63-Ball VFBGA (H4) 9mm x 11mm



Note: 1. All dimensions are in millimeters.

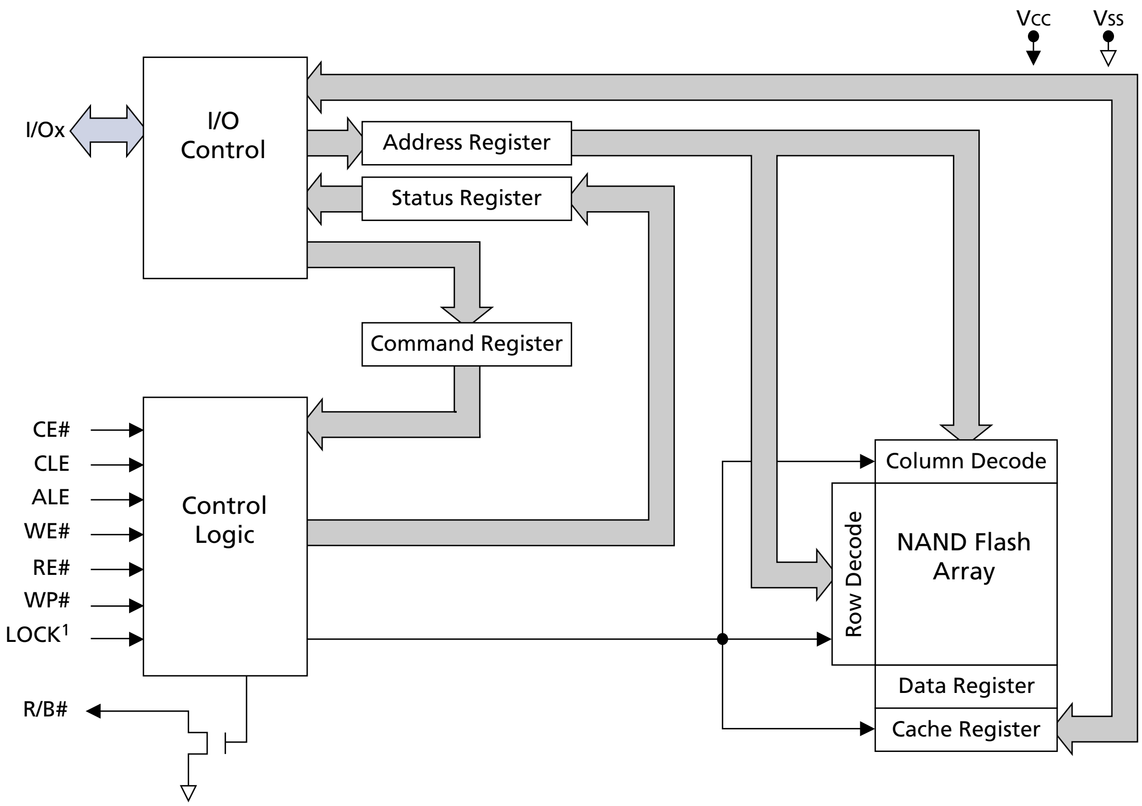
Architecture

These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte (x8) or word by word (x16), through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput. The status register reports the status of die operations.

Figure 8: NAND Flash Die (LUN) Functional Block Diagram



Note: 1. The LOCK pin is used on the 1.8V device.

Device and Array Organization

Figure 9: Array Organization – x8

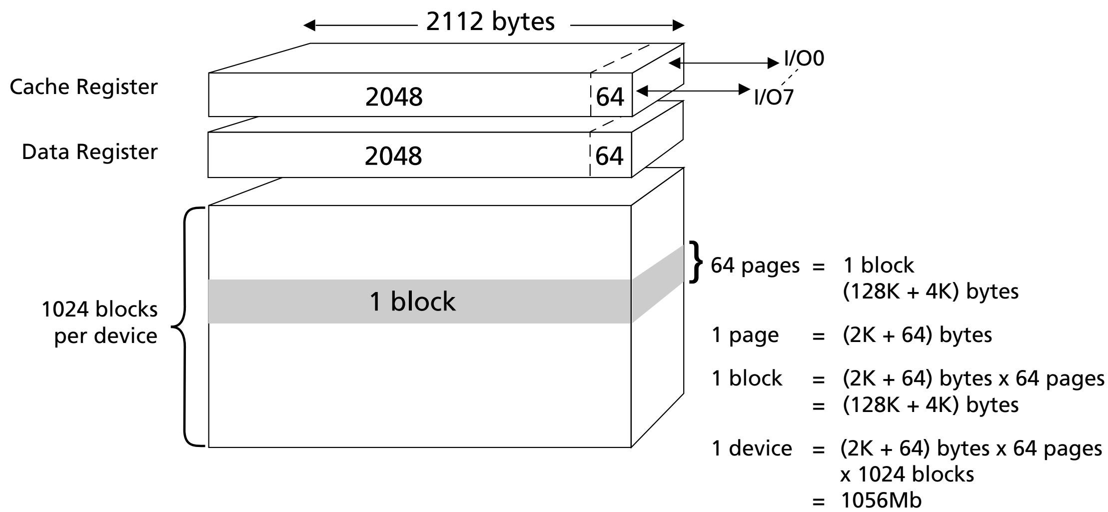


Table 2: Array Addressing (x8)

Cycle	I/O7	I/O6	I/O5	I/O4	I/OQ3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	CA11[1]	CA10	CA9	CA8
Third	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8

Notes:
1. If CA11 is 1, then CA[10:6] must be 0.
2. Block address concatenated with page address = actual page address; CAx = column address; PAx = page address; BAx = block address.

Figure 10: Array Organization – x16

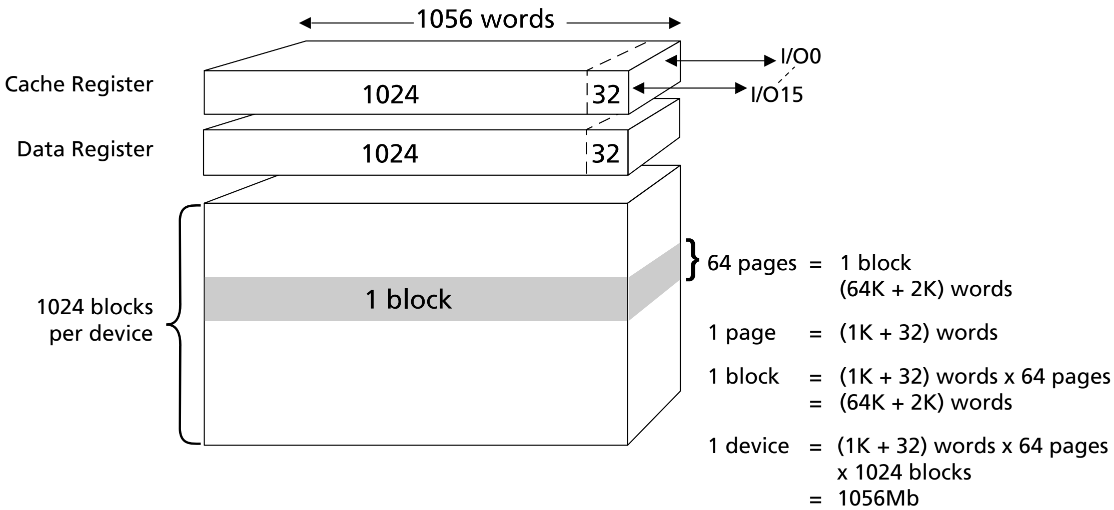


Table 3: Array Addressing (x16)

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10[1]	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8

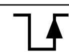
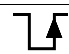
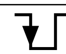
Notes:
1. If CA10 is 1, then CA[9:5] must be 0.
2. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
3. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

Asynchronous Interface Bus Operation

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O[15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O[7:0].

The command sequence normally consists of a COMMAND LATCH cycle, ADDRESS INPUT cycles, and one or more DATA cycles—either READ or WRITE.

Table 4: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	I/Ox	WP#	Notes
Standby	H	X	X	X	X	X	0V/V_{CC}	1
Command input	L	H	L		H	X	H	
Address input	L	L	H		H	X	H	
Data input	L	L	L		H	X	H	
Data output	L	L	L	H		X	X	
Write protect	X	X	X	X	X	X	L	

Notes: 1. WP# should be biased to CMOS LOW or HIGH for standby.
2. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standby

When the device is not performing an operation, the CE# pin is typically driven HIGH and the device enters standby mode. The memory will enter standby if CE# goes HIGH while data is being transferred and the device is not busy. This helps reduce power consumption.

The CE# “Don’t Care” operation enables the NAND Flash to reside on the same asynchronous memory bus as other Flash or SRAM devices. Other devices on the memory bus can then be accessed while the NAND Flash is busy with internal operations. This capability is important for designs that require multiple NAND Flash devices on the same bus.

A HIGH CLE signal indicates that a command cycle is taking place. A HIGH ALE signal signifies that an ADDRESS INPUT cycle is occurring.

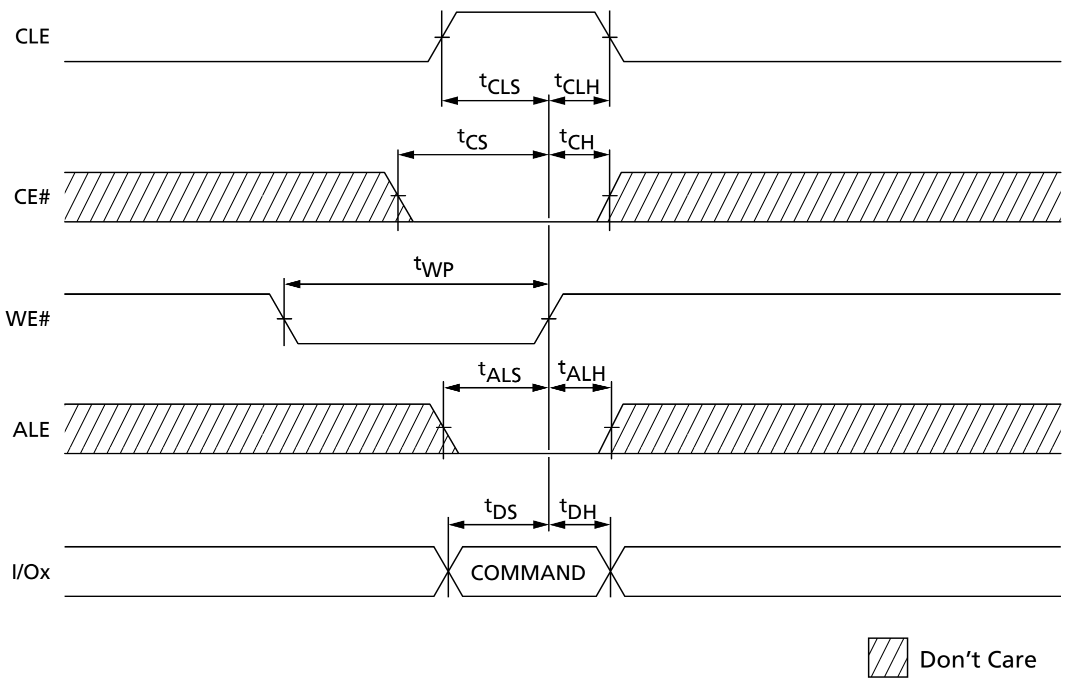
Asynchronous Commands

An asynchronous command is written from I/O[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h), are accepted by die (LUNs) even when they are busy.

For devices with a x16 interface, I/O[15:8] must be written with zeros when a command is issued.

Figure 11: Asynchronous Command Latch Cycle



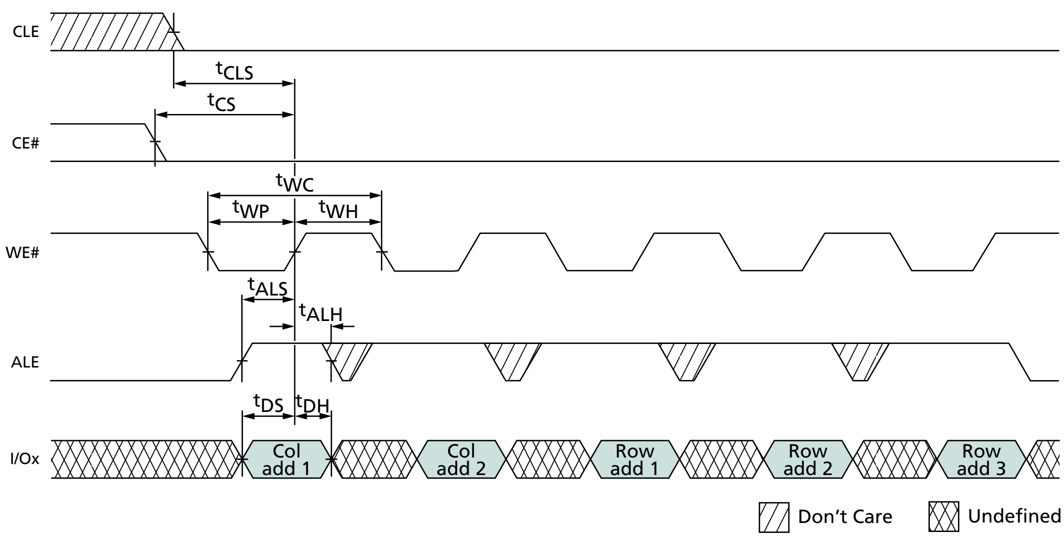
Asynchronous Addresses

An asynchronous address is written from I/O[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization.) The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are input on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices.

Figure 12: Asynchronous Address Latch Cycle



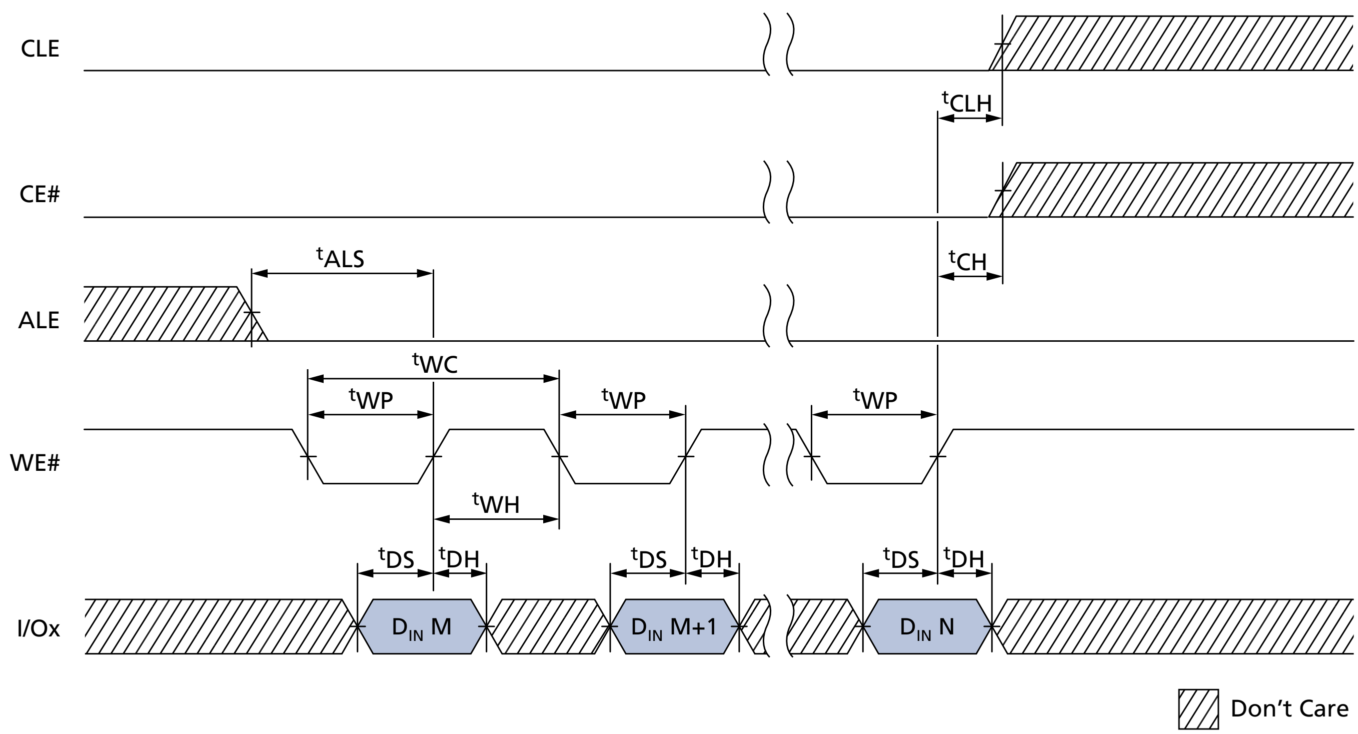
Asynchronous Data Input

Data is written to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0). Data is written to the data register on the rising edge of WE# when CE#, CLE, and ALE are LOW, and the device is not busy.

Data is input on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices.

Figure 13: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE# (see (page 0) for extended data output (EDO) timing).

Data is output on I/O[7:0] on x8 devices and on I/O[15:0] on x16 devices.

Figure 14: Asynchronous Data Output Cycles

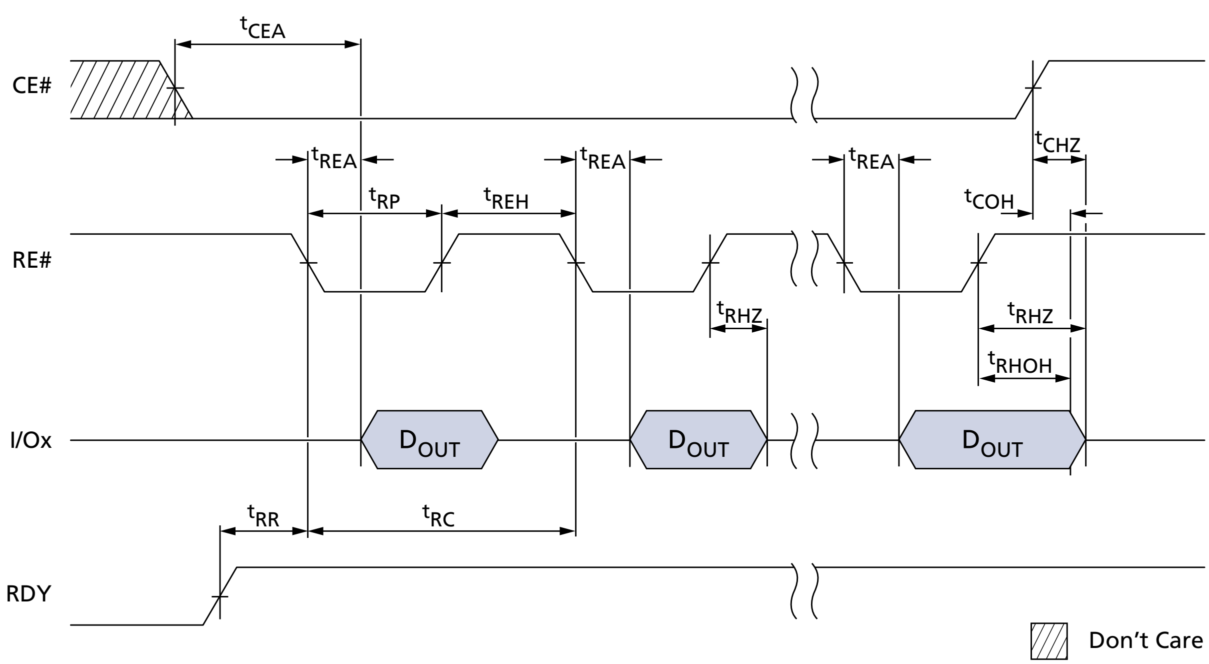
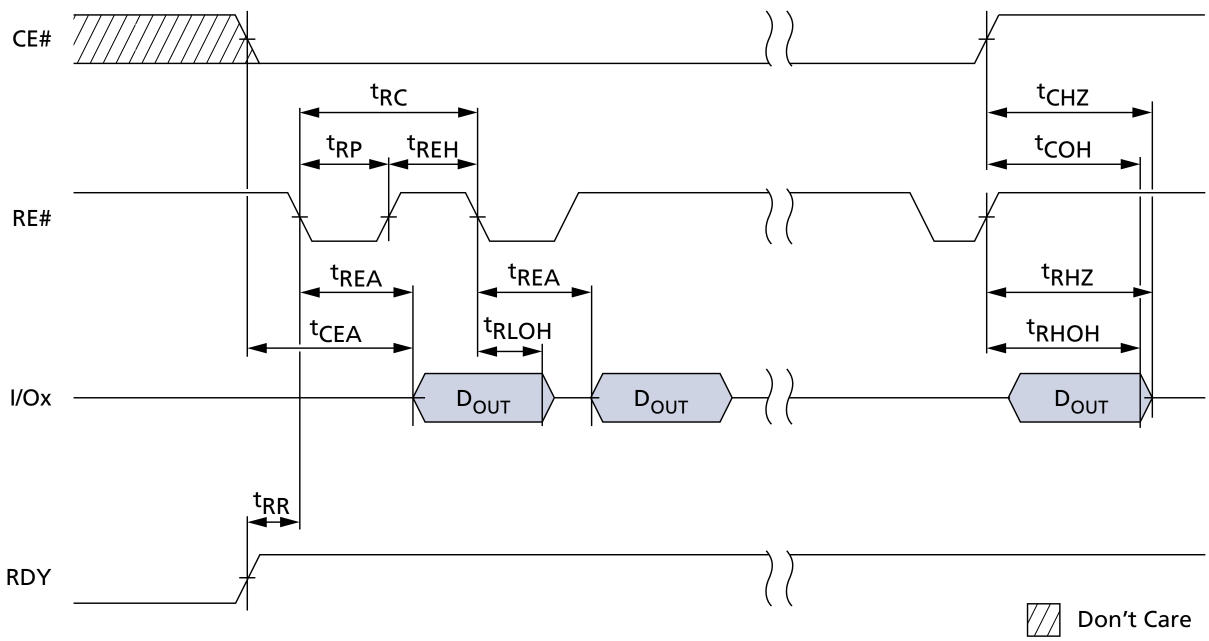


Figure 15: Asynchronous Data Output Cycles (EDO Mode)



Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc is stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization (page 28) for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = *Rp* (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 21 (page 27).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

$$Rp = \frac{V_{CC}\,(MAX) - V_{OL}\,(MAX)}{I_{OL} + \Sigma_{IL}}$$

Where Σ_{IL} is the sum of the input currents of all devices tied to the R/B# pin.

Figure 16: READ/BUSY# Open Drain

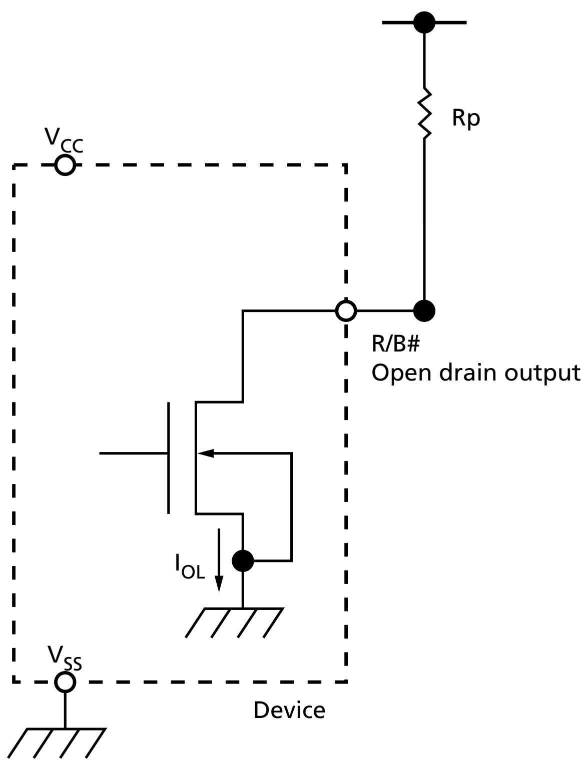
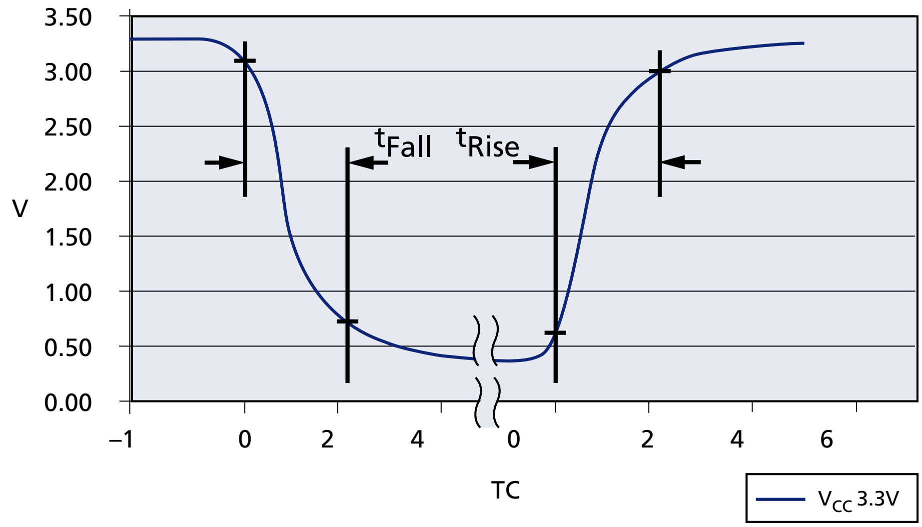
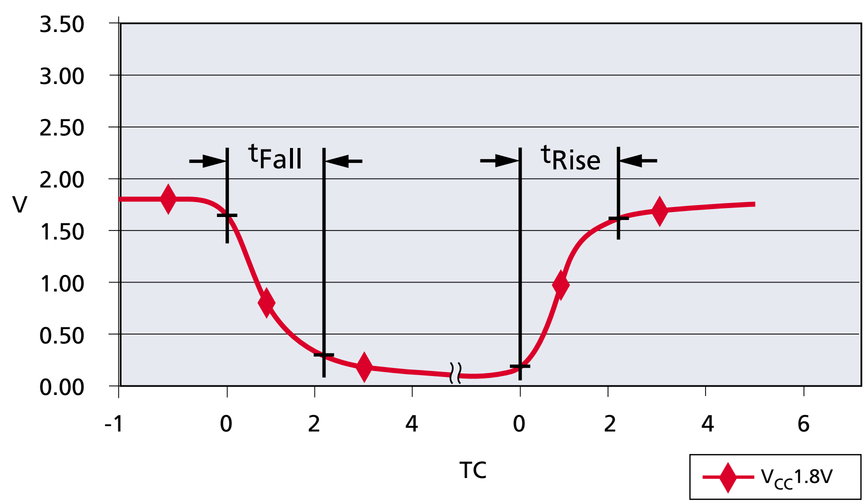


Figure 17: ^{t}Fall and ^{t}Rise (3.3V V_{CC})



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10% and 90% points.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall = 10ns at 3.3V
5. See TC values in Figure 21 (page 27) for approximate Rp value and TC.

Figure 18: ^{t}Fall and ^{t}Rise (1.8V V_{CC})



Notes:
1. ^{t}Fall and ^{t}Rise are calculated at 10% and 90% points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 21 (page 27) for TC and approximate Rp value.

Figure 19: I_{OL} vs Rp (V_{CC} = 3.3V V_{CC})

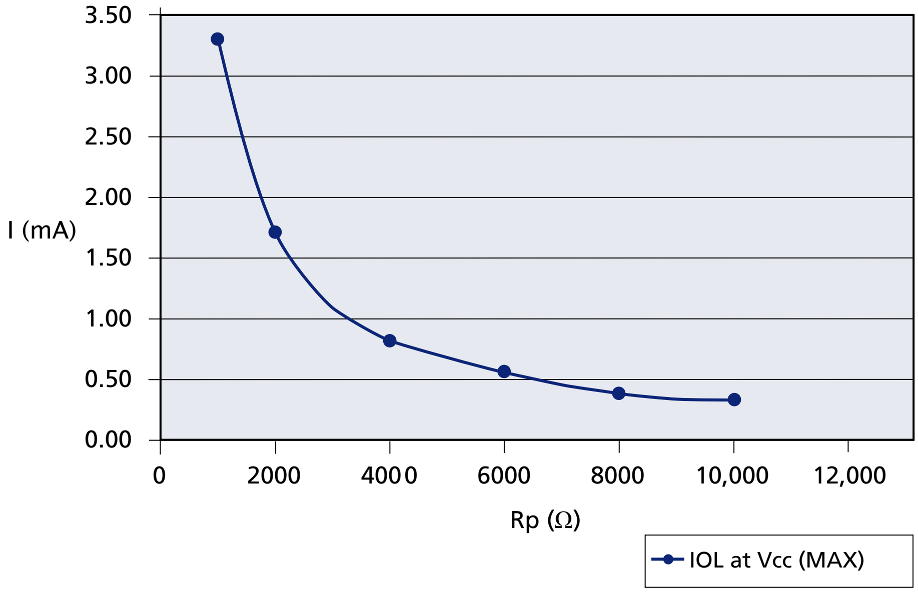


Figure 20: I_{OL} vs Rp (1.8V V_{CC})

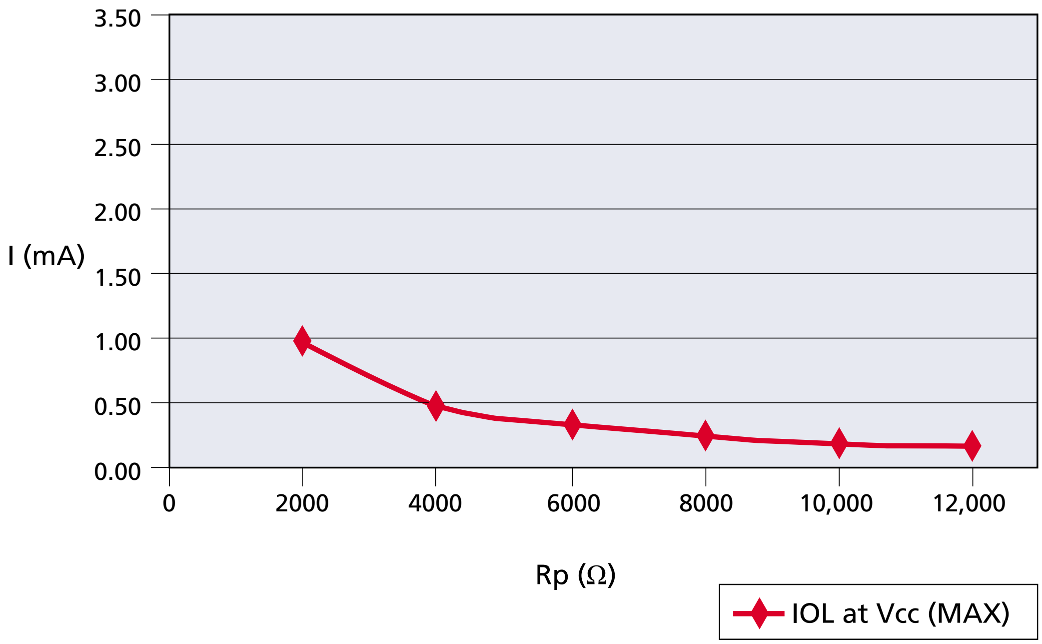
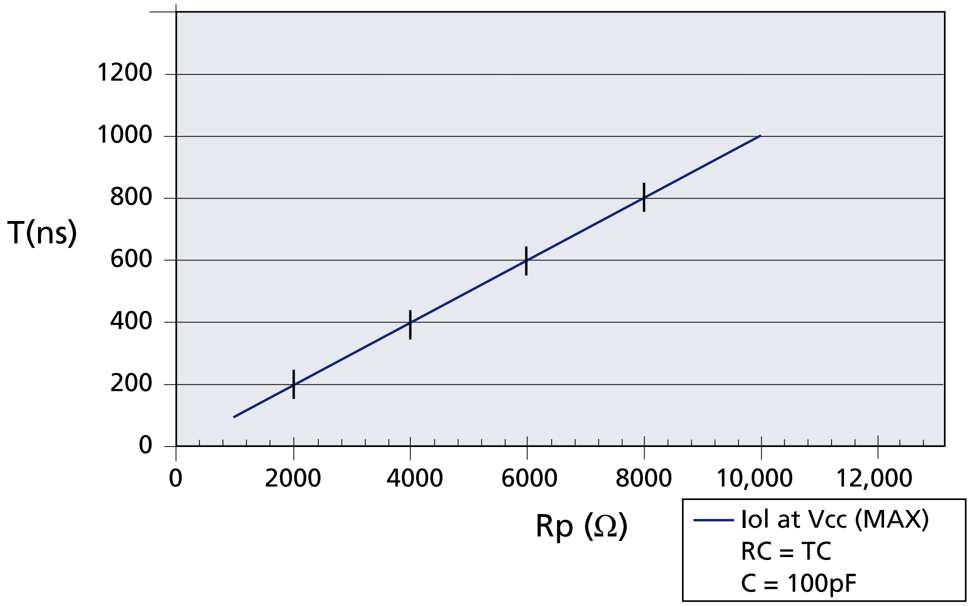


Figure 21: TC vs Rp

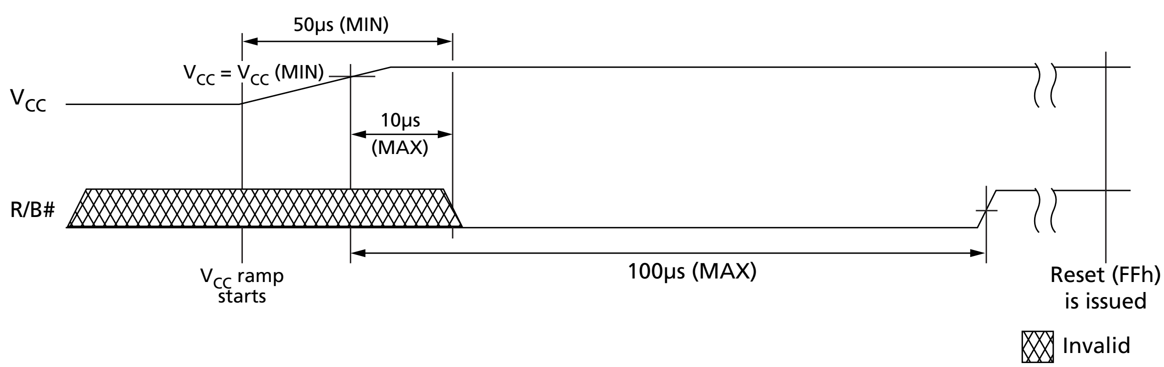


Device Initialization

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CC} reaches V_{CC} (MIN).
3. If not monitoring R/B#, the host must wait at least 100µs after V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
4. The asynchronous interface is active by default for each target. Each LUN draws less than an average of 10mA (I_{ST}) measured over intervals of 1ms until the RESET (FFh) command is issued.
5. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for 1ms after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
6. The device is now initialized and ready for normal operation.

Figure 22: R/B# Power-On Behavior



Command Definitions

Table 5: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Notes
Rest Operations						
RESET	FFh	0	–	–	Yes	
Identification Operations						
READ ID	90h	1	–	–	No	2
READ PARAMETER PAGE	ECh	1	–	–	No	
READ UNIQUE ID	EDh	1	–	–	No	
Feature Operations						
GET FEATURES	EEh	1	–	–	No	2
SET FEATURES	EFh	1	4	–	No	3
Status Operations						
READ STATUS	70h	0	–	–	Yes	
Column Address Operations						
RANDOM DATA READ	05h	2	–	E0h	No	
RANDOM DATA INPUT	85h	2	Optional	–	No	
PROGRAM FOR INTERNAL DATA MOVE	85h	4	Optional	–	No	
Read Operations						
READ MODE	00h	0	–	–	No	
READ PAGE	00h	4	–	30h	No	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	No	4
READ PAGE CACHE RANDOM	00h	4	–	31h	No	4
READ PAGE CACHE LAST	3Fh	0	–	–	No	4
Program Operations						
PROGRAM PAGE	80h	4	Yes	10h	No	
PROGRAM PAGE CACHE	80h	4	Yes	15h	No	5
Erase Operations						
ERASE BLOCK	60h	2	–	D0h	No	
Internal Data Move Operations						
READ FOR INTERNAL DATA MOVE	00h	4	–	35h	No	
PROGRAM FOR INTERNAL DATA MOVE	85h	4	Optional	10h	No	
Boot Block Operations						

Table 5: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid While Selected LUN is Busy[1]	Notes
BOOT BLOCK PROTECT	80h	4	Yes	10h	No	6
Block Lock Operations						
BLOCK UNLOCK LOW	23h	2	–	–	No	
BLOCK UNLOCK HIGH	24h	2	–	–	No	
BLOCK LOCK	2Ah	–	–	–	No	
BLOCK LOCK-TIGHT	2Ch	–	–	–	No	
BLOCK LOCK READ STATUS	7Ah	2	–	–	No	
One-Time Programmable (OTP) Operations						
OTP DATA LOCK BY PAGE (ONFI)	80h	4	No	10h	No	7, 8
OTP DATA PROGRAM (ONFI)	80h	4	Yes	10h	No	7, 8
OTP DATA READ (ONFI)	00h	4	No	30h	No	7, 8

Notes:
1. Busy means RDY = 0.
2. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
3. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
4. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
5. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
6. The BOOT BLOCK PROTECT command can only be issued after issuing the SET FEATURES command with the feature address.
7. Read page cache sequential is not supported on OTP pages.
8. OTP commands can be entered only after issuing the SET FEATURES command with the feature address.

Reset Operations

RESET (FFh)

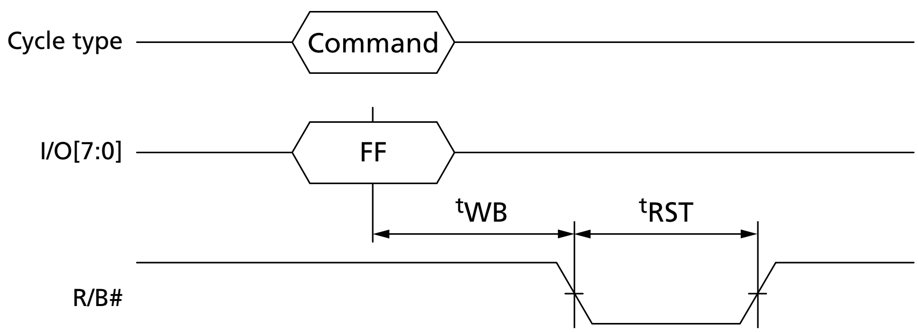
The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The command register is cleared and is ready for the next command. The data register and cache register contents are marked invalid.

The status register contains the value E0h when WP# is HIGH; otherwise it is written with a 60h value. R/B# goes LOW for ^{t}RST after the RESET command is written to the command register.

The RESET command must be issued to all CE#s as the first command after power-on. The device will be busy for a maximum of 1ms.

Figure 23: RESET (FFh) Operation



Identification Operations

READ ID (90h)

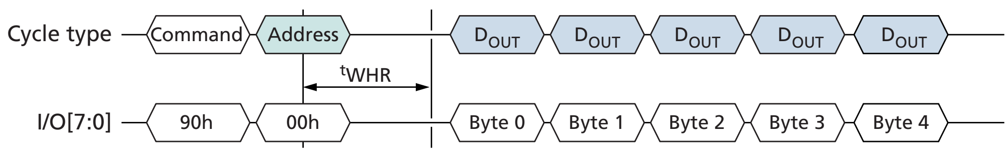
The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

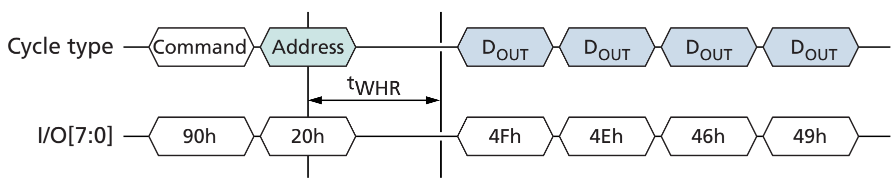
When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

Figure 24: READ ID (90h) with 00h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 25: READ ID (90h) with 20h Address Operation



Note: 1. See READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 6: READ ID Parameters for Address 00h

		Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]
Byte 0 – Manufacturer ID											
Manufacturer		Micron	0	0	1	0	1	1	0	0	2Ch
Byte 1 – Device ID											
MT29F1G08AAC		1Gb, x8, 3.3V	1	1	1	1	0	0	0	1	F1h
MT29F1G08ABC		1Gb, x8, 1.8V	1	0	1	0	0	0	0	1	A1h
MT29F1G16ABC		1Gb, x16, 1.8V	1	0	1	1	0	0	0	1	B1h
Byte 2											
Number of die per CE		1							0	0	00b
Cell type		SLC					0	0			00b
Number of simultaneously programmed pages		1			0	0					00b
Interleaved operations between multiple die		Not supported		0							0b
Cache programming		Supported	1								1b
Byte value	MT29F1G08AAC	1Gb, x8, 3.3V	1	0	0	0	0	0	0	0	80h
	MT29F1G08ABC	1Gb, x8, 1.8V	1	0	0	0	0	0	0	0	80h
	MT29F1G16ABC	1Gb, x16, 1.8V	1	0	0	0	0	0	0	0	80h
Byte 3											
Page size		2KB							0	1	01b
Spare area size (bytes)		64B						1			1b
Block size (w/o spare)		128KB			0	1					01b
Organization		1Gb, x8, 3.3V, 1.8V		0							0b
		1Gb, x16, 1.8V		1							1b
Serial access (MIN)		35ns (1.8V)	0				0				0xxx0b
		25ns (3.3V)	1				0				1xxx0b
Byte value		MT29F1G08AAC	1	0	0	1	0	1	0	1	95h
		MT29F1G08ABC	0	0	0	1	0	1	0	1	15h
		MT29F1G16ABC	0	1	0	1	0	1	0	1	55h
Byte 4											
Reserved									0	0	00b
Planes per CE#		1					0	0			00b
Plane size		1Gb		0	0	0					000b
Reserved			0								0b
Byte value		3.3V	0	0	0	0	0	0	0	0	00h
		1.8V	0	0	0	0	0	0	0	0	00h

Note: 1. b = binary; h = hexadecimal.

Table 7: READ ID Parameters for Address 20h

Byte	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value[1]
0	"O"	0	1	0	0	1	1	1	1	4Fh
1	"N"	0	1	0	0	1	1	1	0	4Eh
2	"F"	0	1	0	0	0	1	1	0	46h
3	"I"	0	1	0	0	1	0	0	1	49h

Note: 1. h = hexadecimal.

READ PARAMETER PAGE (ECh)

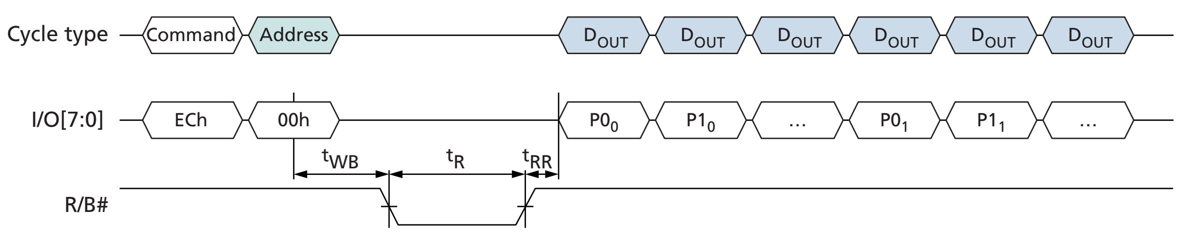
The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the location of data output.

Figure 26: READ PARAMETER (ECh) Operation



Parameter Page Data Structure Tables

Table 8: Parameter Page Data Structure

Byte	Description		Value
0–3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4–5	Revision number		02h, 00h
6–7	Features supported	MT29F1G08ABC	10h, 00h
		MT29F1G16ABC	11h, 00h
		MT29F1G08AAC	
8–9	Optional commands supported		3Fh, 00h
10–31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32–43	Device manufacturer		4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model	MT29F1G08ABC	4Dh, 54h, 32h, 39h, 46h, 31h, 47h, 30h, 38h, 41h, 42h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F1G16ABC	4Dh, 54h, 32h, 39h, 46h, 31h, 47h, 31h, 36h, 41h, 42h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		MT29F1G08AAC	4Dh, 54h, 32h, 39h, 46h, 31h, 47h, 30h, 38h, 41h, 41h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		2Ch
65–66	Date code		00h,00h
67–79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80–83	Number of data bytes per page		00h, 08h, 00h, 00h
84–85	Number of spare bytes per page		40h, 00h
86–89	Number of data bytes per partial page		00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page		10h, 00h
92–95	Number of pages per block		40h, 00h, 00h, 00h
96–99	Number of blocks per unit		00h, 04h, 00h, 00h
100	Number of logical units		01h
101	Number of address cycles		22h
102	Number of bits per cell		01h
103–104	Bad blocks maximum per unit		14h, 00h
105–106	Block endurance		01h, 05h
107	Guaranteed valid blocks at beginning of target		01h
108–109	Block endurance for guaranteed valid blocks		00h, 00h
110	Number of programs per page		04h
111	Partia lprogramming attributes		00h
112	Number of ECC bits		01h
113	Number of interleaved address bits		00h
114	Interleaved operation attributes		00h

Table 8: Parameter Page Data Structure (Continued)

Byte	Description		Value
115–127	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance		0Ah
129–130	Timing mode support	MT29F1G08ABC	07h, 00h
		MT29F1G16ABC	07h, 00h
		MT29F1G08AAC	1Fh, 00h
131–132	Program cache timing	MT29F1G08ABC	07h, 00h
		MT29F1G16ABC	07h, 00h
		MT29F1G08AAC	1Fh, 00h
133–134	^{t}PROG maximum page program time		BCh, 02h
135–136	^{t}BERS maximum block erase time		B8h, 0Bh
137–138	^{t}R maximum page read time		19h, 00h
139–140	^{t}CCS minimum	MT29F1G08ABC	64h, 00h
		MT29F1G16ABC	64h, 00h
		MT29F1G08AAC	46h, 00h
141–163	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164–165	Vendor-specific revision number		01h, 00h
166–253	Vendor specific		00h, 00h, 00h, 02h, 04h, 80h, 01h, 81h, 04h, 02h, 02h, 01h, 1Eh, 90h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254–255	Integrity CRC		Set at shipment
256–511	Value of bytes 0–255		
512–767	Value of bytes 0–255		
768+	Additional redundant parameter pages		

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

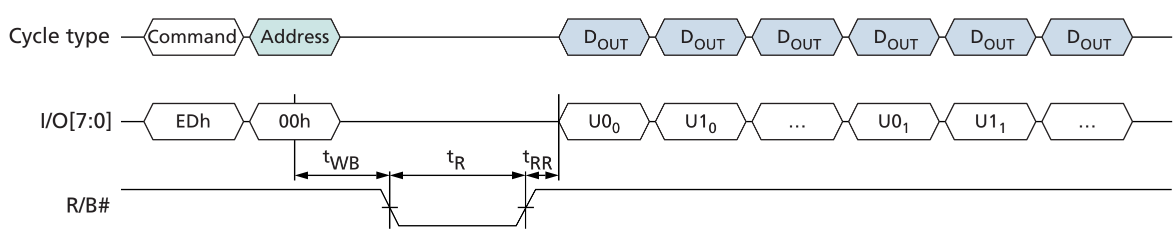
When the EDh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the RANDOM DATA READ (05h-E0h) command can be used to change the data output location.

The upper eight I/Os on a x16 device are not used and are a "Don't Care" for x16 devices.

Figure 27: READ UNIQUE ID (EDh) Operation



Feature Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in below. The SET FEATURES (EFh) command writes subfeature parameters (P1–P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1–P4) at the specified feature address.

Table 9: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–FFh	Reserved
90h	Array operation mode (1.8V only)

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1–P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

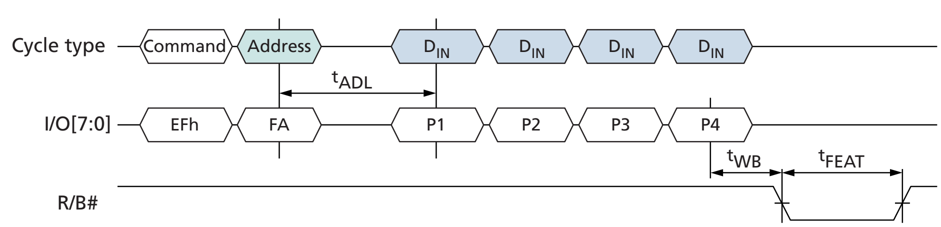
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in . The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC.

Figure 28: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1–P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for ^{t}FEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters.

Figure 29: GET FEATURES (EEh) Operation

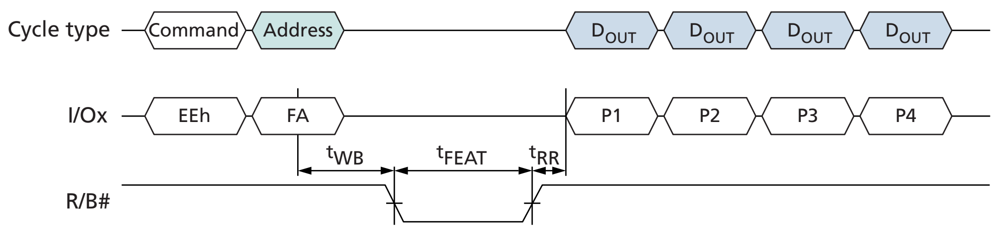


Table 10: Feature Addresses 01h: Timing Mode

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1, 2
	Mode 1	Reserved (0)					0	0	1	01h	2
	Mode 2	Reserved (0)					0	1	0	02h	2
	Mode 3	Reserved (0)					0	1	1	03h	3
	Mode 4	Reserved (0)					1	0	0	04h	3
	Mode 5	Reserved (0)					1	0	1	05h	4
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Notes:
1. The timing mode feature address is used to change the default timing mode. The timing mode should be selected to indicate the maximum speed at which the device will receive commands, addresses, and data cycles. The five supported settings for the timing mode are shown. The default timing mode is mode 0. The device returns to mode 0 when the device is power cycled. Supported timing modes are reported in the parameter page.
2. Supported for both 1.8V and 3.3V.
3. Supported for 3.3V only.
4. Not supported.

Table 11: Feature Addresses 80h: Programmable I/O Drive Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. The programmable drive strength feature address is used to change the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive strength settings. The default drive strength is full strength. The device returns to the default drive strength mode when the device is power cycled. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.

Table 12: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarters							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 13: Features Address 90h: Operation Mode

Note:

These bits are reset to 00h on power cycle.

Subfeature Parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Operation mode operation	Normal	Reserved (0)							0	00h	1
	OTP operation	Reserved (0)							1	01h	
	OTP protection	Reserved (0)						1	1	03h	
	Boot block lock	Reserved (0)					1	0	0	04h	
P2											
Reserved		Reserved (0)								00h	
P3											
Reserved		Reserved (0)								00h	
P4											
Reserved		Reserved (0)								00h	

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) command is issued, status register output is enabled. The contents of the status register are returned on I/O[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^tR) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see Read Operations).

Table 14: Status Register Definition

SR Bit	Program Page	Program Page Cache Mode	Page Read	Page Read Cache Mode	Block Erase	Description
7	Write protect	Write protect	Write protect	Write protect	Write protect	0 = Protected 1 = Not protected
6	RDY	RDY[2] cache	RDY	RDY[2] cache	RDY	0 = Busy 1 = Ready
5	ARDY	ARDY[1]	ARDY	ARDY[1]	ARDY	0 = Busy 1 = Ready
4	–	–	–	–	–	Reserved (0)
3	–	–	–	–	–	Reserved (0)
2	–	–	–	–	–	Reserved (0)
1	–	FAILC (N–1)	–	–	–	0 = Pass 1 = Fail
0	FAIL	FAIL (N)	–	–	FAIL	0 = Pass 1 = Fail

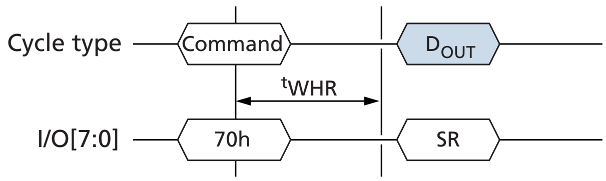
Notes:
1. Status register bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.
2. Status register bit 6 is 1 when the cache is ready to accept new data. R/B# follows bit 6.

READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

Figure 30: READ STATUS (70h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

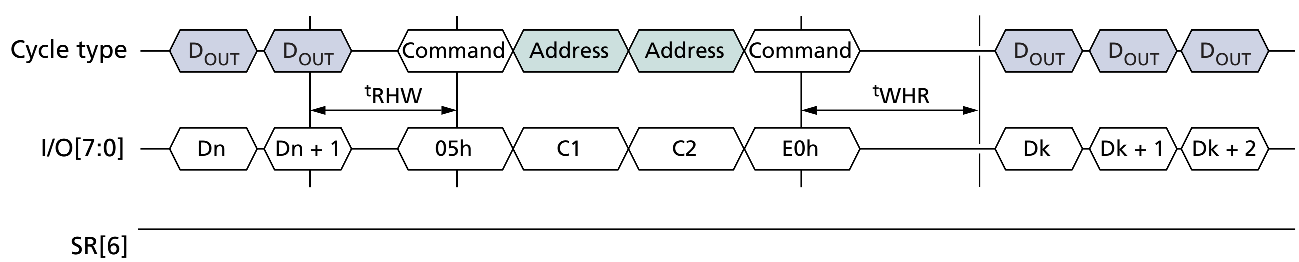
When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

RANDOM DATA READ (05h-E0h)

The RANDOM DATA READ (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}WHR before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

Figure 31: RANDOM DATA READ (05h-E0h) Operation



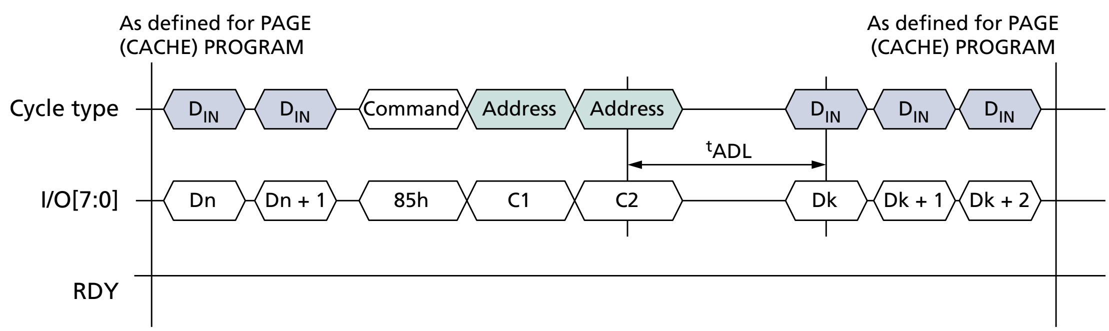
RANDOM DATA INPUT (85h)

The RANDOM DATA INPUT (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}ADL before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The RANDOM DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h), and PROGRAM FOR INTERNAL DATA MOVE (85h-10h).

Figure 32: RANDOM DATA INPUT (85h) Operation



PROGRAM FOR INTERNAL DATA INPUT (85h)

The PROGRAM FOR INTERNAL DATA INPUT (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected device for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}ADL before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE CACHE (80h-15h), and PROGRAM FOR INTERNAL DATA MOVE (85h-10h). When used with these commands, the LUN address and device select bits are required to be identical to the LUN address and device select bits originally specified.

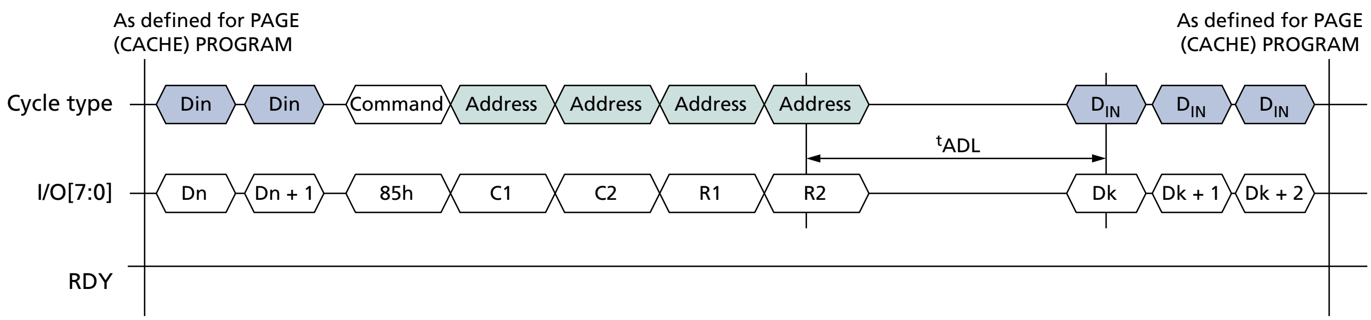
The PROGRAM FOR INTERNAL DATA INPUT (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used with the RANDOM DATA READ (05h-E0h) command to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM FOR INTERNAL DATA MOVE command sequence to modify one or more bytes of the original data. First, data is copied into the cache register using the 00h-35h command sequence, then the RANDOM DATA INPUT (85h) command is written along with the address of the data to be modified next. New data is input on the external data pins. This copies the new data into the cache register.

Figure 33: PROGRAM FOR INTERNAL DATA INPUT (85h) Operation



Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: RANDOM DATA READ (05h-E0h) and RANDOM DATA INPUT (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h) – copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h) – copies the page specified in this command from the NAND Flash array to its corresponding data register

After the READ PAGE CACHE series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h) and RESET (FFh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE series (31h, 00h-31h) operations are status operations (70h), READ MODE (00h), READ PAGE CACHE series (31h, 00h-31h), RANDOM DATA READ (05h-E0h), and RESET (FFh).

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-3Ah, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

READ PAGE (00h-30h)

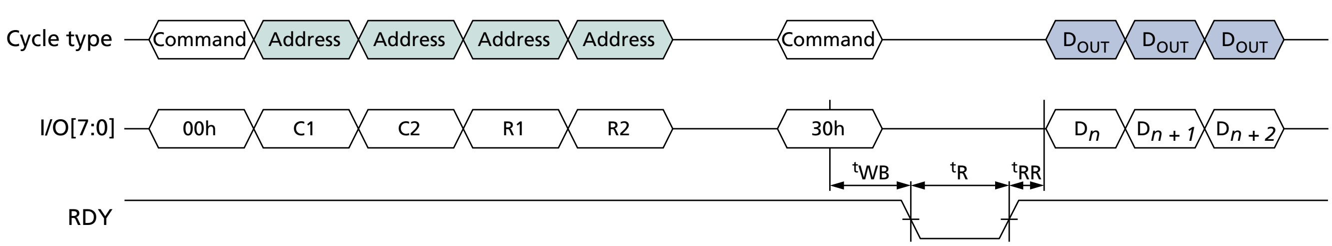
The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, then write *n* address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the RANDOM DATA READ (05h-E0h) command can be issued.

Figure 34: READ PAGE (00h-30h) Operation



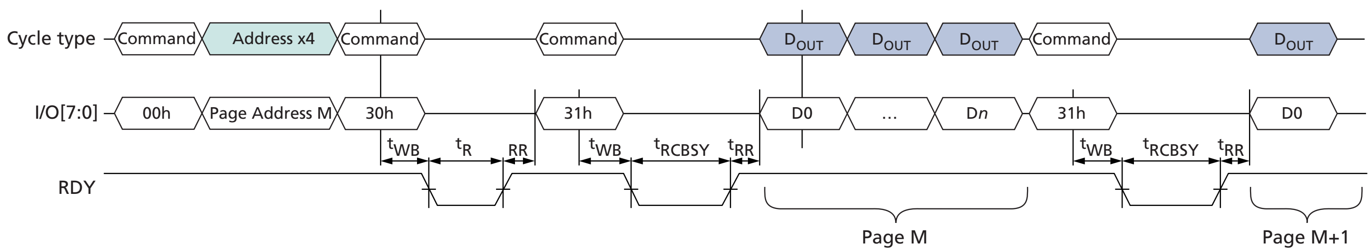
READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

Figure 35: READ PAGE CACHE SEQUENTIAL (31h) Operation



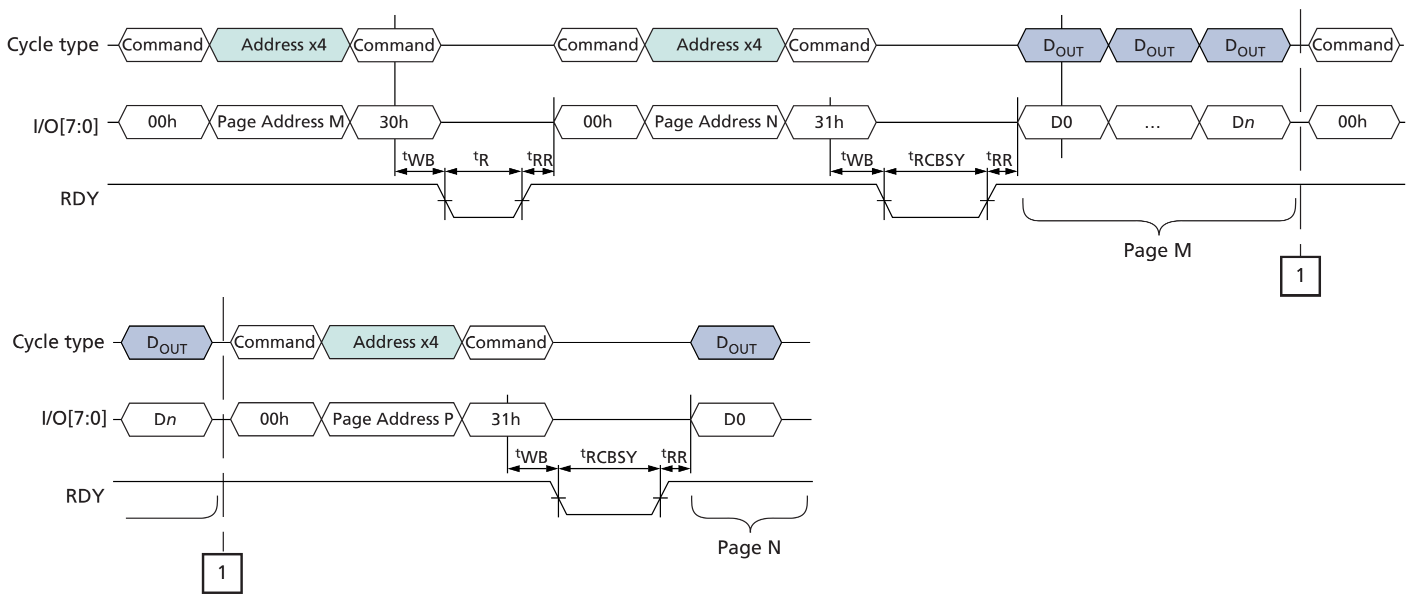
READ PAGE CACHE RANDOM (00h-31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write *n* address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

Figure 36: READ PAGE CACHE RANDOM (00h-31h) Operation

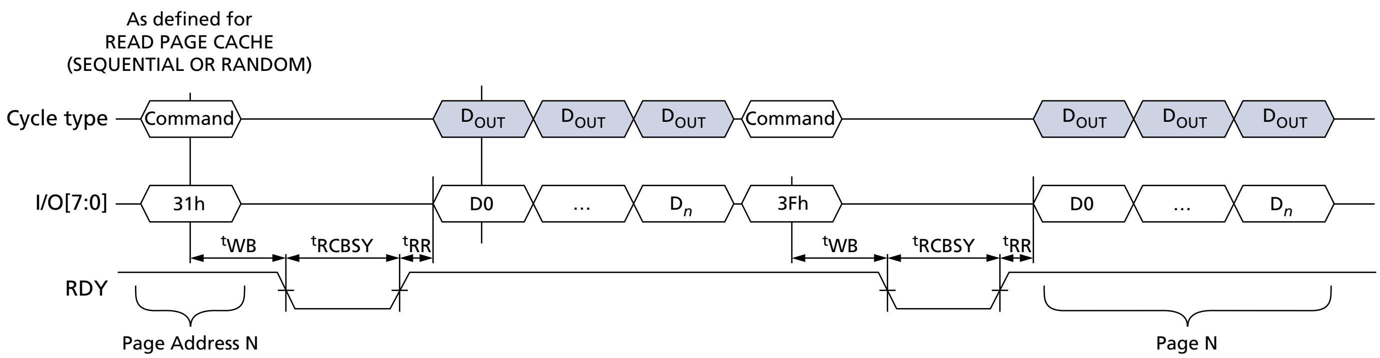


READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The RANDOM DATA READ (05h-E0h) command can be used to change the column address of the data being output from the cache register.

Figure 37: READ PAGE CACHE LAST (3Fh) Operation



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (0, 1, 2, ….., 63). During a program operation, the contents of the cache and/or data registers are modified by the internal control logic.

Program Operations

The PROGRAM PAGE (80h-10h) command programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operation (70h) and reset (FFh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE series (80h-15h) operations are status operation (70h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), RANDOM DATA INPUT (85h), PROGRAM FOR INTERNAL DATA INPUT (85h), and RESET (FFh).

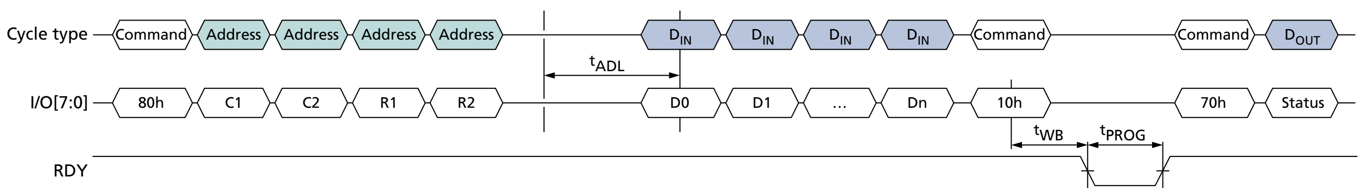
PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operation (70h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

Figure 38: PROGRAM PAGE (80h-10h) Operaton



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write *n* address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT (85h) and PROGRAM FOR INTERNAL DATA INPUT (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operation (70h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

Figure 39: PROGRAM PAGE CACHE (80h-15h) Operation (Start)

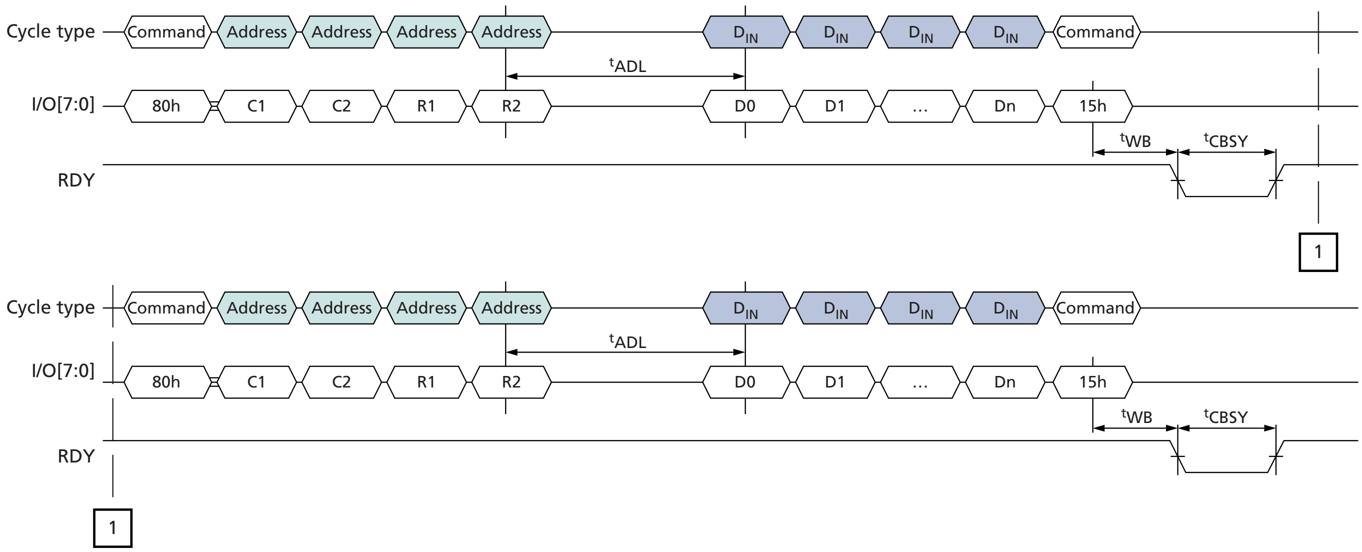
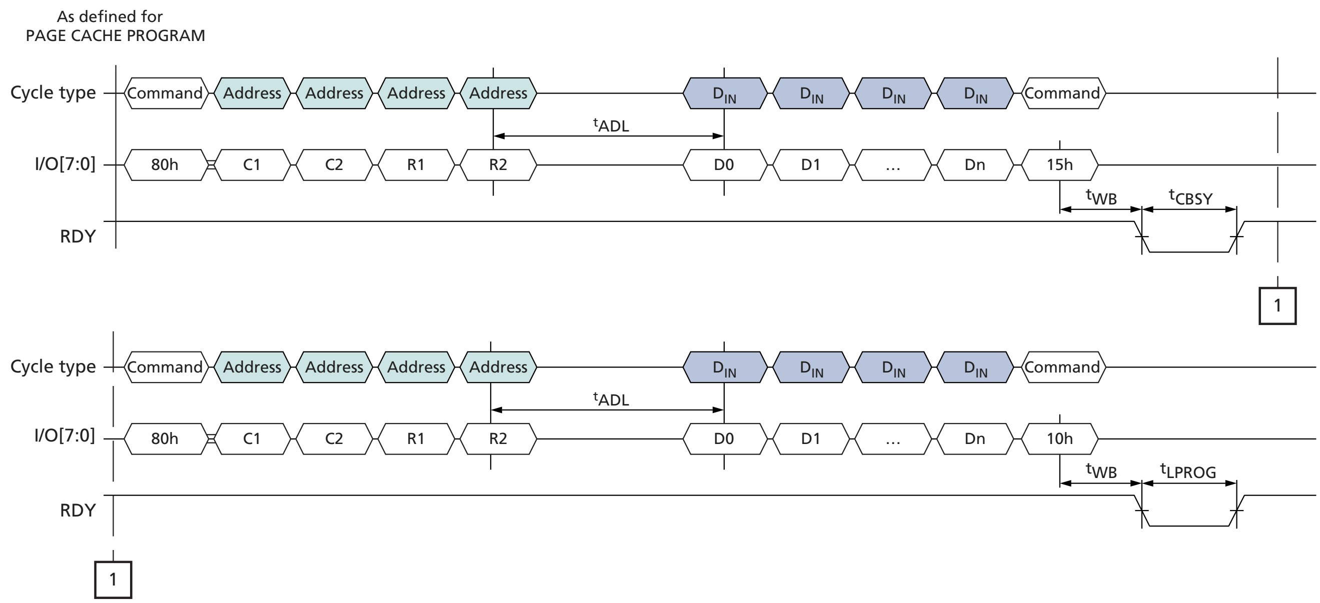


Figure 40: PROGRAM PAGE CACHE (80h-15h) Operation (End)



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

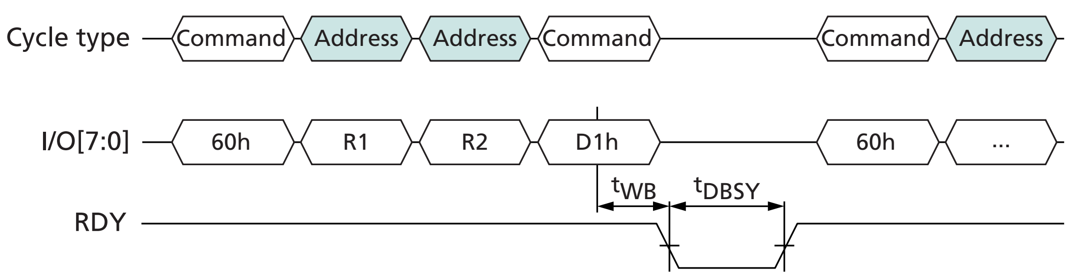
ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To erase a block, write 60h to the command register. Then write two address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operation (70h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

Figure 41: ERASE BLOCK (60h-D0h) Operation



Internal Data Move Operations

Internal data move operations make it possible to transfer data within a device from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The INTERNAL DATA MOVE operation is a two-step process consisting of a READ FOR INTERNAL DATA MOVE (00h-35h) and a PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. To move data from one page to another, first issue the READ FOR INTERNAL DATA MOVE (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple INTERNAL DATA MOVE operations, it is recommended that the host read the data out of the cache register after the READ FOR INTERNAL DATA MOVE (00h-35h) completes and prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command. The RANDOM DATA READ (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is issued, any corrected data can be input. The PROGRAM FOR INTERNAL DATA INPUT (85h) command can be used to change the column address.

Between the READ FOR INTERNAL DATA MOVE (00h-35h) and PROGRAM FOR INTERNAL DATA MOVE (85h-10h) commands, the following commands are supported: status operation (70h) and column address operations (05h-E0h, 85h). The RESET operation (FFh) can be issued after READ FOR INTERNAL DATA MOVE (00h-35h), but the contents of the cache registers on the target are not valid.

READ FOR INTERNAL DATA MOVE (00h-35h)

The READ FOR INTERNAL DATA MOVE (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command to prevent the propagation of data errors.

Figure 42: READ FOR INTERNAL DATA MOVE (00h-35h) Operation

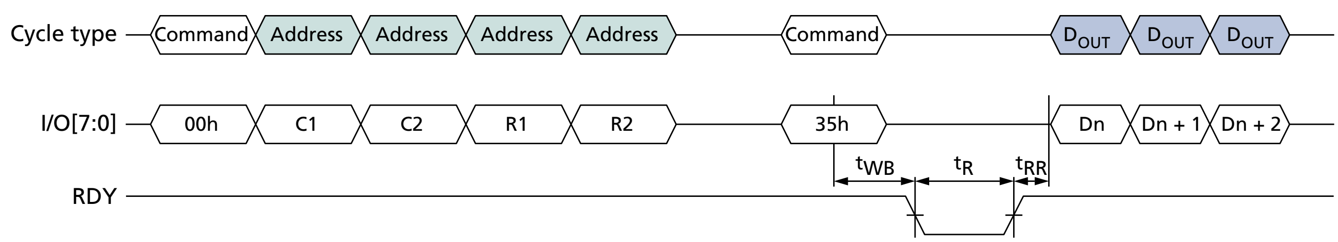
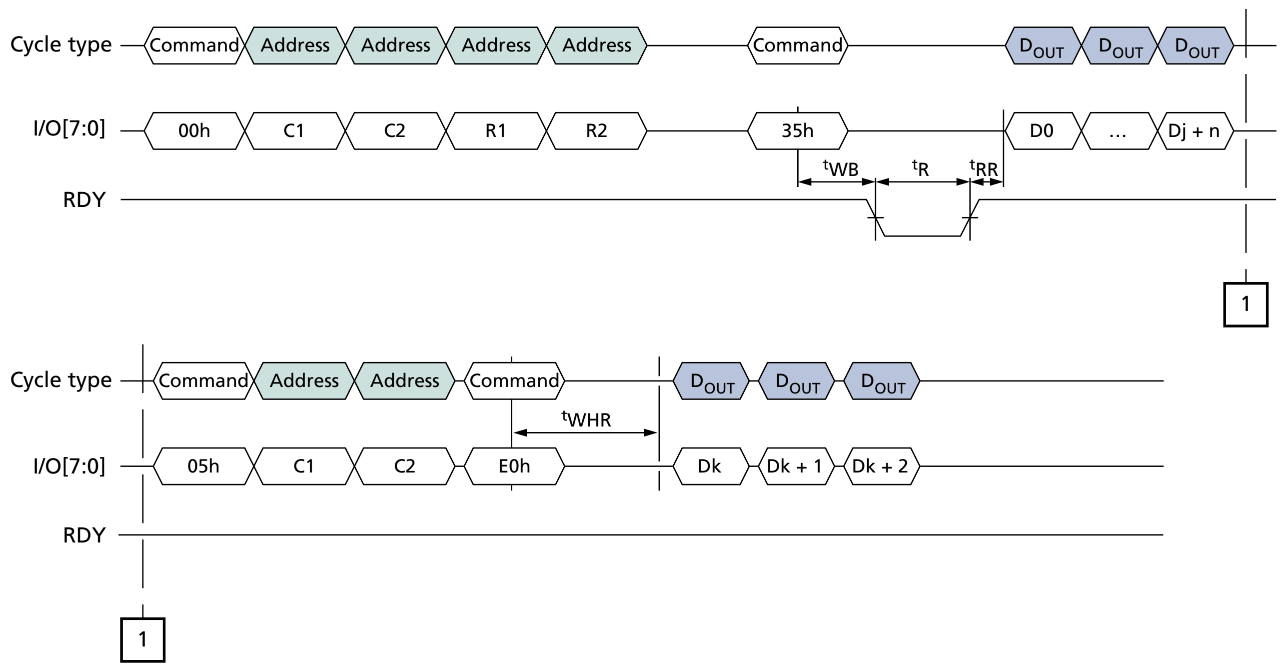


Figure 43: READ FOR INTERNAL DATA MOVE (00h-35h) with RANDOM DATA READ (05h-E0h)



PROGRAM FOR INTERNAL DATA MOVE (85h-10h)

The PROGRAM FOR INTERNAL DATA MOVE (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared.

Figure 44: PROGRAM FOR INTERNAL DATA MOVE (85h-10h)

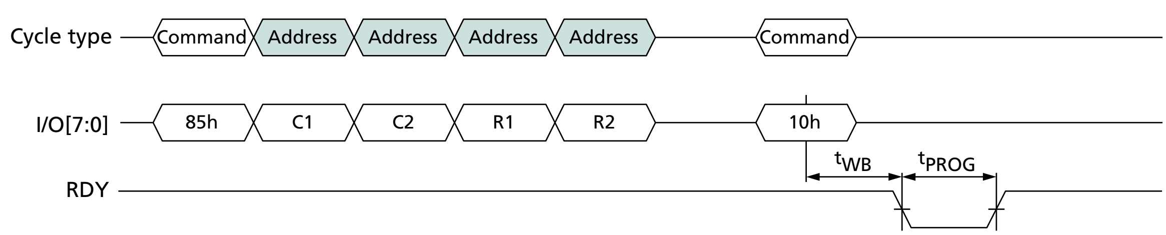
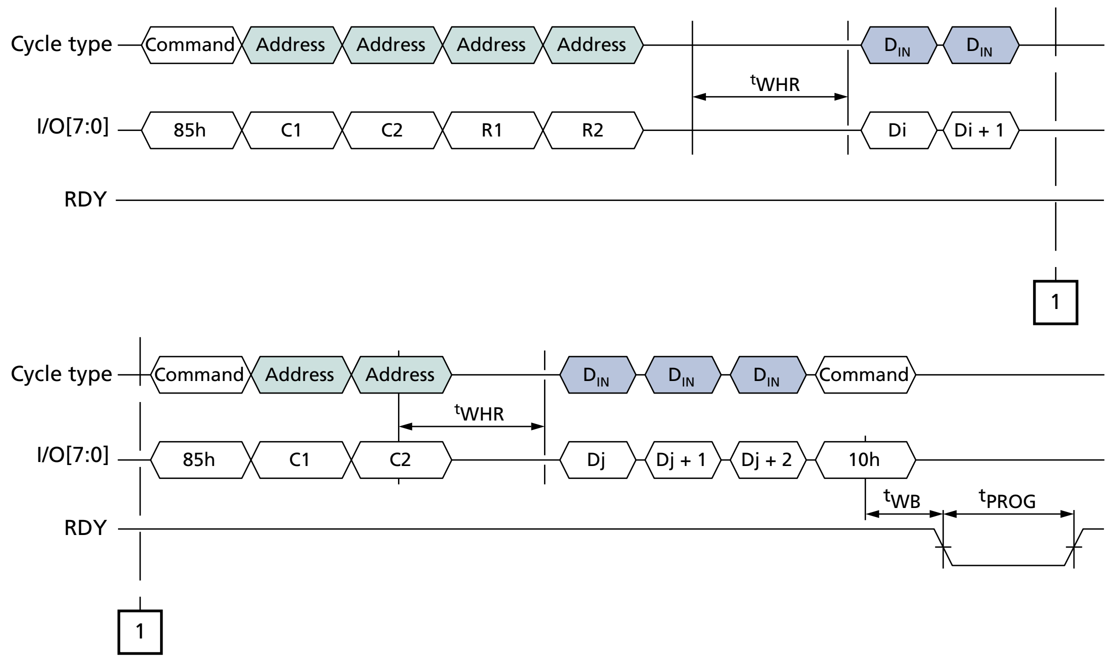


Figure 45: PROGRAM FOR INTERNAL DATA MOVE (85h-10h) with RANDOM DATA INPUT (85h)



Boot Blocks

This device provides up to four securable blocks (0, 1, 2, 3) that can be used to store critical information or boot code. Normal program/erase and cache operations (except PROGRAM PAGE CACHE MODE) are supported on the boot blocks. After the boot blocks are protected, no further program/erase operations can be issued to these blocks. The internal data move and program page cache mode are not supported on boot blocks.

Protecting the Boot Blocks

Protect the boot blocks by entering the boot block protect mode. To set up the device and enter the protect mode, issue the SET FEATURES (EFh) command to 90h (feature address) and write 04h to P1, followed by three cycles of 00h to P2–P4.

To protect the block, issue the 80h command followed by four address cycles (00h-00h-block address-00h), one data cycle of 00h, and then the 10h command. R/B# goes LOW for ^{t}ROH. After the device is protected, it cannot be unprotected.

Block Lock Feature

The block lock feature protects either the entire device or ranges of blocks from being programmed and erased. Using the block lock feature is preferable to using WP# to prevent PROGRAM and ERASE operations.

Block lock is enabled and disabled at power-on through the LOCK pin. At power-on, if LOCK is LOW, all block lock commands are disabled. However if LOCK is HIGH at power-on, the block lock commands are enabled and, by default, all the blocks on the device are protected, or locked, from PROGRAM and ERASE operations, even if WP# is HIGH.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and ERASE operations.

Blocks that are locked can be protected further, or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked until the device is power cycled.

WP# and Block Lock

The following is true when the block lock feature is enabled:

- Holding WP# LOW locks all blocks, provided the blocks are not locked tight.
- If WP# is held LOW to lock blocks, then returned to HIGH, a new UNLOCK command must be issued to unlock blocks.

UNLOCK (23h-24h)

By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. The UNLOCK (23h) command is used to unlock a range of blocks. (Unlocked blocks have no protection and can be programmed or erased.)

The UNLOCK command uses two registers, a lower boundary block address register and an upper boundary block address register, and the invert area bit to determine what range of blocks are unlocked. When the invert area bit = 0, the range of blocks within the lower and upper boundary address registers are unlocked. When the invert area bit = 1, the range of blocks outside the boundaries of the lower and upper boundary address registers are unlocked. The lower boundary block address must be less than the upper boundary block address. The following figures show examples of how the lower and upper boundary address registers work with the invert area bit.

To unlock a range of blocks, issue the UNLOCK (23h) command followed by the appropriate address cycles that indicate the lower boundary block address. Then issue the 24h command followed by the appropriate address cycles that indicate the upper boundary block address. The least significant page address bit, PA0, should be set to 1 if setting the invert area bit; otherwise, it should be 0. The other page address bits should be 0.

Only one range of blocks can be specified in the lower and upper boundary block address registers. If after unlocking a range of blocks the UNLOCK command is again issued, the new block address range determines which blocks are unlocked. The previous unlocked block address range is not retained.

Figure 46: Flash Array Protected: Invert Area Bit = 0

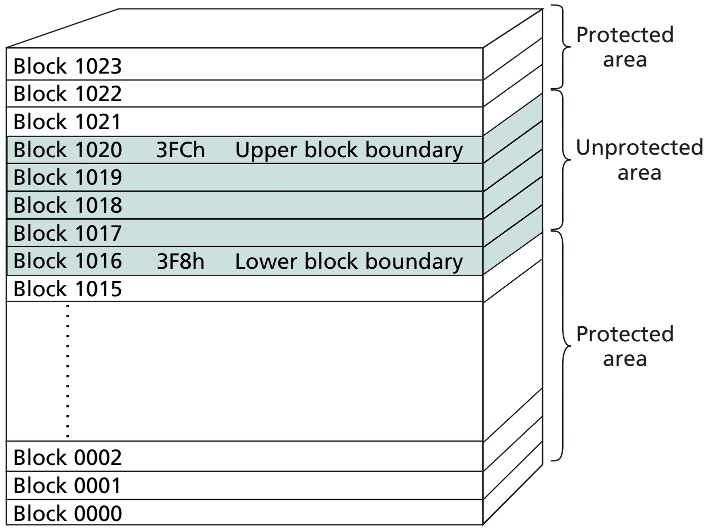


Figure 47: Flash Array Protected: Invert Area Bit = 1

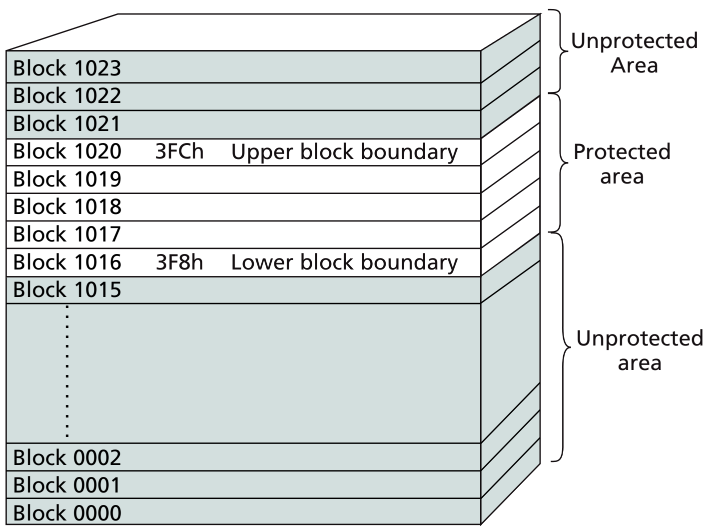
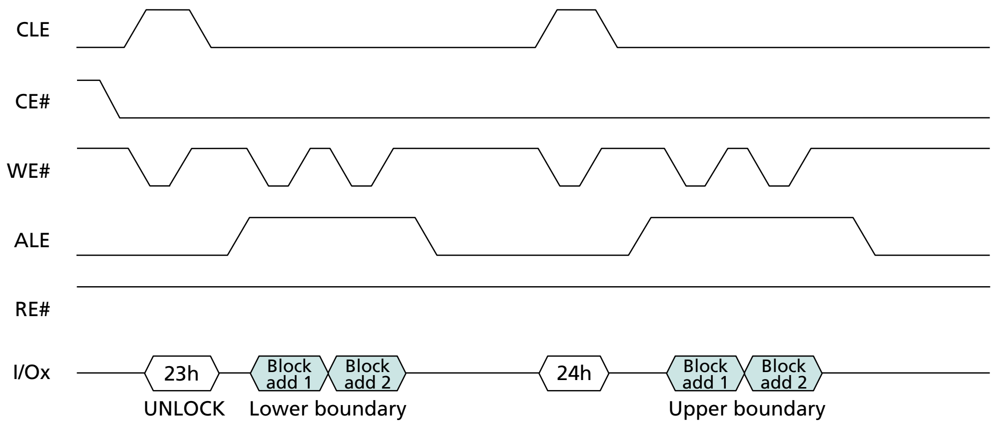


Table 15: Block Lock Address Cycle Assignments

ALE Cycle	I/O[15:8][1]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	BA7	BA6	LOW	LOW	LOW	LOW	LOW	Invert area bit[2]
Second	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8

Notes: 1. I/O[15:8] is applicable only for x16 devices.
2. Invert area bit is applicable for 24h command; it may be LOW or HIGH for 23h command.

Figure 48: UNLOCK Operation



LOCK (2Ah)

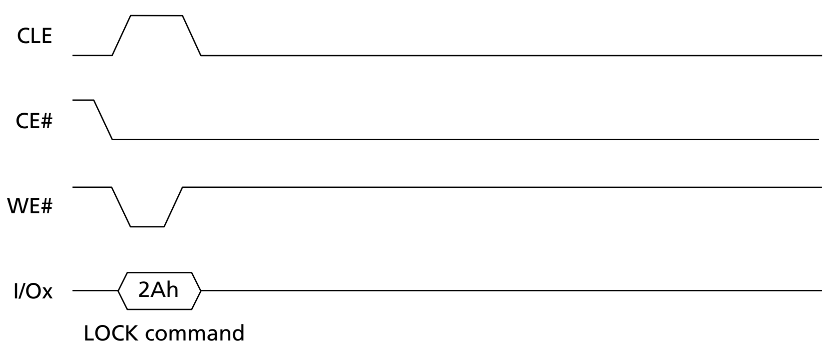
By default at power-on, if LOCK is HIGH, all the blocks are locked and protected from PROGRAM and ERASE operations. If portions of the device are unlocked using the UNLOCK (23h) command, they can be locked again using the LOCK (2Ah) command. The LOCK command locks all of the blocks in the device. Locked blocks are write-protected from PROGRAM and ERASE operations.

To lock all of the blocks in the device, issue the LOCK (2Ah) command.

When a PROGRAM or ERASE operation is issued to a locked block, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. Any READ STATUS command reports bit 7 as 0, indicating that the block is protected.

The LOCK (2Ah) command is disabled if LOCK is LOW at power-on or if the device is locked tight.

Figure 49: LOCK Operation



LOCK TIGHT (2Ch)

The LOCK TIGHT (2Ch) command prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. When this command is issued, the UNLOCK (23h) and LOCK (2Ah) commands are disabled. This provides an additional level of protection against inadvertent PROGRAM and ERASE operations to locked blocks.

To implement LOCK TIGHT tight in all of the locked blocks in the device, verify that WP# is HIGH and then issue the LOCK TIGHT (2Ch) command.

When a PROGRAM or ERASE operation is issued to a locked block that has also been locked tight, R/B# goes LOW for ^{t}LBSY. The PROGRAM or ERASE operation does not complete. The READ STATUS (70h) command reports bit 7 as 0, indicating that the block is protected. PROGRAM and ERASE operations complete successfully to blocks that were not locked at the time the LOCK TIGHT command was issued.

After the LOCK TIGHT command is issued, the command cannot be disabled via a software command. The only ways to disable the lock tight status is to power cycle the device. When the lock tight status is disabled, all of the blocks become locked, the same as if the LOCK (2Ah) command had been issued.

The LOCK TIGHT (2Ch) command is disabled if LOCK is LOW at power-on.

Figure 50: LOCK TIGHT Operation

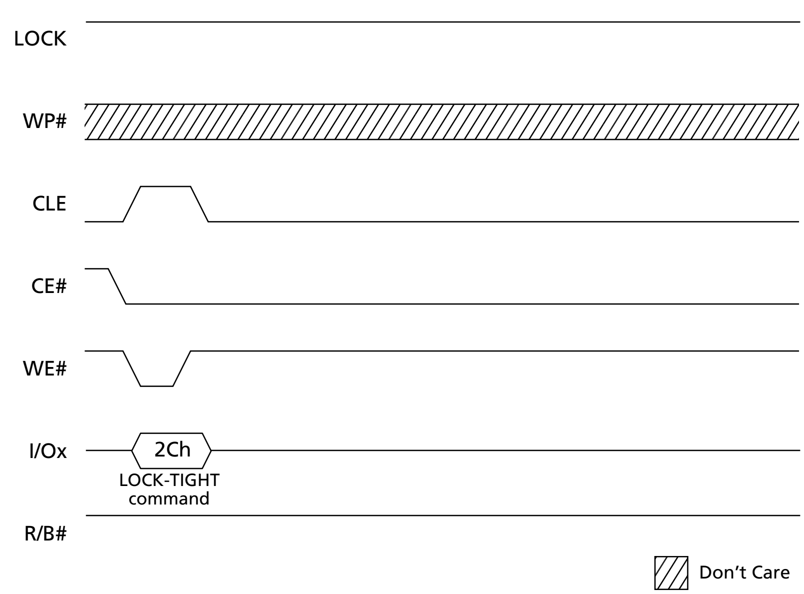
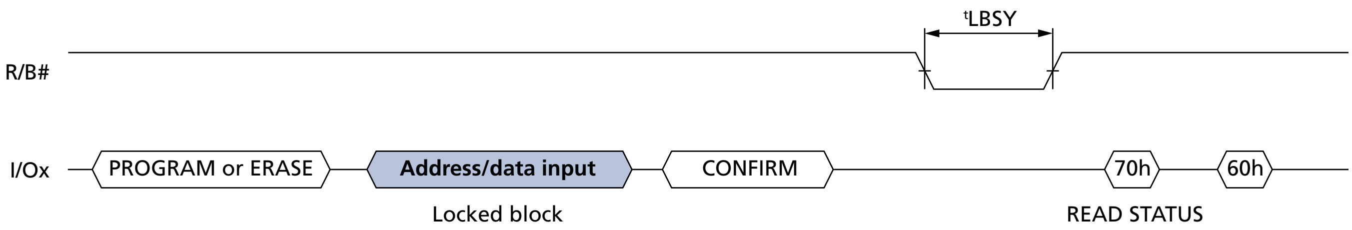


Figure 51: PROGRAM/ERASE Issued to Locked Block



BLOCK LOCK READ STATUS (7Ah)

The BLOCK LOCK READ STATUS (7Ah) command is used to determine the protection status of individual blocks. The address cycles have the same format, as shown below, and the invert area bit should be set LOW. On the falling edge of RE# the I/O pins output the block lock status register, which contains the information on the protection status of the block.

Table 16: Block Lock Status Register Bit Definitions

Block Lock Status Register Definitions	I/O[7:3]	I/O2 (Lock#)	I/O1 (LT#)	I/O0 (LT)
Block is locked tight	X	0	0	1
Block is locked	X	0	1	0
Block is unlocked, and device is locked tight	X	1	0	1
Block is unlocked, and device is not locked tight	X	1	1	0

Figure 52: BLOCK LOCK READ STATUS

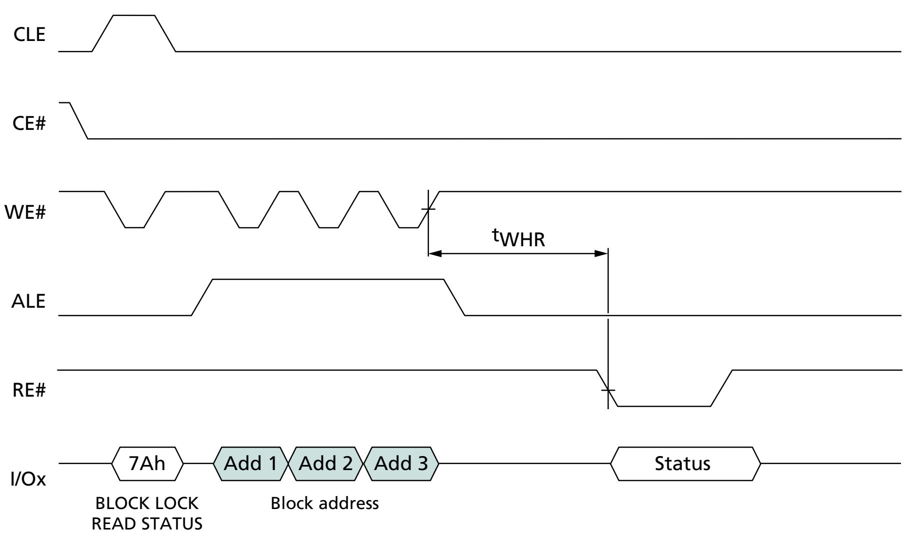
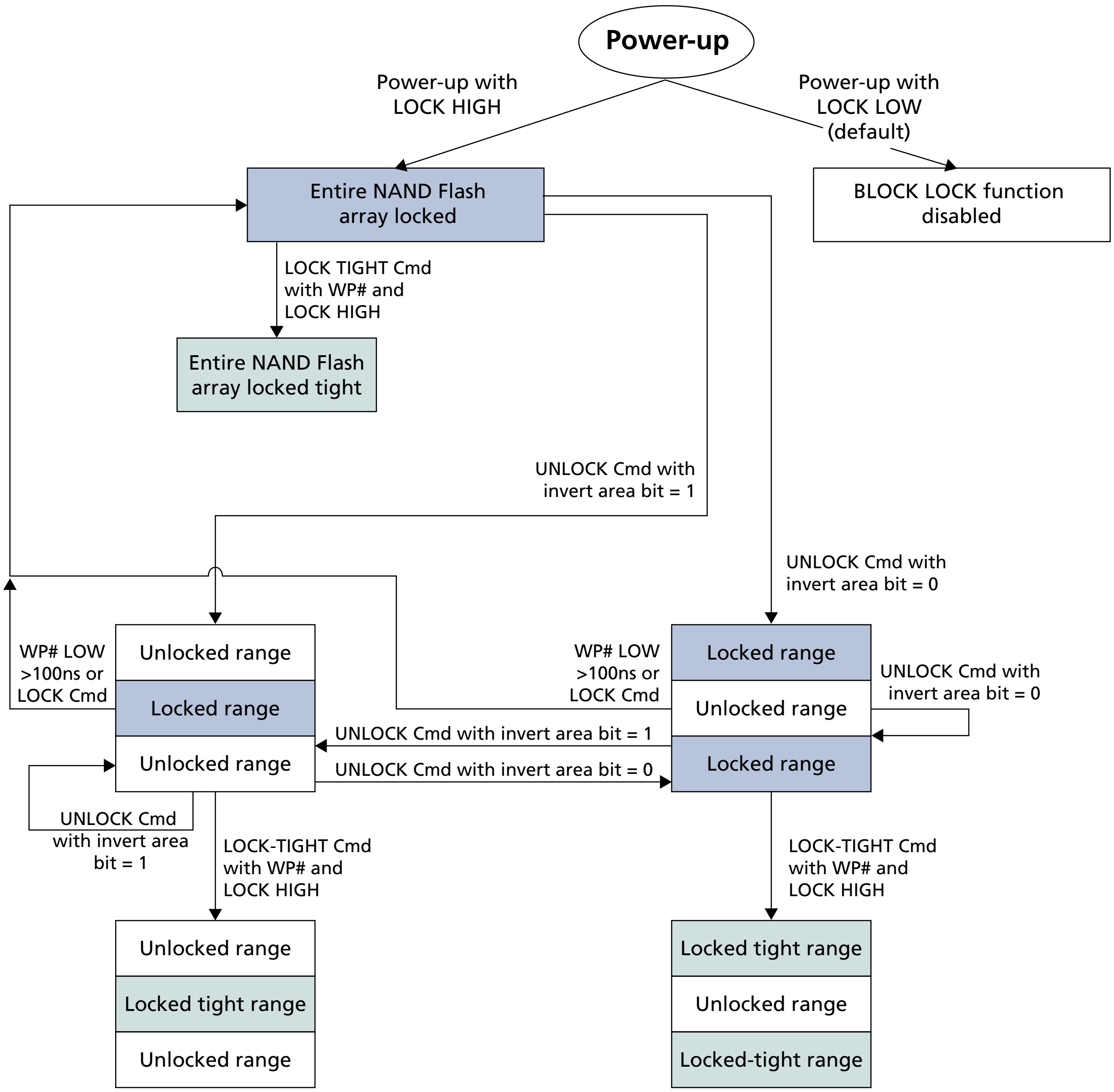


Figure 53: BLOCK LOCK Flowchart



One-Time Programmable Operations (3.3V)

This Micron NAND Flash device offers a protected, one-time programmable (OTP) NAND Flash memory area. Ten full pages (2112 bytes or 1056 words per page) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. The OTP area can be used in a number of ways; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in an unwritten state (each OTP bit is 1). Programming or partial-page programming enables the user to program the OTP area with only 0s. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

Micron provides a unique way to program and verify data before permanently protecting it and preventing future changes. OTP programming and protection are accomplished in two discrete operations. First, the OTP DATA PROGRAM (A0h-10h) command is used to program an entire OTP page in one operation or to perform up to four partial-page programming sequences. Programming can occur on other pages within the OTP area in a similar manner. Second, the OTP area is permanently protected from further programming using the OTP DATA PROTECT (A5h-10h) command. Pages within the OTP area can be read using the OTP DATA READ (AFh-30h) command, whether it is protected or not.

OTP DATA PROGRAM (A0h-10h)

The OTP DATA PROGRAM (A0h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to eight times. There is no ERASE operation for the OTP pages.

The OTP DATA PROGRAM enables programming into an offset of an OTP page, using the two bytes of column address (CA[11:0]). The OTP DATA PROGRAM command will not execute if the OTP area has been protected. If the OTP area is protected, the busy time for the OTP DATA PROGRAM operation is ^{t}OBSY (not ^{t}PROG).

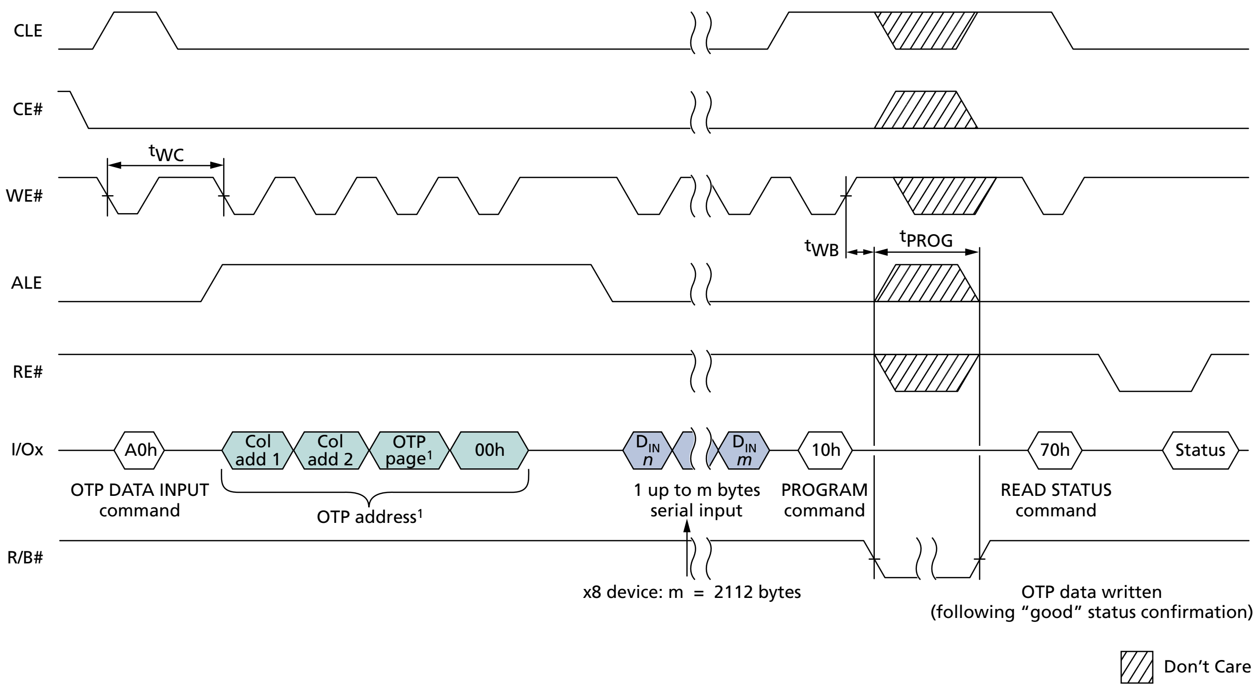
To use the OTP DATA PROGRAM command, issue the A0h command. Issue four address cycles: for the first two address cycles, select the column address; for the other two cycles, select a page in the 02h–0Bh range. Next, write the data using 1–2112 bytes of data (x8 device). After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification. Program verification only detects 1s that are not successfully written to 0s.

RANDOM DATA INPUT (85h) commands are supported during OTP DATA PROGRAM operations only if the OTP area is unprotected.

R/B# goes LOW during the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only command valid during the OTP DATA PROGRAM operation. For this operation, bits 5 and 6 of the status register reflect the state of R/B#. If bit 7 is 0, then the OTP area has been protected; otherwise, it is 1.

When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Register Definition).

Figure 54: OTP DATA PROGRAM Operation



Note: 1. The OTP page must be within the 02h–0Bh range.

OTP DATA PROTECT (A5h-10h)

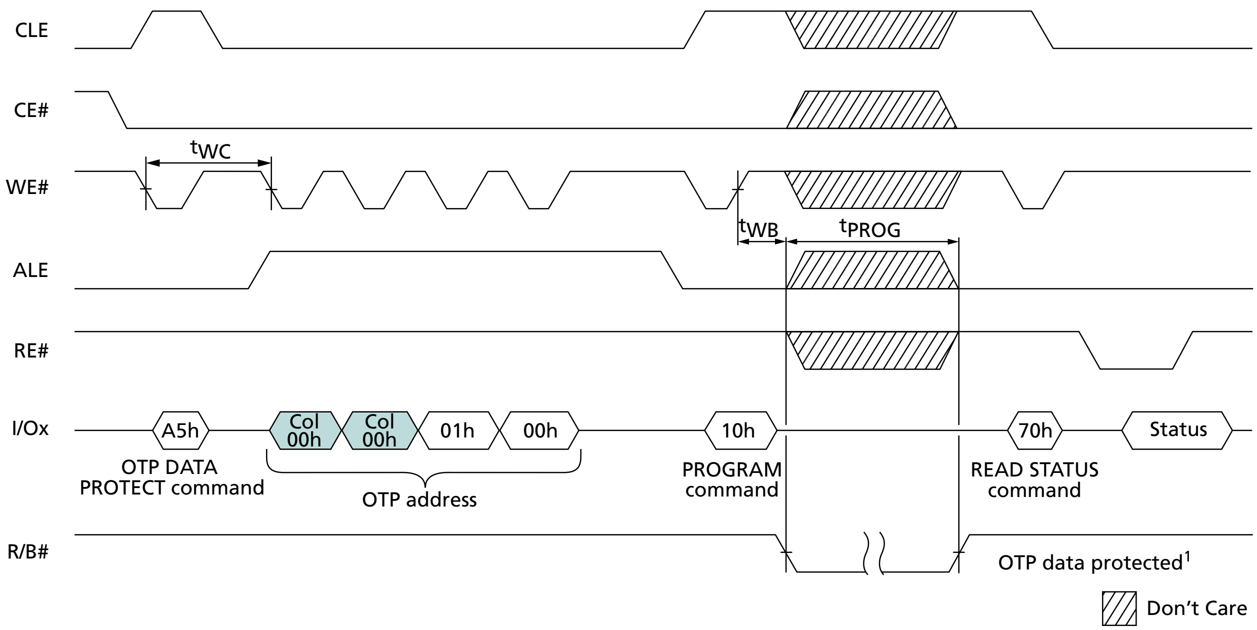
The OTP DATA PROTECT (A5h-10h) command is used to protect all the data in the OTP area. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

To use the OTP DATA PROTECT command, issue the A5h command; then issue the following four address cycles: 00h-00h-01h-00h, followed by the 10h command.

R/B# goes LOW while the OTP area is being protected. The protect command duration is similar to a normal page programming operation, ^{t}PROG. The READ STATUS (70h) command is the only command valid during the OTP DATA PROTECT operation. For this operation, bits 5 and 6 of the status register will reflect the state of R/B#.

When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed (see Status Register Definition).

Figure 55: OTP DATA PROTECT Operation



Note: 1. OTP data is protected following a good status confirmation.

OTP DATA READ (AFh-30h)

The OTP DATA READ (AFh-30h) command is used to read data from a page within the OTP area. An OTP page within the OTP area is available for reading data whether the area is protected or not.

To use the OTP DATA READ command, issue the AFh command; then issue four address cycles: for the first two cycles, select the column address; for the other two cycles, select a page in the range of 02h–0Bh. Then issue the 30h command.

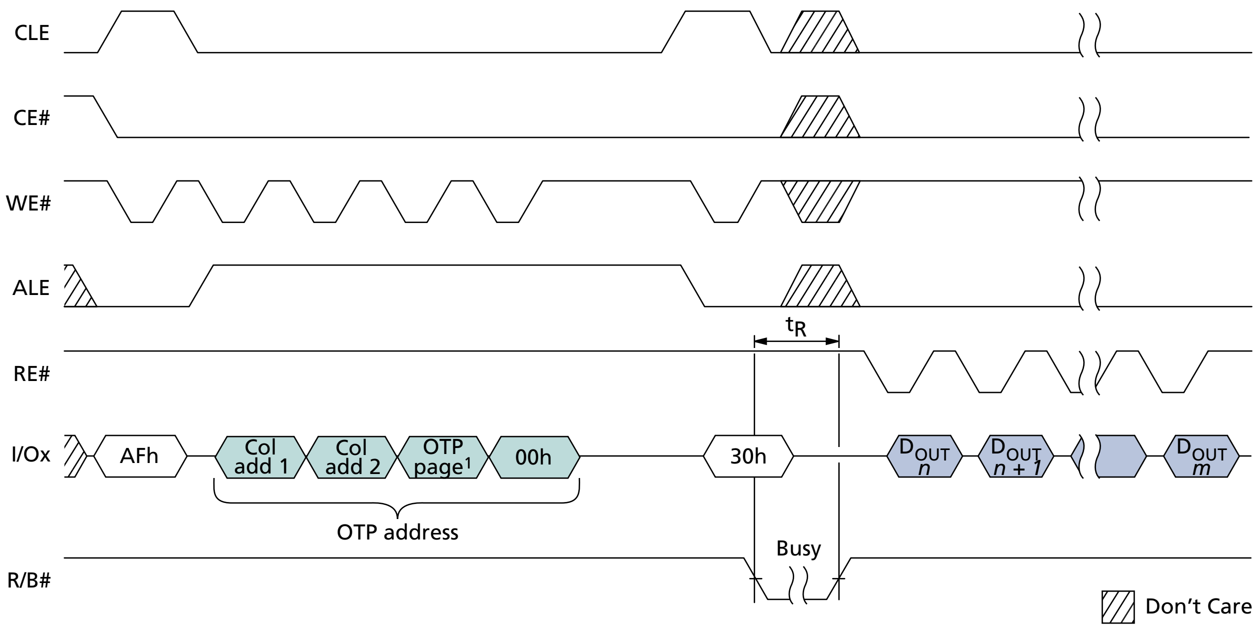
RANDOM DATA READ (05h-E0h) commands are supported during OTP DATA READ operations.

R/B# goes LOW (^{t}R) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command and the RESET (FFh) command are the only commands valid during the OTP DATA READ operation. For this operation, bits 5 and 6 of the status register reflect the state of R/B#. For details, refer to see Status Register Definition.

Normal READ operation timings apply to OTP read accesses (see the figure below). Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

Note that if OTP DATA READ is followed by PAGE READ CACHE MODE, a RESET (FFh) must be issued prior to issuing the PAGE READ CACHE MODE command. The maximum RESET time will not exceed 5µs.

Figure 56: OTP DATA READ Operation



Note: 1. The OTP page must be within the 02h–0Bh range.

One-Time Programmable Operations (1.8V)

This Micron NAND Flash device offers a protected, one-time programmable (OTP) NAND Flash memory area. Thirty full pages (2112 bytes per page) of OTP data is available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. The OTP area can be used in a number of ways; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in an unwritten state (all bits are 1s). Programming or partial-page programming enables the user to program the OTP area with only 0s. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

Micron provides a unique way to program and verify data before permanently protecting it and preventing future changes. The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURE (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2–P4.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h–1Eh. To program an OTP page, issue the PROGRAM PAGE (80h-10h) command. The pages must be programmed in ascending order. To read an OTP page, issue the PAGE READ (00h-30h) command.

The OTP area can be protected page by page using the OTP protect mode. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to feature address 90h and write 03h to P1, followed by three cycles of 00h to P2–P4.

To protect a page in the OTP area, issue the 80h command, followed by four address cycles (00h-00h-page address-00h), followed by one data cycle of 00h, followed by the 10h command. R/B# goes LOW for ^{t}PROG.

To determine whether the device is busy during an OTP operation, monitor R/B# or use the READ STATUS (70h) command.

To exit OTP operation or protect mode, write 00h to P1 at feature address 90h.

OTP DATA PROGRAM (80h-10h)

The OTP DATA PROGRAM (80h-10h) command is used to write data to the pages within the OTP area. An entire page can be programmed at one time, or a page can be partially programmed up to eight times. Only the OTP area allows up to eight partial-page programs. The rest of the blocks support four partial-page programs. There is no ERASE operation for OTP pages.

PROGRAM PAGE enables programming into an offset of an OTP page, using the two bytes of column address (CA[12:0]). The command is compatible with the RANDOM DATA INPUT (85h) command. The PROGRAM PAGE command will not execute if the OTP area has been protected.

To use the PROGRAM PAGE command, issue the 80h command. Issue four address cycles: for the first two address cycles, select the column address; for the other two cycles, select a page in the range of 02h-00h through 1Eh-00h. Next, write 1–2112 bytes of data. After data input is complete, issue the 10h command. The internal control logic automatically executes the proper programming algorithm and controls the necessary timing for programming and verification.

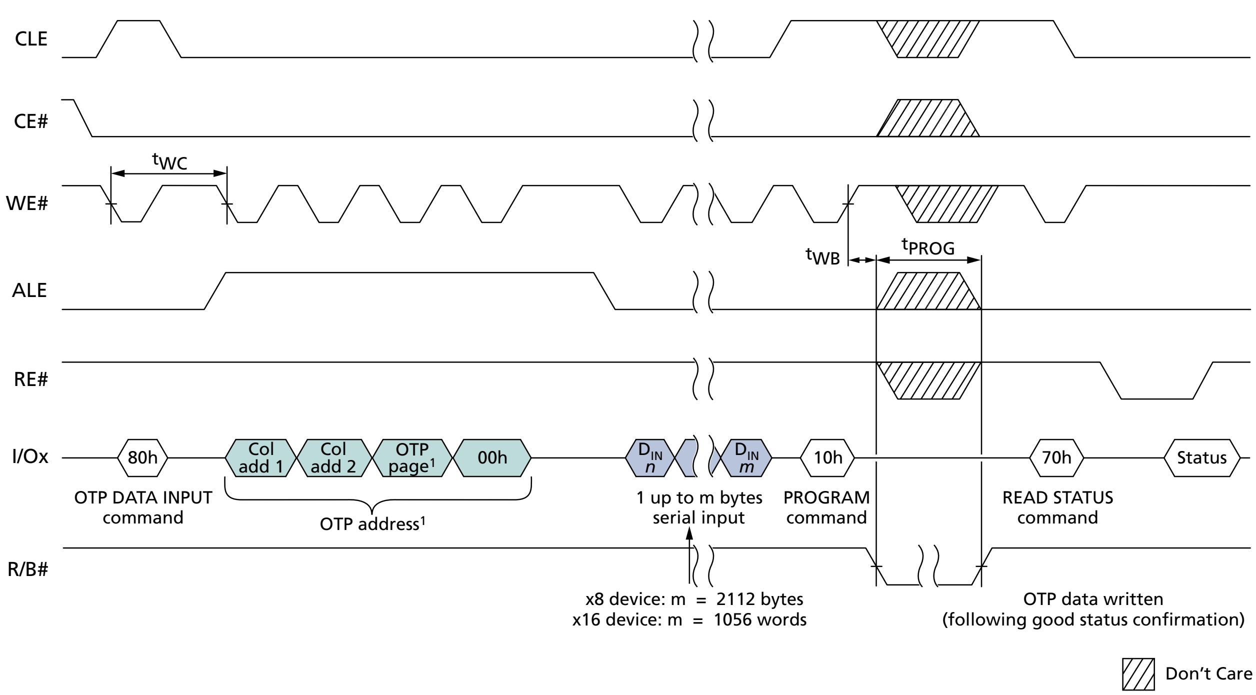
R/B# goes LOW for the duration of the array programming time (^{t}PROG). The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#. When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed. Each OTP page can only be programmed one time.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, R/B# will go LOW for ^{t}OBSY.

RANDOM DATA INPUT (85h)

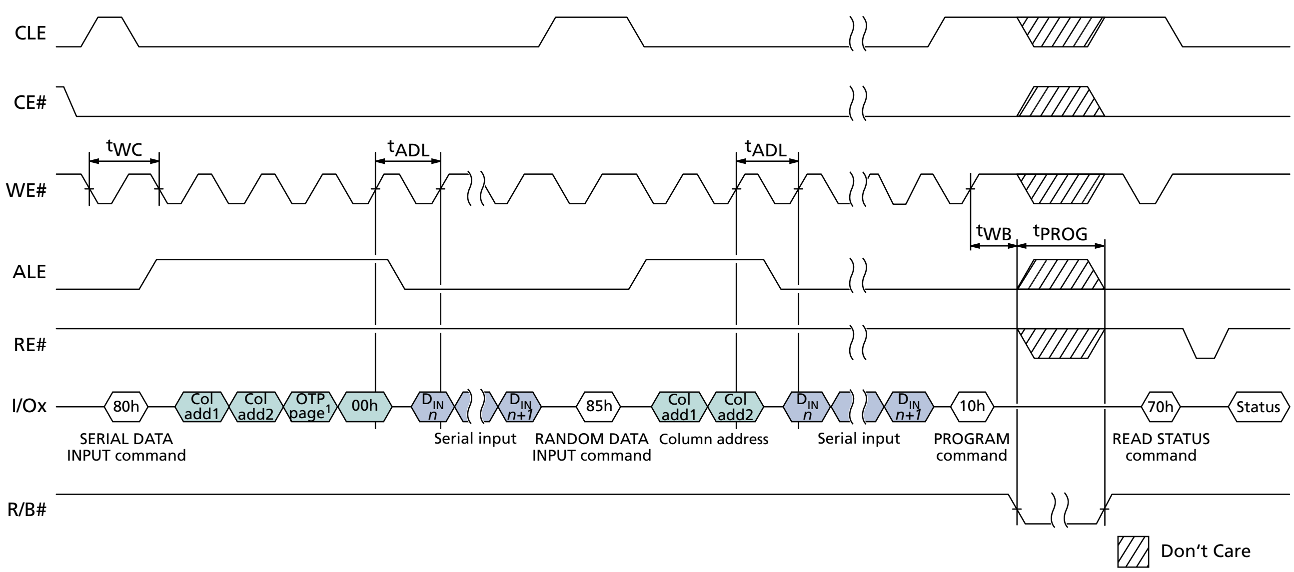
After the initial OTP data set is input, additional data can be written to a new column address with the RANDOM DATA INPUT (85h) command. The RANDOM DATA INPUT command can be used any number of times in the same page prior to the OTP PAGE WRITE (10h) command being issued.

Figure 57: OTP DATA PROGRAM Operation (after entering OTP operation mode)



Note: 1. The OTP page must be within the 02h–1Eh range.

Figure 58: OTP DATA PROGRAM with RANDOM DATA INPUT (after entering OTP operation mode)



Note: 1. The OTP page must be within the 02h–1Eh range.

OTP DATA PROTECT (80h-10h)

The OTP area is protected on a page basis. To protect a page or all pages, set the device to OTP protect mode, then issue the PROGRAM PAGE (80h-10h) command and write page address to protect a specific page. To set the device to OTP protect mode, issue the SET FEATURE (EFh) command to feature address 90h and write 03h to P1, followed by three cycles of 00h to P2–P4.

After the data is protected, it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

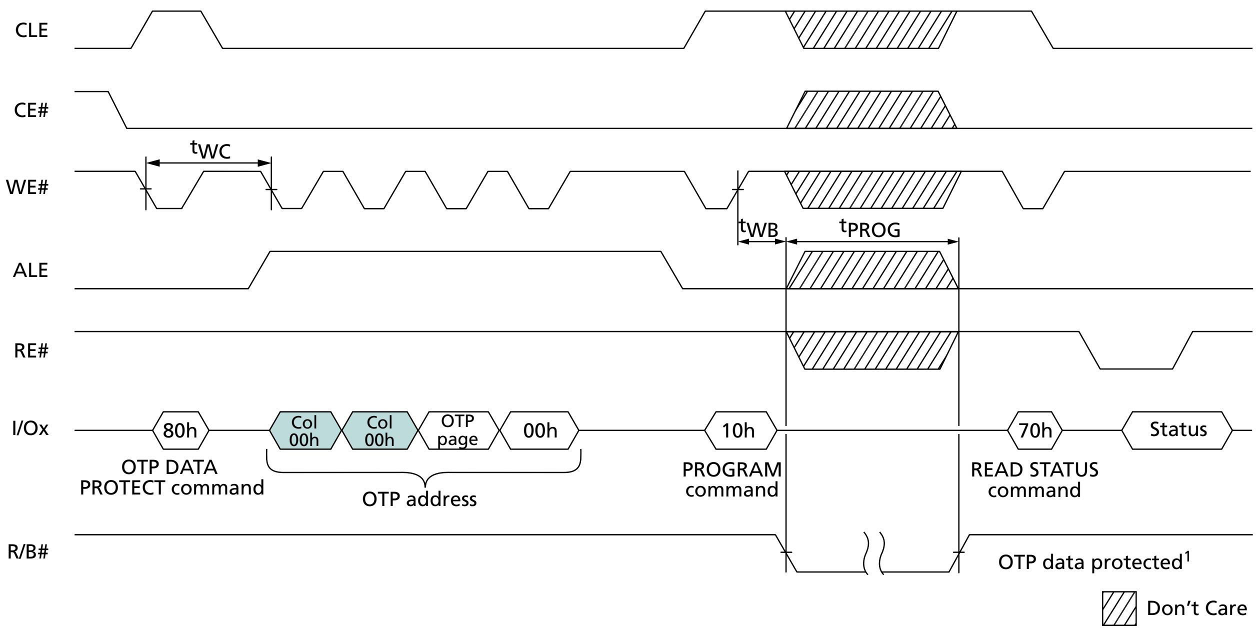
To use the PROGRAM PAGE command to protect the OTP area, issue the 80h command; then issue the following four address cycles: 00h-00h-page address-00h and write 00h data, followed by the 10h command.

If an OTP DATA PROGRAM command is issued after the OTP area has been protected, R/B# will go LOW for ^{t}OBSY.

The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#.

When the device is ready, read bit 0 of the status register to determine whether the operation passed or failed.

Figure 59: OTP DATA PROTECT Operation (after entering OTP protect mode)



Note: 1. OTP data is protected following a good status confirmation.

OTP DATA READ (00h-30h)

To read data from the OTP area, set the device to OTP operation mode, then issue the PAGE READ (00h-30h) command. Data can be read from OTP pages within the OTP area whether the area is protected or not.

To use the PAGE READ command for reading data from the OTP area, issue the 00h command; then issue four address cycles: for the first two cycles, select the column address; for the other two cycles, select a page in the range of 02h-00h-00h through 1Eh-00h-00h. Then issue the 30h command. The PAGE READ CACHE MODE command is not supported on OTP pages.

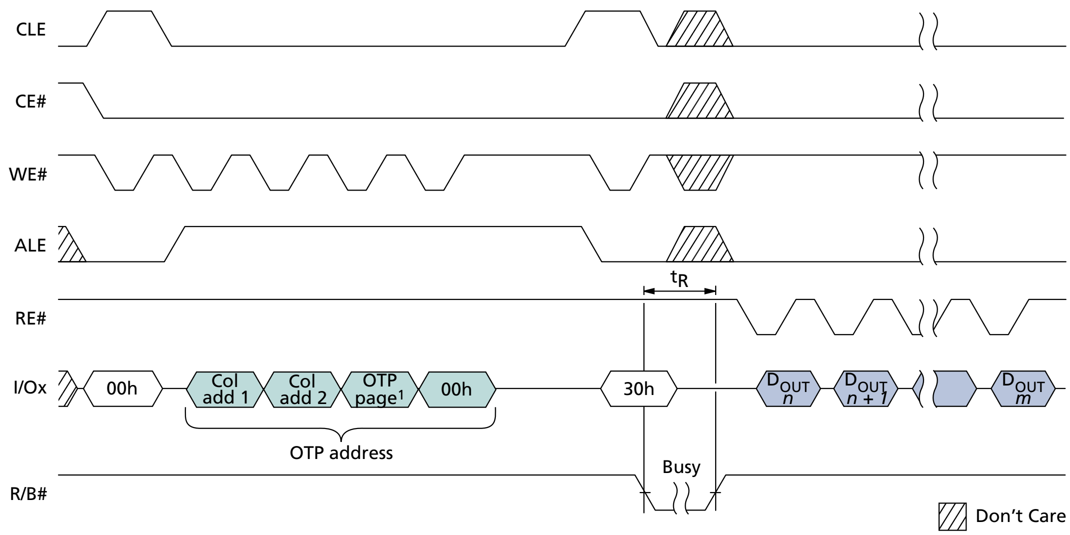
R/B# goes LOW (^tR) while the data is moved from the OTP page to the data register. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. Bit 5 of the status register reflects the state of R/B#.

Normal READ operation timings apply to OTP read accesses. Additional pages within the OTP area can be selected by repeating the OTP DATA READ command.

The PAGE READ command is compatible with the RANDOM DATA OUTPUT (05h-E0h) command.

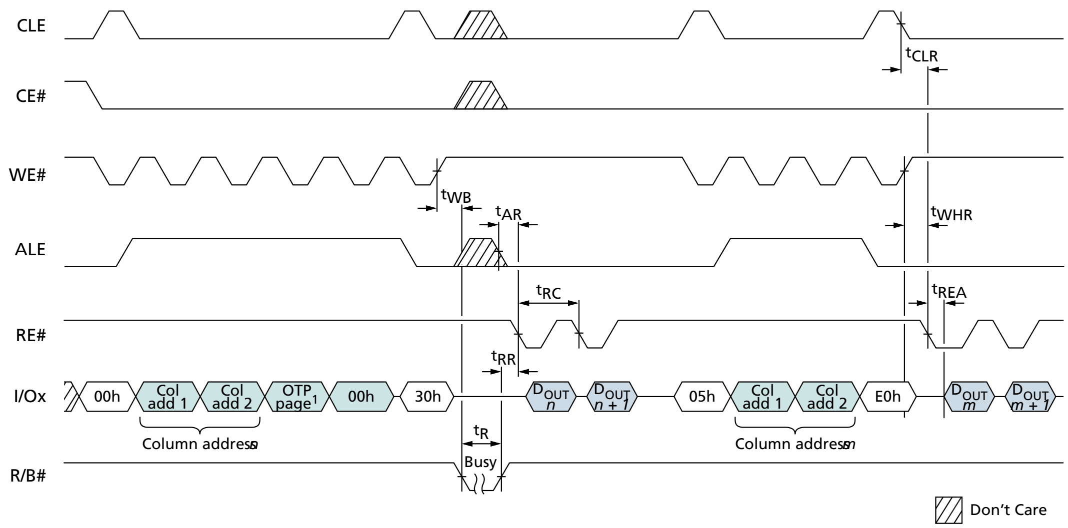
Only data on the current page can be read. Pulsing the RE# pin outputs data sequentially.

Figure 60: OTP DATA READ Operation



Note: 1. The OTP page must be within the 02h–1Eh range.

Figure 61: OTP DATA READ with RANDOM DATA READ Operation



Note: 1. The OTP page must be within the range 02h–1Eh.

WRITE PROTECT Operation

The PROGRAM and ERASE commands can be enabled and disabled using the WP# pin. The following six figures illustrate the setup time (^{t}WW) required from WP# toggling until a PROGRAM or ERASE command is latched into the command register. After command cycle 1 is latched, the WP# pin must not be toggled until the command is complete and the device is ready (status register bit 5 is 1).

Figure 62: ERASE Enable

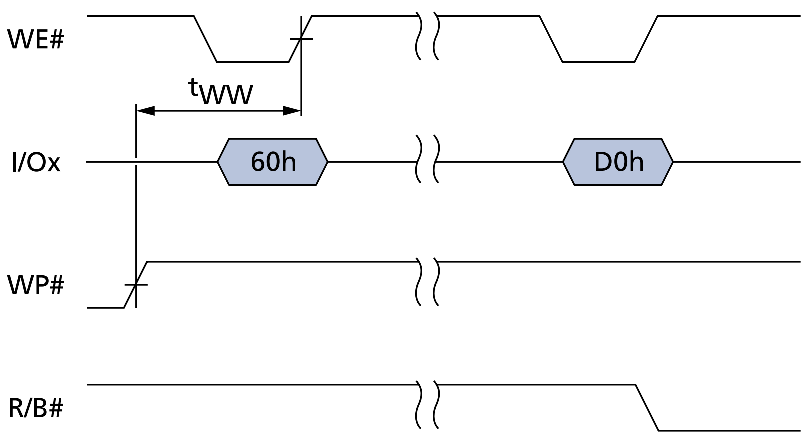


Figure 63: ERASE Disable

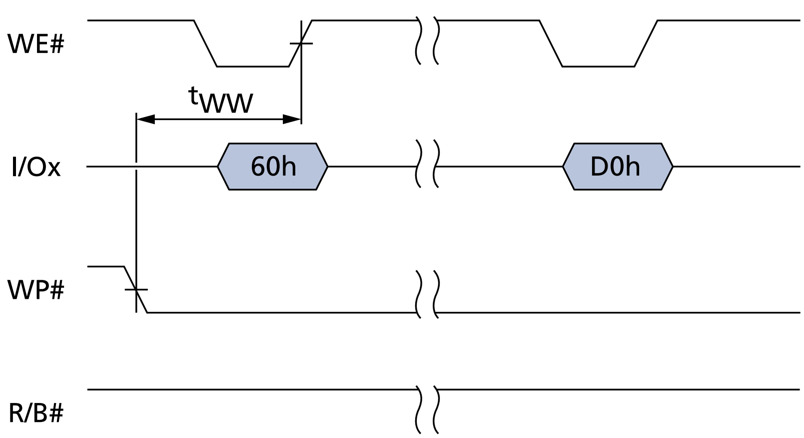


Figure 64: PROGRAM Enable

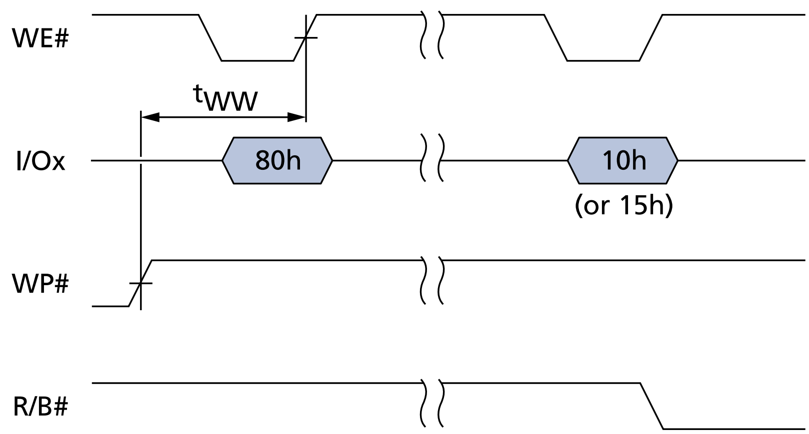


Figure 65: PROGRAM Disable

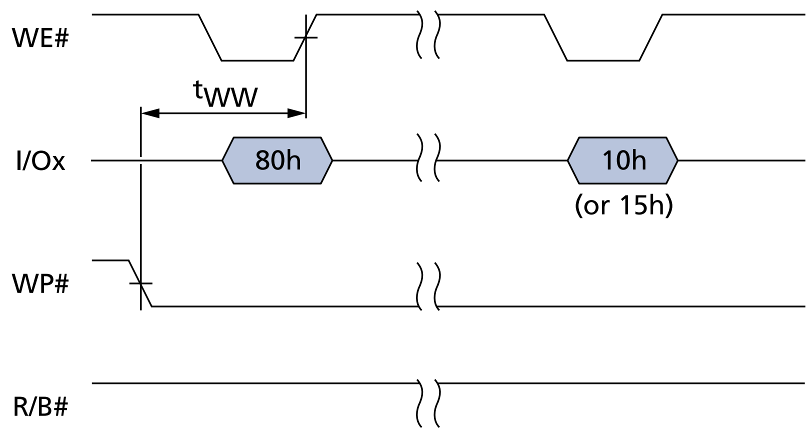


Figure 66: PROGRAM for INTERNAL DATA MOVE Enable

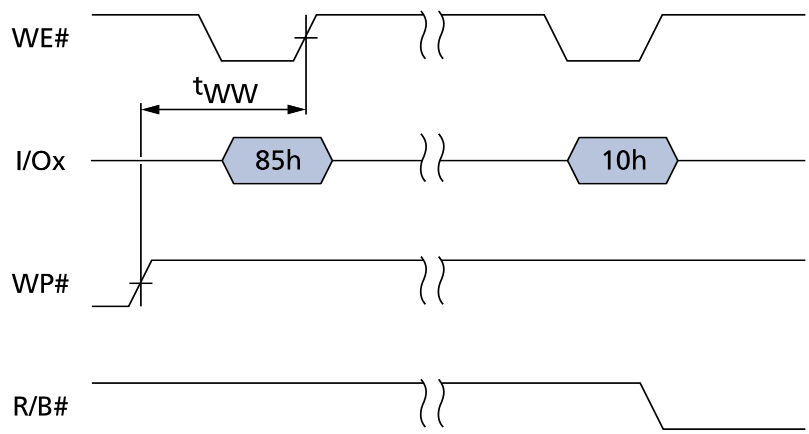
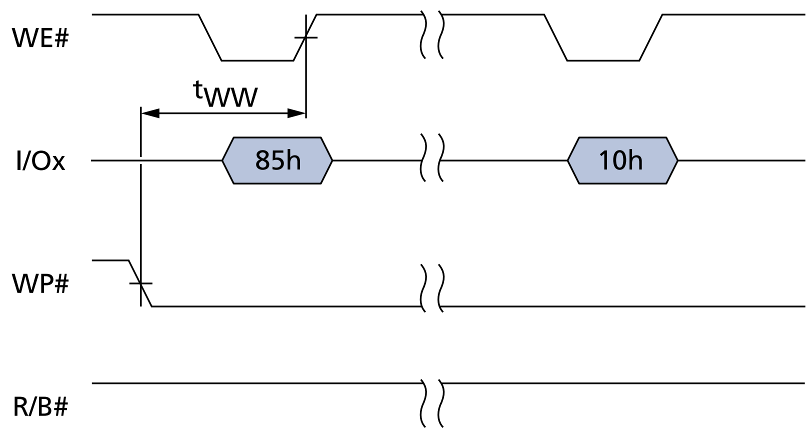


Figure 67: PROGRAM for INTERNAL DATA MOVE Disable



Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

  The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Blocks 0-7 (block address 00h-40h) guaranteed to be valid with ECC when shipped from factory (3.3V only). Blocks 0-3 (block address 00h-40h) guaranteed to be valid with ECC when shipped from factory (1.8V only).

Table 17: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	1004
Total available blocks per LUN	1024
First spare area location	x8: byte 2048 x16: word 1024
Bad-block mark	x8: 00h x16: 0000h
Minimum required ECC	1-bit ECC per 528 bytes of data

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 18: Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}

Parameter/Condition		Symbol	Min	Max	Unit
Voltage Input	3.3V	V_{IN}	–0.6	+4.6	V
	1.8V		–0.6	+2.4	V
V_{CC} supply voltage	3.3V	V_{CC}	–0.6	+4.6	V
	1.8V		–0.6	+2.4	V
Storage temperature		T_{STG}	–65	+150	°C
Short circuit output current, I/Os		–	–	5	mA

Table 19: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Industrial		–40	–	+85	°C
V_{CC} supply voltage	3.3V	V_{CC}	2.7	3.3	3.6	V
	1.8V		1.65	1.8	1.95	V
Ground supply voltage		V_{SS}	0	0	0	V

Table 20: Valid Blocks

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	3.3V/1.8V	1004	1024	blocks	1, 2

Notes:
1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Blocks 0–7 (3.3V) and blocks 0–3 (1.8V) are guaranteed to be valid with ECC when shipped from the factory.

Table 21: Capacitance

Description	Symbol	Max	Unit	Notes
Input capacitance	C_{IN}	10	pF	1, 2
Input/output capacitance (I/O)	C_{IO}	10	pF	1, 2

Notes:
1. These parameters are verified in device characterization and are not 100% tested.
2. Test conditions: T_C = 25°C; f = 1 MHz; V_{IN} = 0V.

Table 22: Test Conditions

Parameter		Value	Notes
Input pulse levels		0.0V to V_{CC}	
Input rise and fall times		5ns	
Input and output timing levels		$V_{CC}/2$	
Output load	3.3V	1 TTL GATE and CL = 30pF	1
	1.8V	1 TTL GATE and CL = 30pF	1

Note:
1. These parameters are verified in device characterization and are not 100% tested.

Electrical Specifications – AC Characteristics and Operating Conditions

Table 23: AC Characteristics: Command, Data, and Address Input (3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	70	–	ns	1
ALE hold time	^{t}ALH	5	–	ns	
ALE to setup time	^{t}ALS	10	–	ns	
CE# hold time	^{t}CH	5	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	10	–	ns	
CE# setup time	^{t}CS	15	–	ns	
DATA hold time	^{t}DH	5	–	ns	
DATA setup time	^{t}DS	10	–	ns	
WRITE cycle time	^{t}WC	25	–	ns	
WE# pulse width HIGH	^{t}WH	10	–	ns	
WE# pulse width	^{t}WP	12	–	ns	
WP# setup time	^{t}WW	100	–	ns	

Note: 1. Timing for ^{t}ADL begins in the address cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

Table 24: AC Characteristics: Command, Data, and Address Input (1.8V)

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	^{t}ADL	100	–	ns	1
ALE hold time	^{t}ALH	10	–	ns	
ALE setup time	^{t}ALS	15	–	ns	
CE# hold time	^{t}CH	10	–	ns	
CLE hold time	^{t}CLH	5	–	ns	
CLE setup time	^{t}CLS	15	–	ns	
CE# setup time	^{t}CS	25	–	ns	
Data hold time	^{t}DH	5	–	ns	
Data setup time	^{t}DS	15	–	ns	
WRITE cycle time	^{t}WC	35	–	ns	
WE# pulse width HIGH	^{t}WH	15	–	ns	
WE# pulse width	^{t}WP	17	–	ns	
WP# setup time	^{t}WW	100	–	ns	

Note: 1. Timing for ^{t}ADL begins in the address cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

Table 25: AC Characteristics: Normal Operation (3.3V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	25	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	30	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	25	–	ns	
RE# access time	^{t}REA	–	20	ns	
RE# HIGH hold time	^{t}REH	10	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	2
RE# LOW to output hold	^{t}RLOH	5	–	ns	
RE# pulse width	^{t}RP	12	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	60	–	ns	

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will be busy for a maximum of 1ms. Thereafter, the device will be busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Table 26: AC Characteristics: Normal Operation (1.8V)

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	^{t}AR	10	–	ns	
CE# access time	^{t}CEA	–	30	ns	
CE# HIGH to output High-Z	^{t}CHZ	–	45	ns	2
CLE to RE# delay	^{t}CLR	10	–	ns	
CE# HIGH to output hold	^{t}COH	15	–	ns	
Output High-Z to RE# LOW	^{t}IR	0	–	ns	
READ cycle time	^{t}RC	35	–	ns	
RE# access time	^{t}REA	–	25	ns	
RE# HIGH hold time	^{t}REH	15	–	ns	
RE# HIGH to output hold	^{t}RHOH	15	–	ns	
RE# HIGH to WE# LOW	^{t}RHW	100	–	ns	
RE# HIGH to output High-Z	^{t}RHZ	–	100	ns	2
RE# pulse width	^{t}RP	17	–	ns	
Ready to RE# LOW	^{t}RR	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	^{t}RST	–	5/10/500	µs	3
WE# HIGH to busy	^{t}WB	–	100	ns	4
WE# HIGH to RE# LOW	^{t}WHR	80	–	ns	

Notes:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100% tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will be busy for a maximum of 1ms. Thereafter, the device will be busy for maximum 5µs.
4. Do not issue a new command during ^{t}WB, even if R/B# is ready.

Electrical Specifications – DC Characteristics and Operating Conditions

Table 27: DC Characteristics and Operating Conditions (3.3V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$^{t}RC = {}^{t}RC$ (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1_A}	–	25	35	mA	
PROGRAM current	–	I_{CC2_A}	–	25	35	mA	
ERASE current	–	I_{CC3_A}	–	25	35	mA	
I/O burst read current	–	I_{CC4R_A}	–	25	35	mA	
I/O burst write current	–	I_{CC4W_A}	–	25	35	mA	
Bus idle current	–	I_{CC5_A}	–	2	3	mA	
Standby current (TTL)	CE# = V_{IH}; WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; WP# = 0V/V_{CC}	I_{SB_A}	–	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10	mA	1
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –400µA	V_{OH}	0.67 x V_{CC}	–	–	V	2
Output low voltage	I_{OL} = 2.1mA	V_{OL}	–	–	0.4	V	2
Output low current	V_{OL} = 0.4V	I_{OL} (R/B#)	8	10	–	mA	3

Notes:
1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches $V_{CC,min}$.
2. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.
3. I_{OL} (R/B#) may need to be relaxed if R/B# pull-down strength is not set to full.

Table 28: DC Characteristics and Operating Conditions (1.8V)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	^tRC = ^tRC (MIN); CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1_A}	–	10	20	mA	
PROGRAM current	–	I_{CC2_A}	–	10	20	mA	
ERASE current	–	I_{CC3_A}	–	10	20	mA	
I/O burst read current	–	I_{CC4R_A}	–	10	20	mA	
I/O burst write current	–	I_{CC4W_A}	–	10	20	mA	
Bus idle current	–	I_{CC5_A}	–	2	3	mA	
Stanbdy current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	I_{SB_A}	–	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10	mA	1
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[7:0], I/O[15:0], CE#, CLE, ALE, WE#, RE#, WP#, LOCK	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} - 0.1	–	–	V	2
Output low voltage	I_{OL} = +100µA	V_{OL}	–	–	0.1	V	2
Output low current	V_{OL} = 0.4V	I_{OL} (R/B#)	3	4	–	mA	3

Notes:
1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches $V_{CC,min}$.
2. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.
3. I_{OL} (R/B#) may need to be relaxed if R/B# pull-down strength is not set to full.

Electrical Specifications – Program/Erase Characteristics

Table 29: PROGRAM/ERASE Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	4	Cycles	1
BLOCK ERASE operation time	^{t}BERS	0.5	2	ms	
Busy time for PROGRAM CACHE operation (3.3V)	^{t}CBSY	3	700	µs	2
Busy time for PROGRAM CACHE operation (1.8V)	^{t}CBSY	3	700	µs	2
Busy time for SET FEATURES and GET FEATURES operations (3.3V)	^{t}FEAT	–	1	µs	
Busy time for SET FEATURES and GET FEATURES operations (1.8V)	^{t}FEAT	–	1	µs	
Busy time for PROGRAM/ERASE on locked block	^{t}LBSY	–	3	µs	
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	–	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	30	µs	
PAGE PROGRAM operation time (1.8V)	^{t}PROG	250	700	µs	
PAGE PROGRAM operation time (3.3V)	^{t}PROG	250	700	µs	
Data transfer from Flash array to data register	^{t}R	–	25	µs	
Busy time for READ CACHE operation	^{t}RCBSY	3	25	µs	

Notes:
1. Four total partial page programs to the same page.
2. ^{t}CBSY MAX time depends on timing between internal program completion and data-in.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

Asynchronous Interface Timing Diagrams

Figure 68: RESET Operation

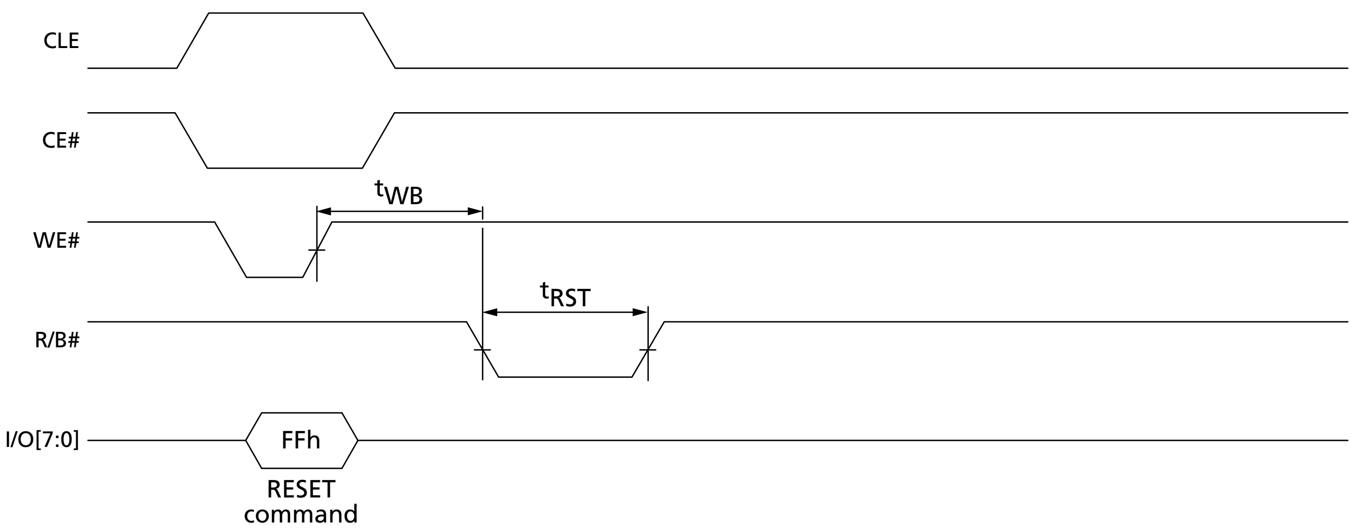


Figure 69: READ STATUS Cycle

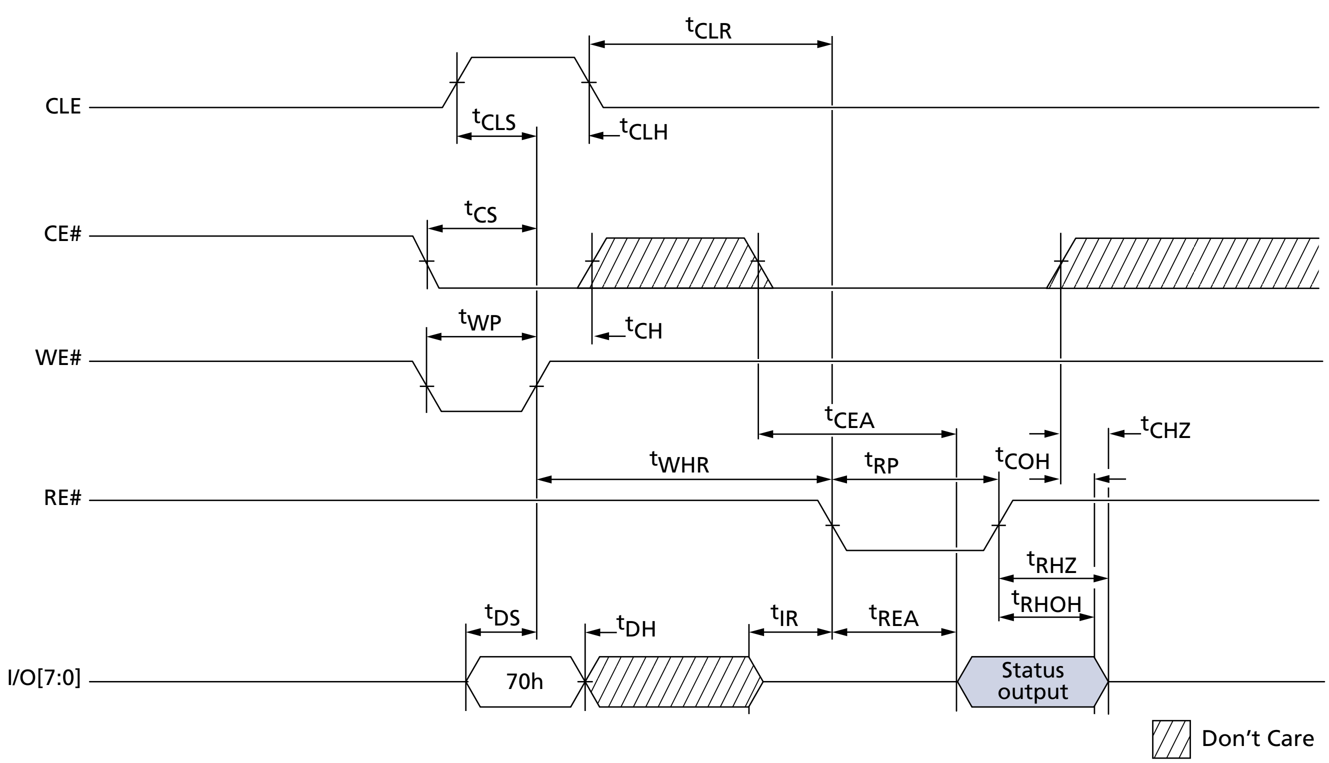


Figure 70: READ PARAMETER PAGE

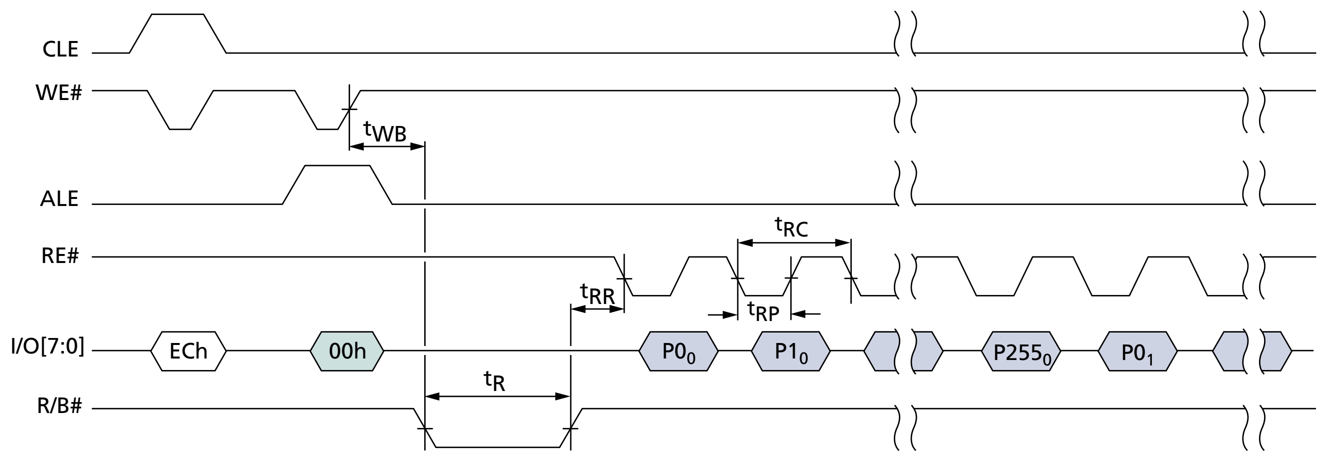


Figure 71: READ PAGE

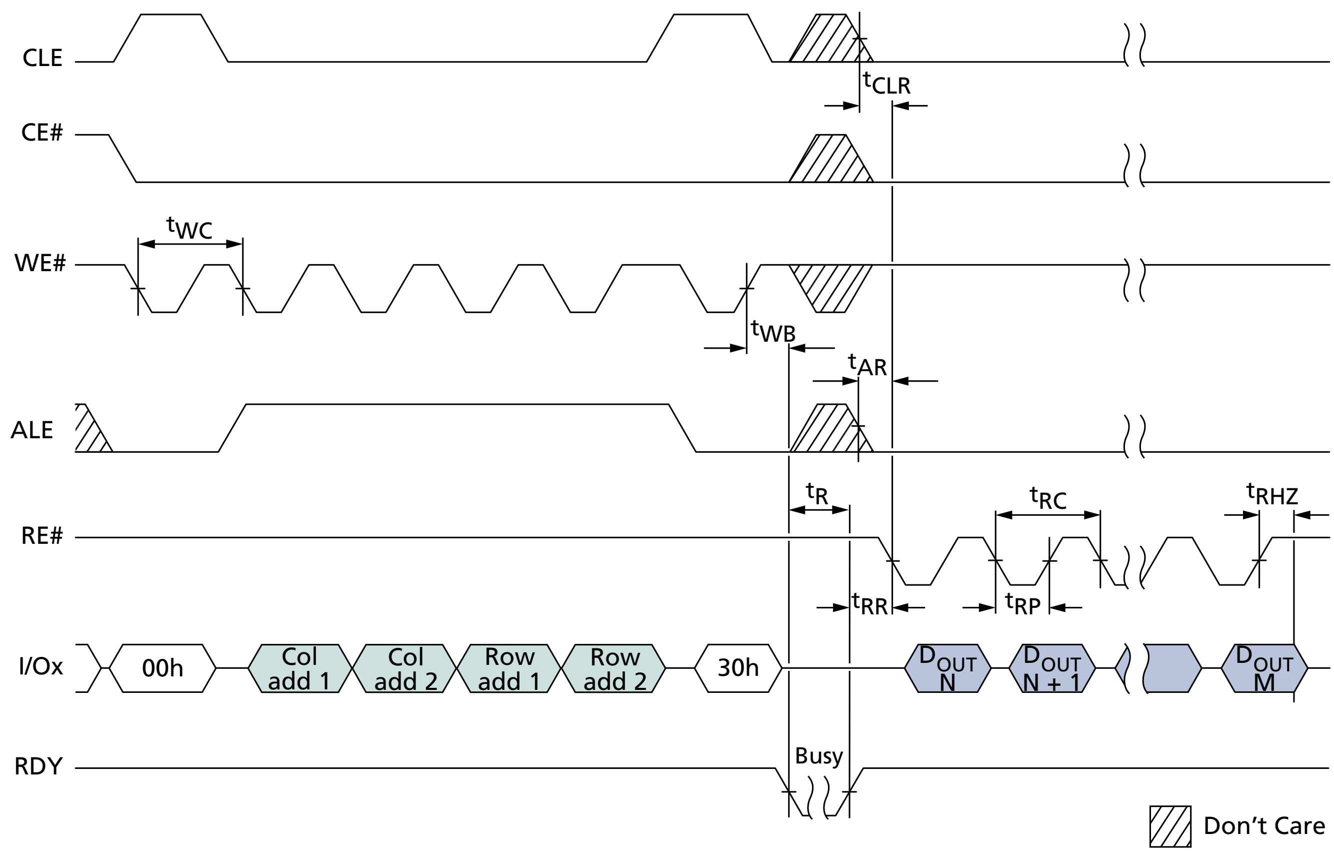


Figure 72: READ PAGE Operation with CE# "Don't Care"

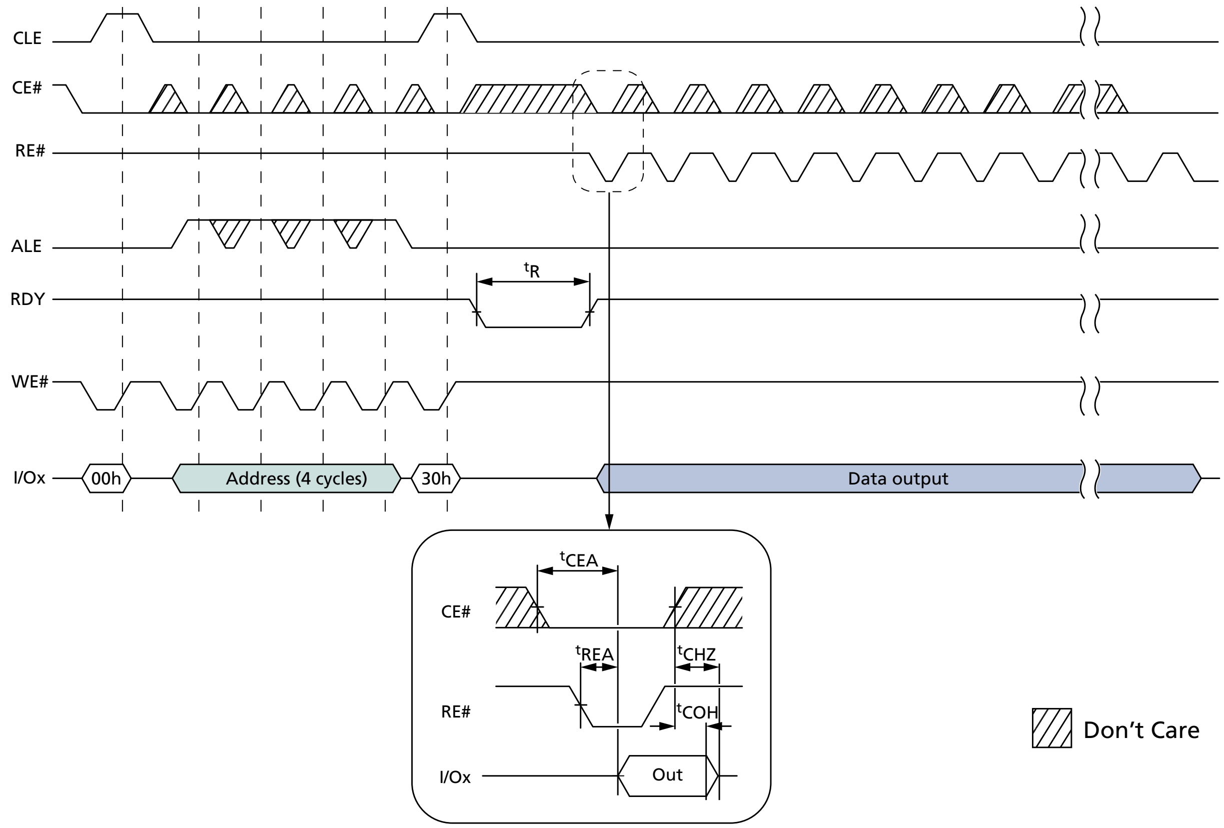


Figure 73: RANDOM DATA READ

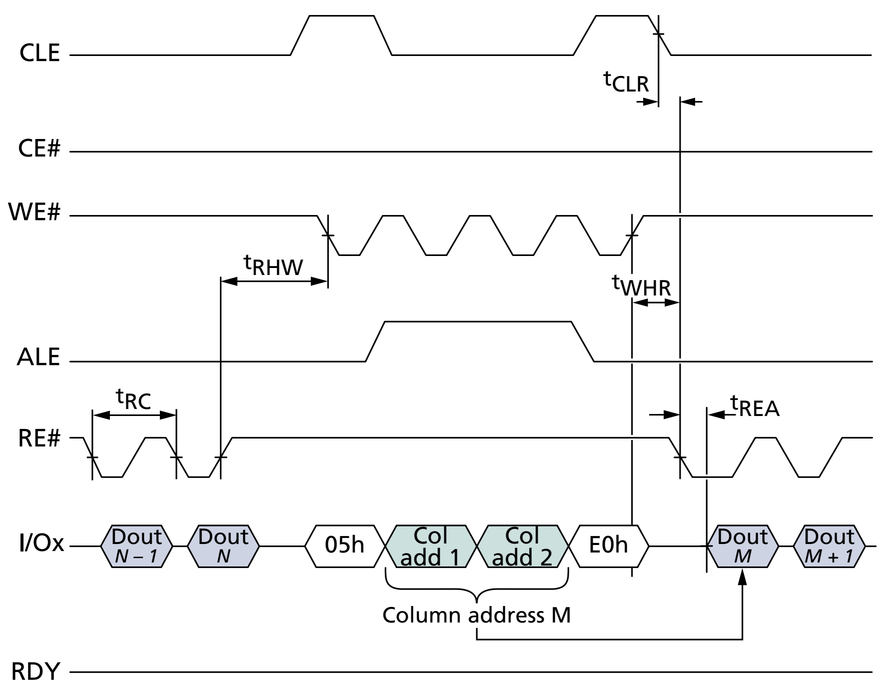


Figure 74: READ PAGE CACHE SEQUENTIAL

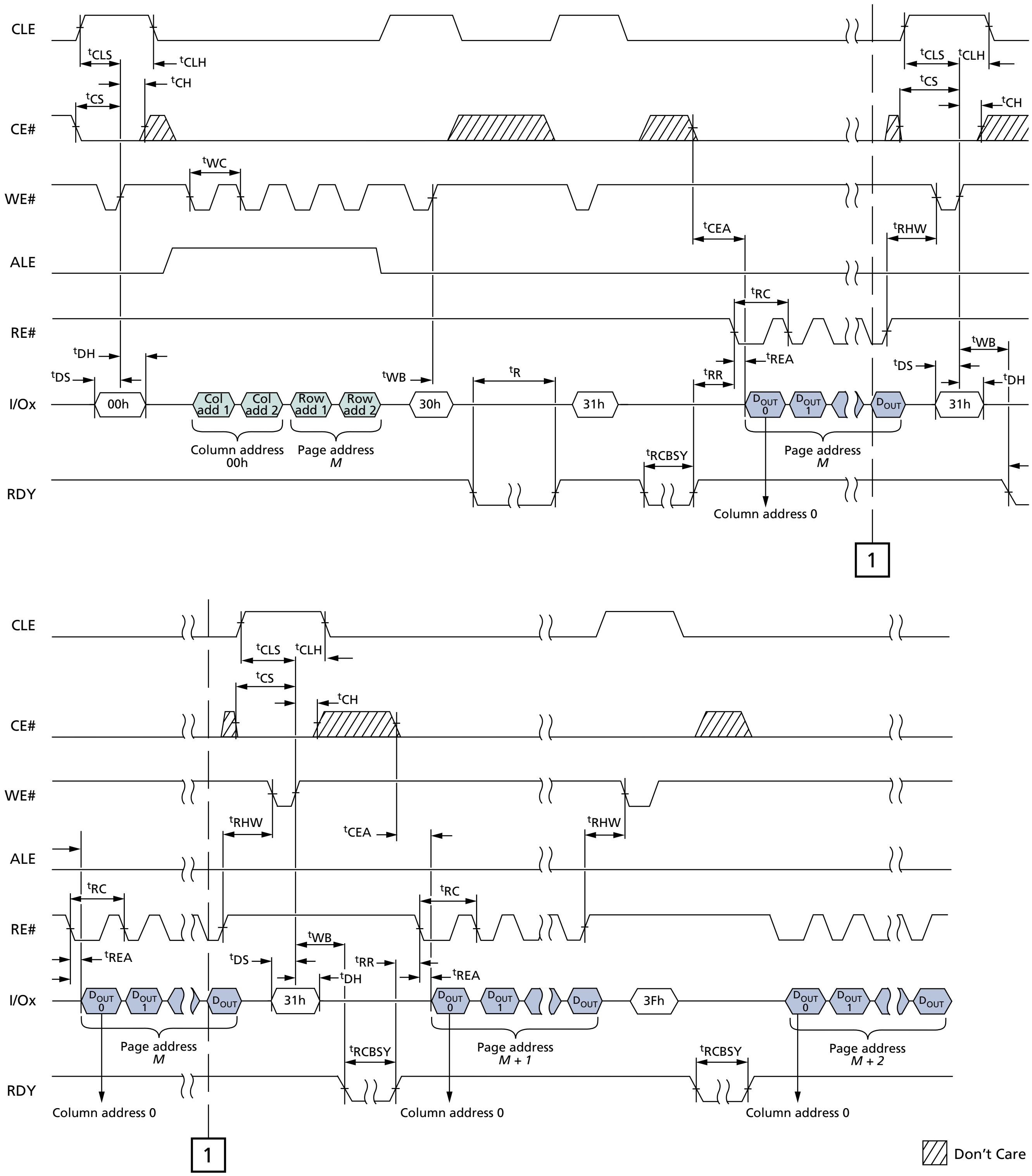


Figure 75: READ PAGE CACHE RANDOM

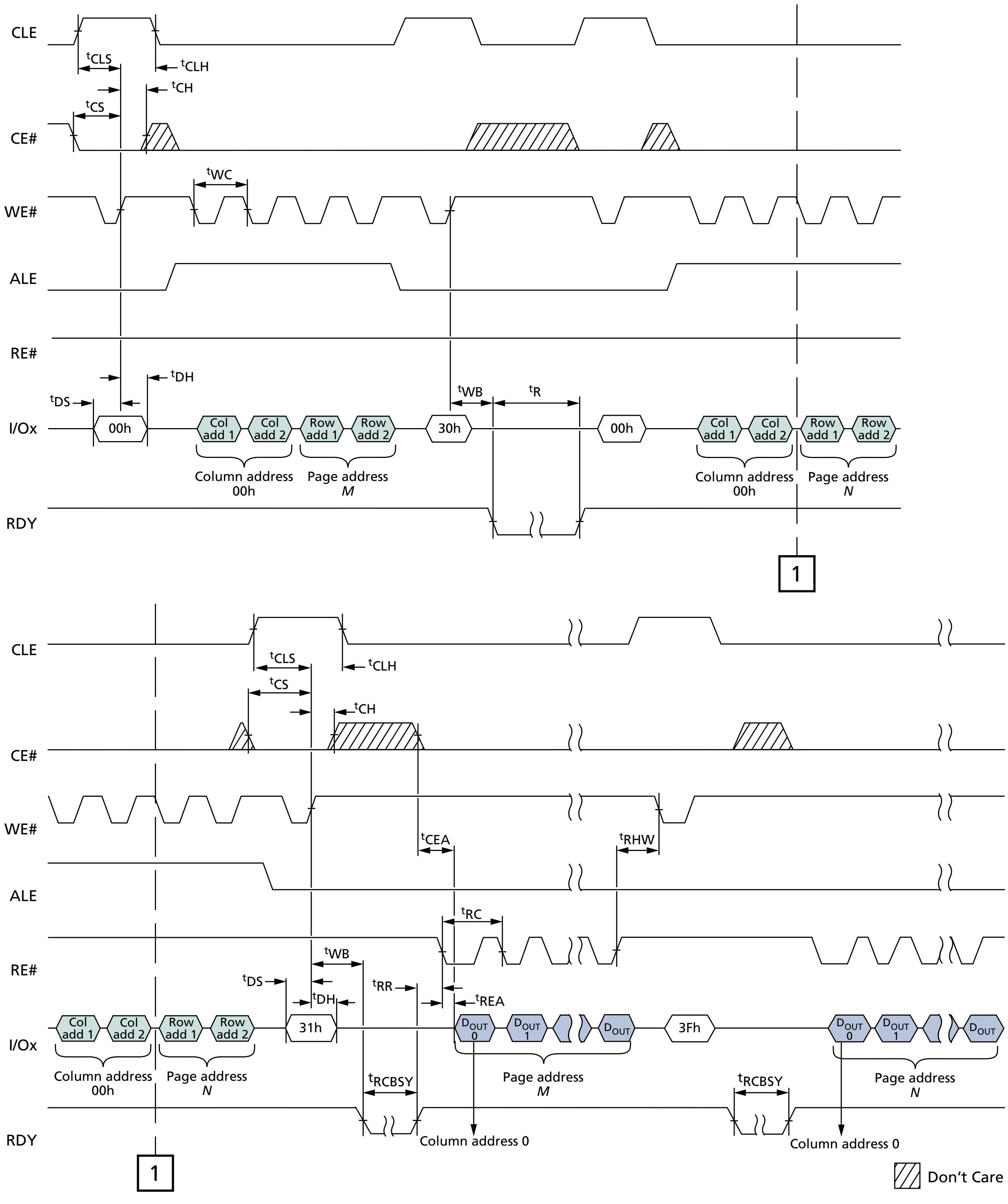


Figure 76: READ ID Operation

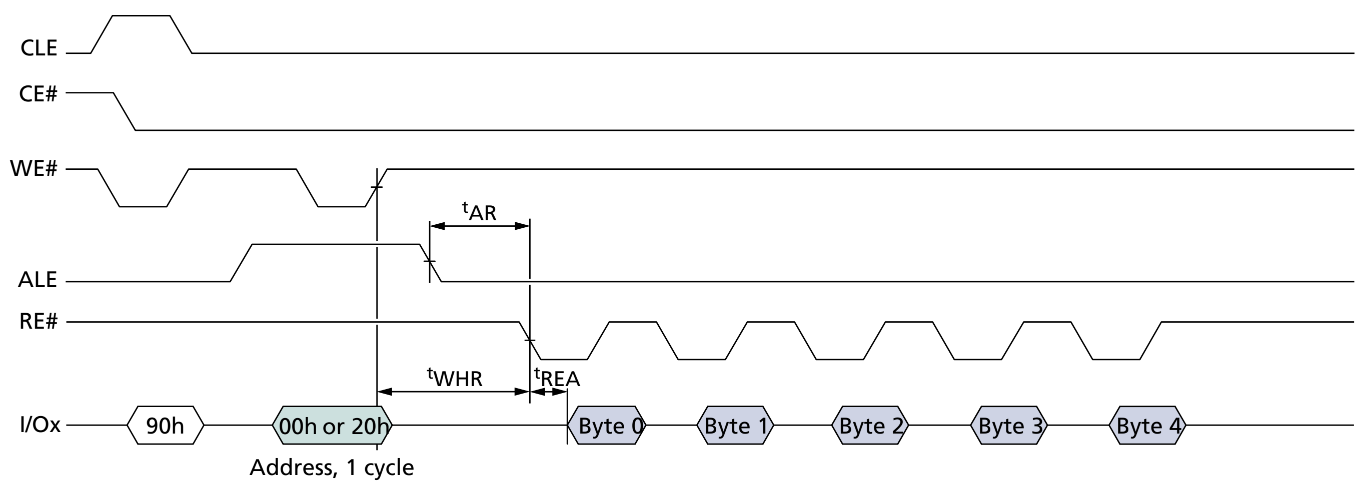


Figure 77: PROGRAM PAGE Operation

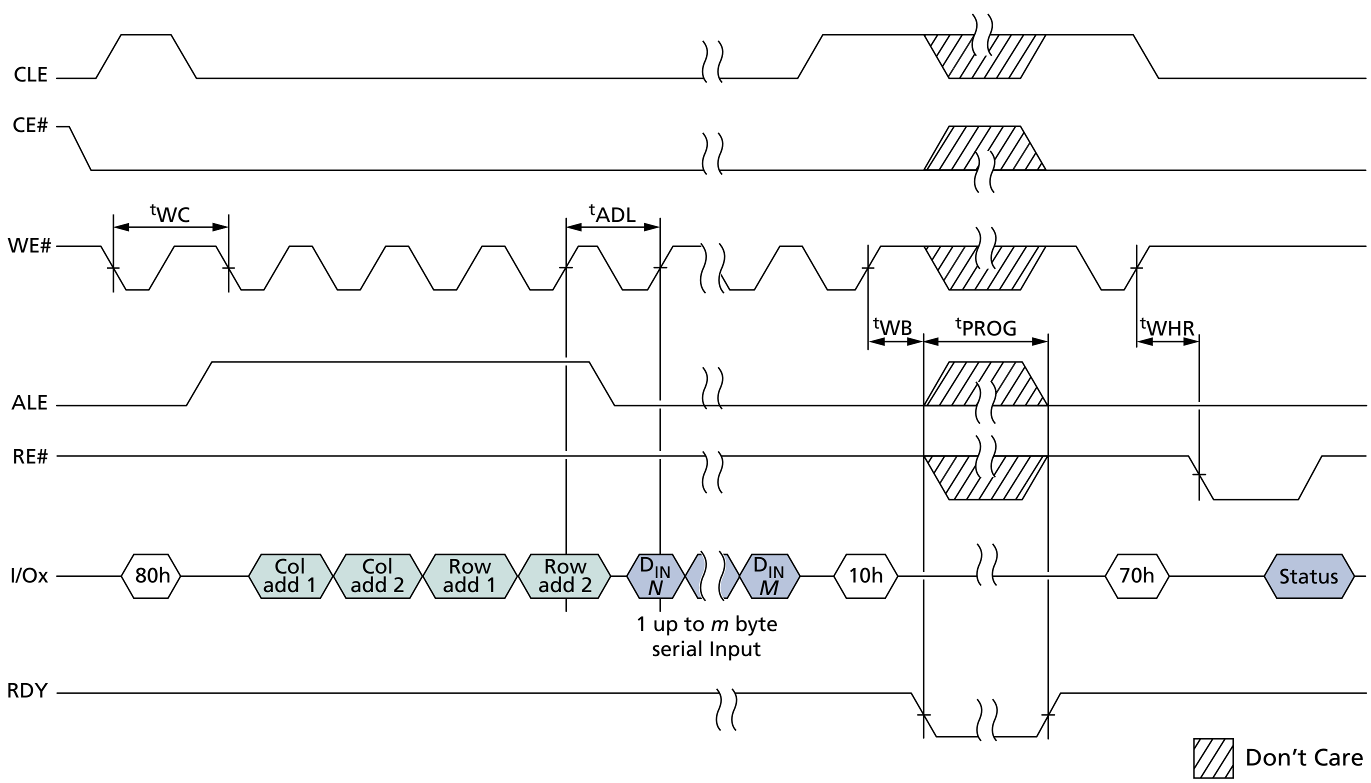


Figure 78: PROGRAM PAGE Operation with CE# "Don't Care"

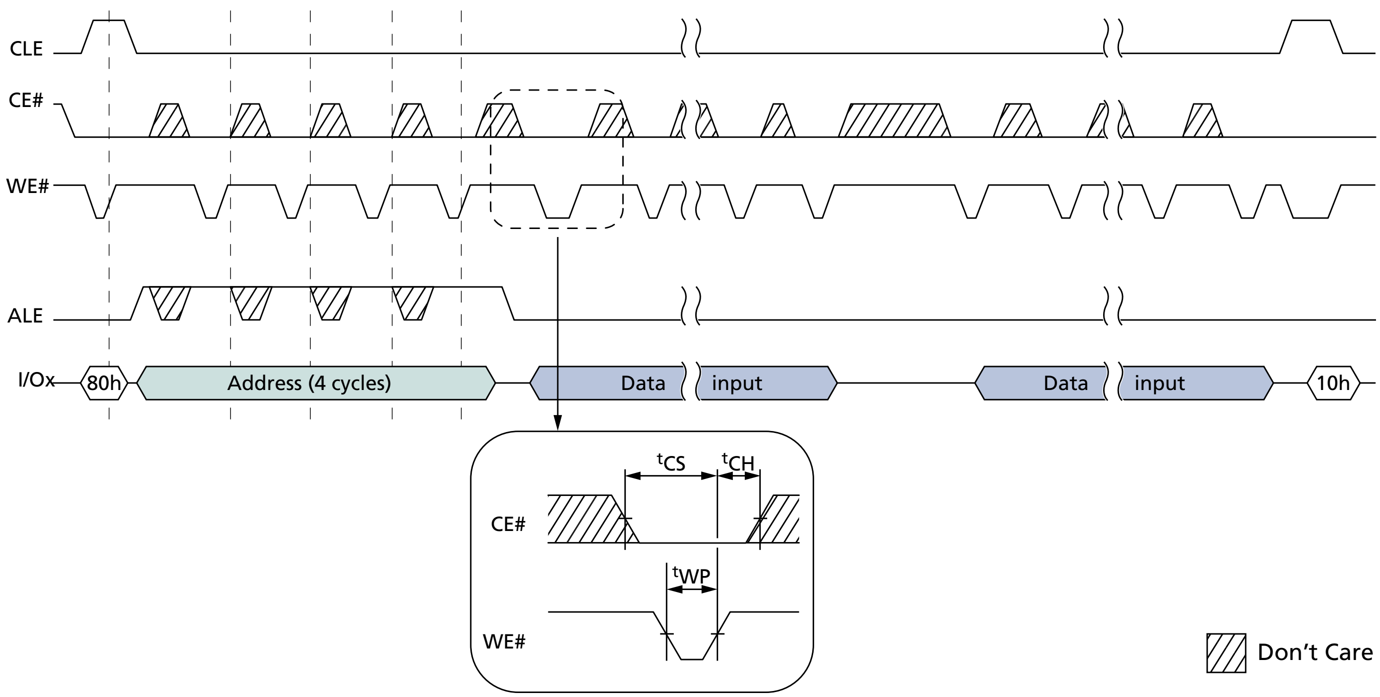


Figure 79: PROGRAM PAGE Operation with RANDOM DATA INPUT

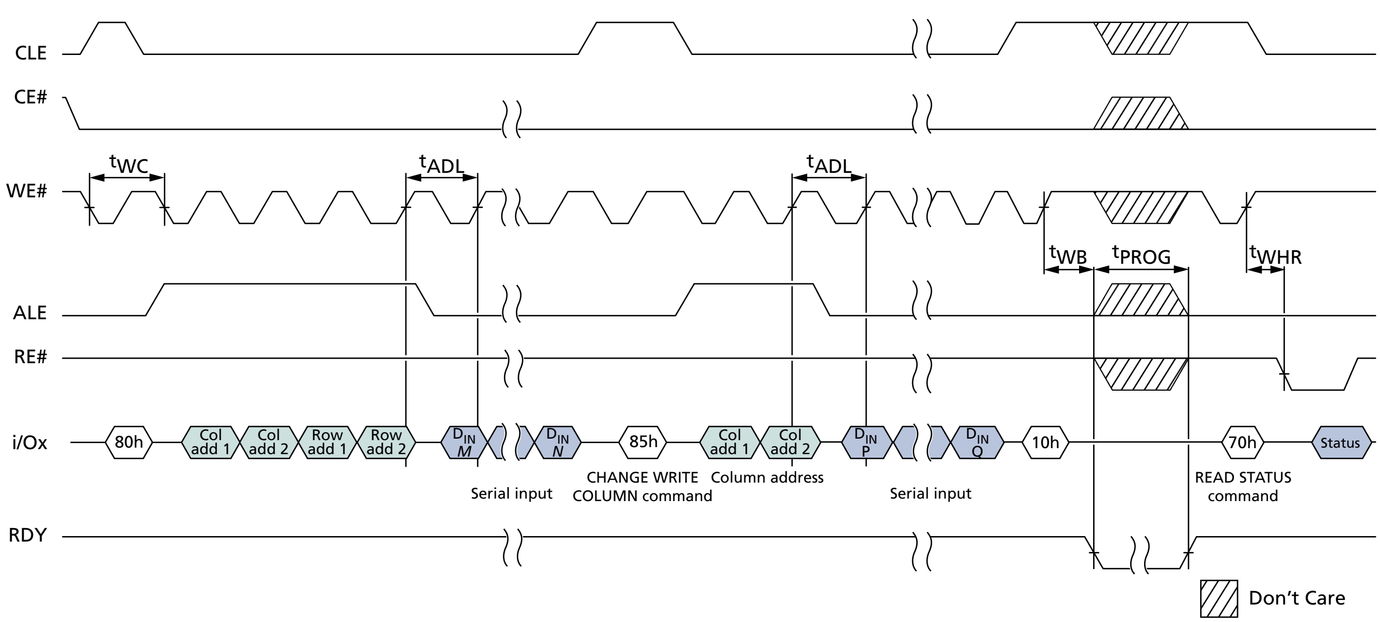


Figure 80: PROGRAM PAGE CACHE

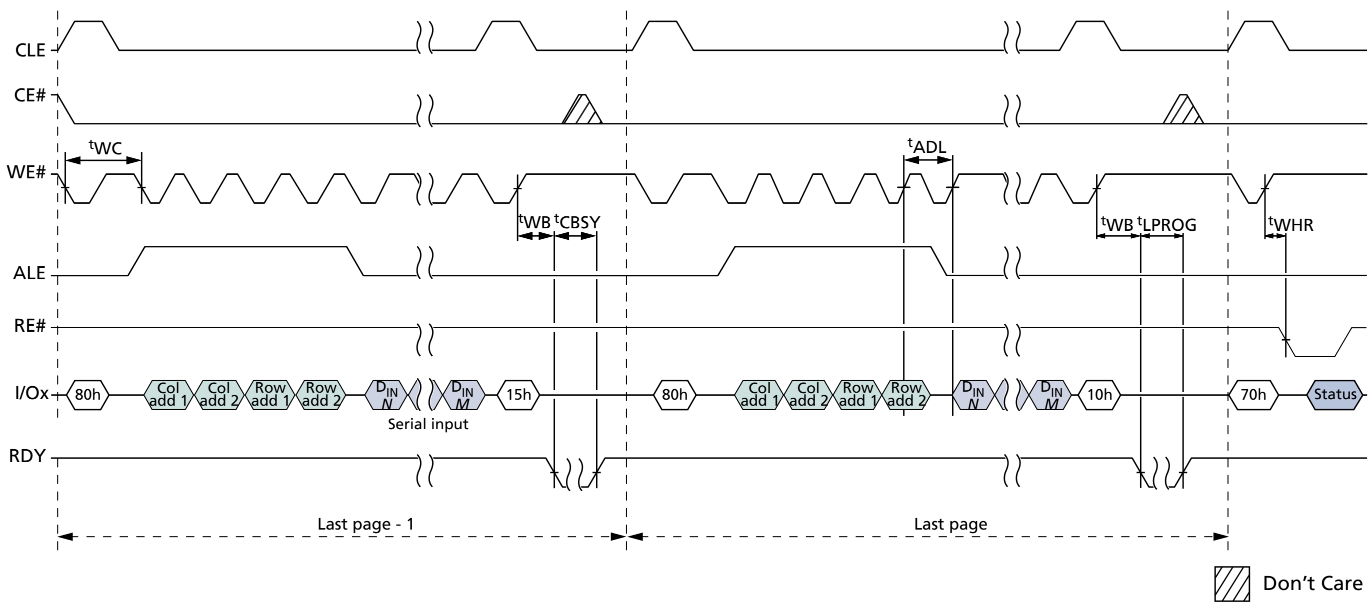


Figure 81: PROGRAM PAGE CACHE Ending on 15h

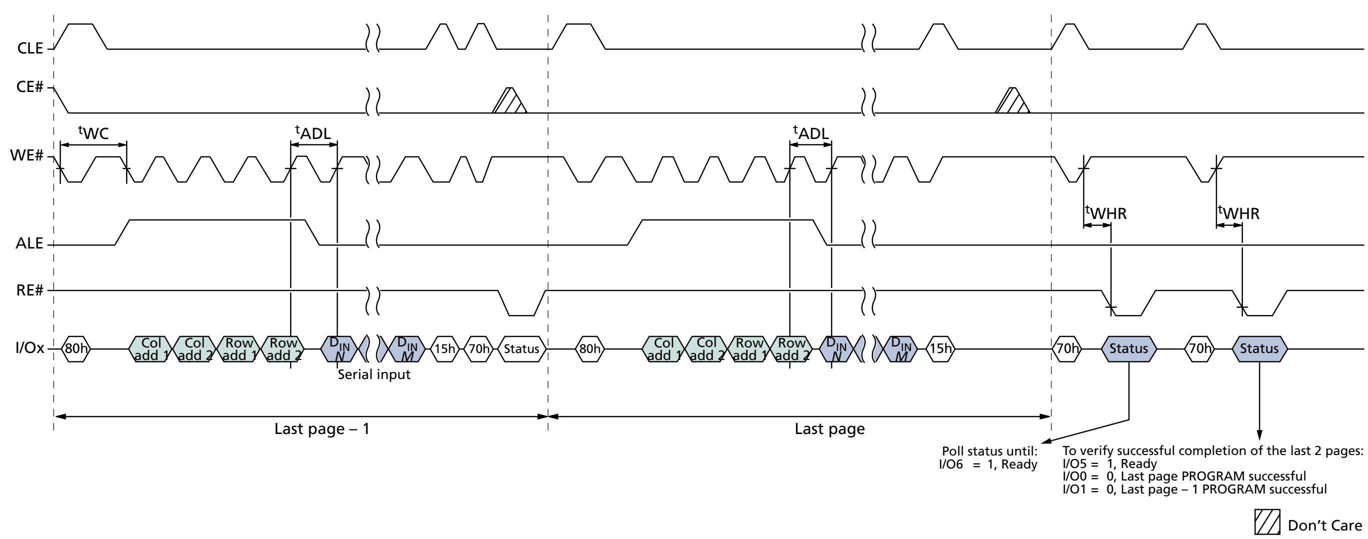


Figure 82: INTERNAL DATA MOVE

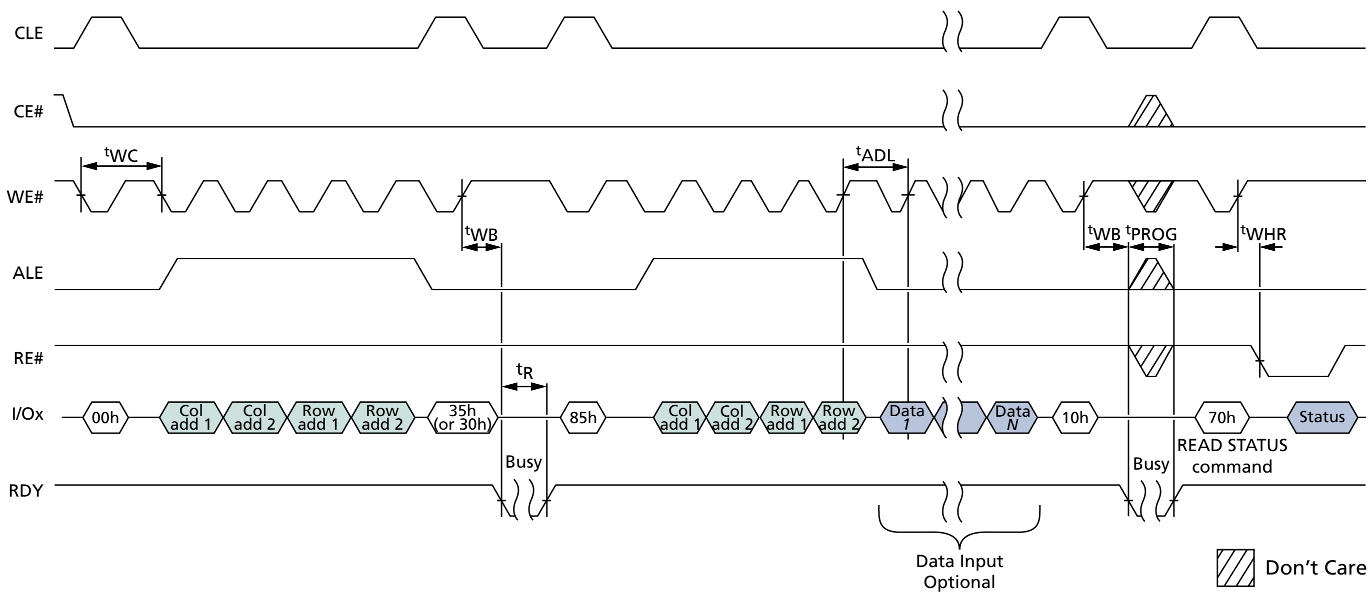
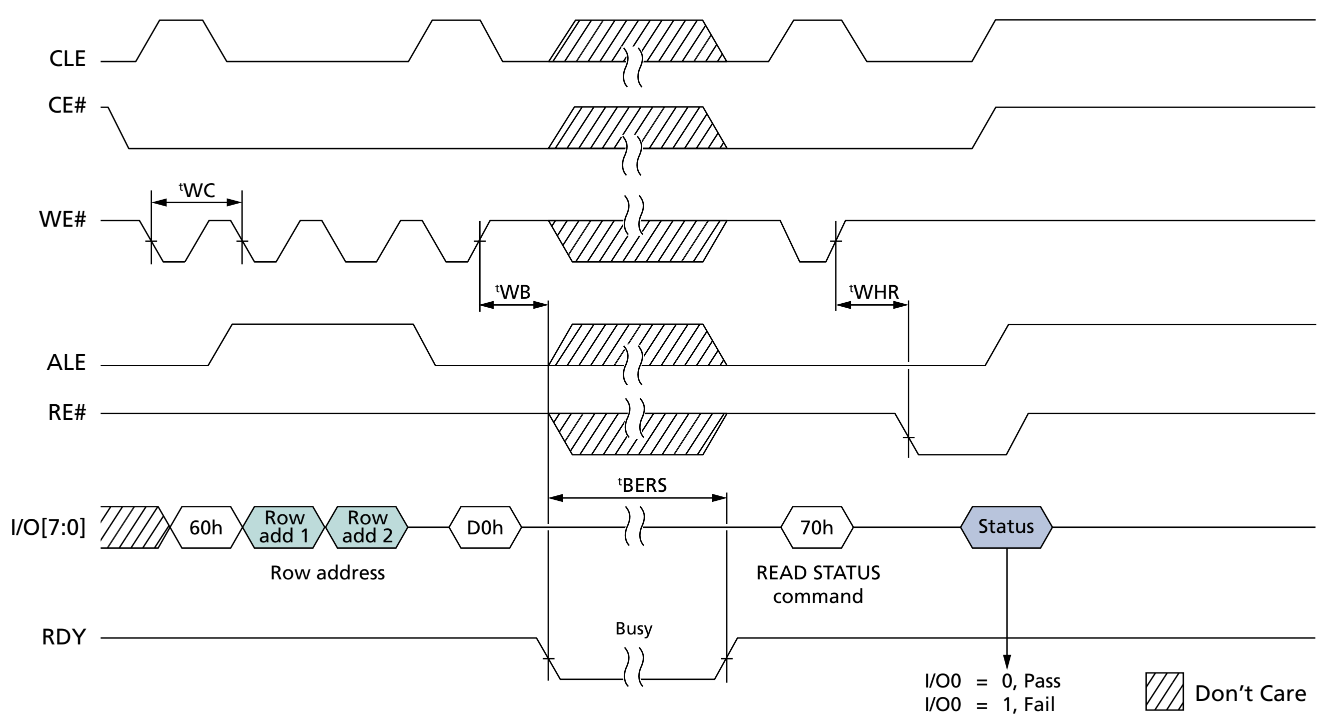


Figure 83: ERASE BLOCK Operation



Revision History

Rev D, Production – 01/10

- New Format Release

Rev C, Production – 7/09

- x8 Operational Example Table: Corrected maximum addresses for Block 0/Page 1 and Block 0/Page 2

Rev B, Production – 5/08

- Updated part numbers and added part number and content to support the H4 device
- Removed V_{CC} Power Cycling section and added Device Initialization section

Rev A, Production – 2/08

- Initial Release

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