MC10H644, MC10H644

68030/040 PECL to TTL Clock Driver

The MC10H/100H644 generates the necessary clocks for the 68030, 68040 and similar microprocessors. The device is functionally equivalent to the H640, but with fewer outputs in a smaller outline 20–lead PLCC package. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part–to–part skew, within–part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H644 also uses differential ECL internally to achieve its superior skew characteristic.

The H644 includes divide–by–two and divide–by–four stages, both to achieve the necessary duty cycle and skew to generate MPU clocks as required. A typical 50MHz processor application would use an input clock running at 100MHz, thus obtaining output clocks at 50MHz and 25MHz (see Logic Symbol).

The 10H version is compatible with MECL 10H™ ECL logic levels, while the 100H version is compatible with 100K levels (referenced to +5.0V).

- Generates Clocks for 68030/040
- Meets 68030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and ECL Power/Ground Pins
- Within Device Skew on Similar Paths is 0.5 ns
- Asynchronous Reset
- Single +5.0V Supply

Function

Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Synchronized Outputs: The device is designed to have the POS edges of the ÷2 and ÷4 outputs synchronized.

Select (SEL): LOW selects the PECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H644 also contains circuitry to force a stable state of the PECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

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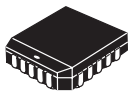
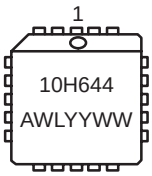


PLCC–20
FN SUFFIX
CASE 775

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10H644FN	PLCC–20	37 Units/Rail
MC100H644FN	PLCC–20	37 Units/Rail

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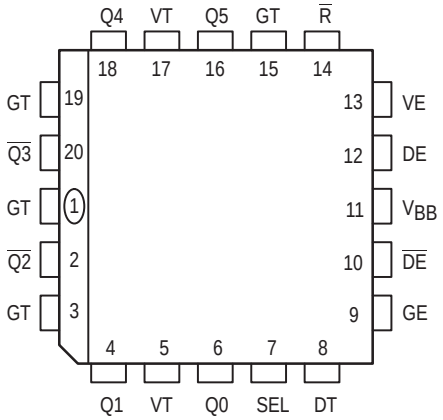
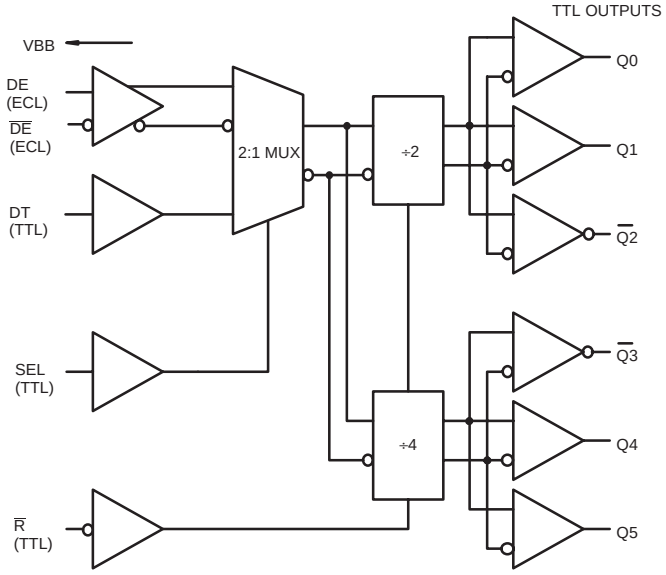
Pinout: 20–Lead PLCC (Top View)



LOGIC DIAGRAM



PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0V)
VT	TTL V_{CC} (+5.0V)
VE	ECL V_{CC} (+5.0V)
GE	ECL Ground (0V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

AC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay ECL D to Output	All Outputs	5.8	6.8	5.7	6.7	6.1	7.1	ns	CL = 50pF
t_{PLH}	Propagation Delay TTL D to Output		5.7	6.7	5.7	6.7	6.0	7.0	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	Q0, 1, 4, 5	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	$\overline{Q2}$, $\overline{Q3}$	–	0.5	–	0.5	–	0.5	ns	CL = 50pF
t_{skwd}*	Within–Device Skew	All Outputs	–	1.5	–	1.5	–	1.5	ns	CL = 50pF
$t_{skp–p}$*	Part–to–Part Skew	Q0, 1, 4, 5	–	1.0	–	1.0	–	1.0	ns	CL = 50pF
t_{PD}	Propagation Delay R to Output	All Outputs	4.3	7.3	4.3	7.3	4.5	7.5	ns	CL = 50pF
t_R t_F	Output Rise/Fall Time 0.8V – 2.0V	All Outputs	–	1.6	–	1.6	–	1.6	ns	CL = 50pF
f_{max}	Maximum Input Frequency		135	–	135	–	135	–	MHz	CL = 50pF
TW	Minimum Pulse Width Reset		1.5	–	1.5	–	1.5	–	ns	
t_{rr}	Reset Recovery Time		1.25	–	1.25	–	1.25	–	ns	
T_{PW}	Pulse Width Out High or Low @ f_{in} = 100 MHz and CL = 50 pf	Q0, 1	9.5	10.5	9.5	10.5	9.5	10.5	ns	CL = 50pf Relative 1.5V
TS	Setup Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	
TH	Hold Time SEL to DE, DT		2.0	–	2.0	–	2.0	–	ns	

* Skews are specified for Identical Edges

DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{EE}	Power Supply Current	ECL		65		65		65	mA	VE Pin
I_{CC}		TTL		85		85		85	mA	Total all V_T pins

TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		–0.6		–0.6		–0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = –3.0 mA I_{OH} = –24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		–1.2		–1.2		–1.2	V	I_{IN} = –18 mA
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0 V

10H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.83 3.05	4.16 3.52	3.87 3.05	4.19 3.52	3.94 3.05	4.28 3.55	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.73	3.65	3.75	3.69	3.81	V	VE = 5.0 V

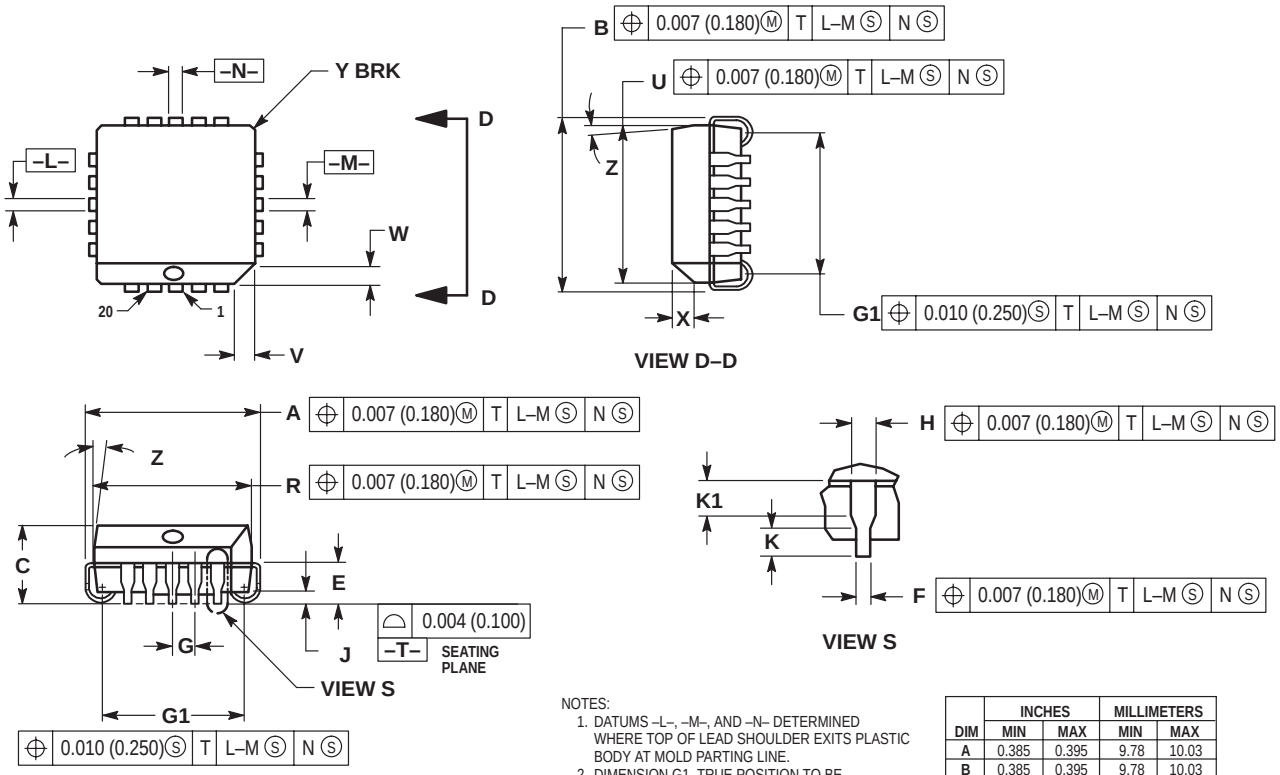
100H PECL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	 0.5	225	 0.5	175	 0.5	175	μA	
V_{IH}* V_{IL}*	Input HIGH Voltage Input LOW Voltage	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	3.835 3.19	4.12 3.525	V	VE = 5.0 V
V_{BB}*	Output Reference Voltage	3.62	3.74	3.62	3.74	3.62	3.74	V	VE = 5.0 V

* NOTE: PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for V_{CC} = 5.0 V.
Only corresponds to ECL Clock Inputs.

PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2 °	10 °	2 °	10 °
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

Notes

Notes

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