CS-514/514R

2, 4 or 6 Channel Ferrite Read/Write Circuit with Enhanced System Write to Read Recovery Time

Description

The CS-514/514R Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The CS-514R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The CS-514 is available in a variety of package and channel configurations.

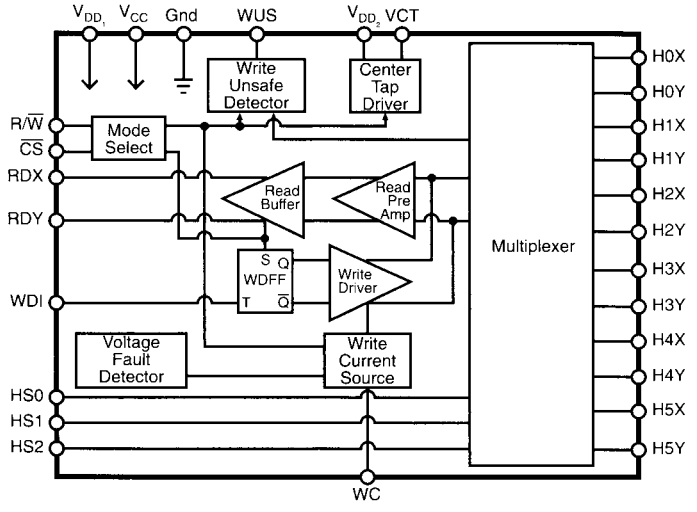
Features

- **High Performance: Read Mode Gain = 150 V/V Write current range = 10mA to 40mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the CS-117 & CS-510A**
- **Programmable write current source**
- **Write unsafe detection**
- **+5V, +12V power supplies**

Absolute Maximum Ratings

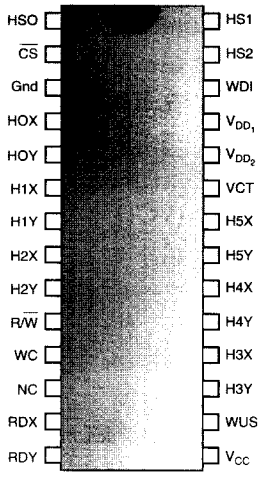
DC Supply Voltage	(V_{DD_1})	-0.3 to +14V_{DC}
	(V_{DD_2})	-0.3 to +14V_{DC}
	(V_{CC})	-0.3 to +6V_{DC}
Digital Input Voltage Range (V_{IN})		-0.3 to Vcc+0.3V_{DC}
Head Port Voltage Range (VH)		-0.3 to V_{DD_1}+0.3V_{DC}
WUS Pin Voltage Range (V_{WUS})		-0.3 to +14V_{DC}
Write Current		60mA
Output Current	RDX, RDY (I_O)	-10mA
	VCT	-60mA
	WUS	+12mA
Storage Temperature Range (T_S)		-65 to 150°C
Lead Temperature PDIP (10 sec Soldering)		260°C
Package Temperature PLCC, SO (20 sec Reflow)		215°C

Block Diagram

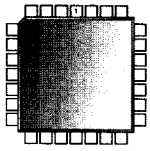


Package Options

18, 24, 28 L SO



28 L PLCC



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Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Supply Voltage (V_{DD_1})		10.8	12.0	13.2	VDC
(V_{CC})		4.5	5.0	5.5	VDC
Head Inductance (Lh)		5		15	µH
Damping Resistor (RD) (514 Only)		500		2000	Ω
RCT Resistor (RTC)*(1/4 Watt)	Iw=40mA	123	130	138	Ω
Write Current (IW)		10		40	mA
Junction Temperature Range (Tj)		+25		+125	°C

* For IW=40mA, At other IW levels refer to Applications Information that follows this specification.

DC Characteristics: Unless otherwise specified, recommended operating conditions apply.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Power Supply					
V_{CC} Supply Current					
Read/Idle	Read/Idle Mode			35	mA
Write	Write Mode			30	mA
V_{DD} Supply Current					
Idle	Idle Mode			20	mA
(sum of V_{DD_1} and V_{DD_2})					
Read	Read Mode			35	mA
Write	Write Mode			20+Iw	mA
Power Dissipation	T_J=+125°C				
Idle	Idle Mode			400	mW
Read	Read Mode			600	mW
Write	Write Mode, IW=40mA, RCT=0Ω			800	mW
	Write Mode, IW=40mA, RCT=130Ω			800	mW
■ Digital I/O					
VIL, Input Low Voltage				0.8	VDC
VIH, Input High Voltage		2.0			VDC
IIl, Input Low Current	VIL=0.8V	-0.4			mA
IIH, Input High Current	VIH=2.0V			100	µA
VOL, WUS Output, Low Voltage	IOL=8mA			0.5	VDC
IOH, WUS Output High Current	VOH=5.0V			100	µA
■ Write Mode					
Center Tap Voltage (VCT)	Write Mode		6.7		VDC
Head Current (per side)	Write Mode, $0 \le V_{CC} \le 3.7V$ $0 \le V_{DD_1} \le 8.7V$	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
I_{WC} to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY=6V Write/Idle Mode	-100		100	µA

DC Characteristics: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Read Mode					
Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode $0 \le V_{CC} \le 5.5V$ $0 \le V_{DD_1} \le 13.2V$	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

Dynamic Characteristics and Timing: Unless otherwise specified, VDD1=VDD2=12V±10%, VCC=5V±10%, +25°C≤T_J≤125°C, IW=35mA, Lh=10µH, Rd=750Ω, f(WDI)=5MHz, Cl (RDX, RDY)≤20pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **Write Mode**					
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	514	10			kΩ
	514R	600		960	Ω
WDI Transition Frequency	WUS=low	250			kHz
■ **Read Mode**					
Differential Voltage Gain	Vin=1mVpp@300kHz	125		175	V/V
Dynamic Range	DC Input Voltage, VI, Where Gain Falls by 10%. $V_{IN}=V_I$+0.5mVpp@300kHz	-2		+2	mV
Bandwidth (-3db)	Zs<5Ω, Vin=1mVpp	30			MHz
Input Noise Voltage	BW=15MHz, Lh=0, Rh=0			1.5	nV/√Hz
Differential Input Capacitance	f=5MHz			20	pF
Differential Input Resistance	f=5MHz 514	3.2			kΩ
	514R	500		1000	Ω
Common Mode Rejection Ratio	Vcm=VCT+100mVpp @5MHz	50			db
Power Supply Rejection Ratio	100mVpp @ 5MHz on VDD1, VDD2, or VCC	45			db
Channel Separation	Unselected Channels: Vin=100mVpp@5MHz & Selected Channel: Vin-0mVpp	45			db
Single Ended Output Resistance	f=5MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA
■ **Switching Characteristics**					
R/W to Write	Delay to 90% of Write Current			1.0	µs
R/W to Read	Delay to 90% of 100mV, 10MHz Read Signal Envelope or to 90% decay of Write Current				

Dynamic Characteristics and Timing: continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Switching Characteristics (continued)					
CS to Select	Delay to 90% of Write Current or to 90% of 100mV 10MHz Read Signal Envelope			1.0	µs
CS to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0-HS2 to any Head	Delay to 90% of 100mV 10MHz Read Signal Envelope			1.0	µs
WUS: Safe to Unsafe-TD1	Iw=35mA	1.6		8.0	µs
Unsafe to Safe-TD2				1.0	µs
Head Current	Lh=0µH, Rh=0Ω				
Prop. Delay-TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10%-90% Points			20	ns

Package Pin Description

PACKAGE PIN #				PIN SYMBOL	FUNCTION
	SO Wide		PLCC		
18	24	28	28		
18	24	1	1	HSO	Head Select
1	1	2	2	CS	Chip Select: a low level enables device
2	2	3	3	Gnd	Ground
4	3	4	4	H0X	X, Y Head connections
5	4	5	5	H0Y	X, Y Head connections
13	5	6	6	H1X	X, Y Head connections
12	6	7	7	H1Y	X, Y Head connections
	7	8	8	H2X	X, Y Head connections
	8	9	9	H2Y	X, Y Head connections
6	9	10	10	R/$\overline{W}$	Read/Write: a high level selects Read Mode
7	10	11	11	WC	Write Current: used to set the magnitude of the write current
3	15, 16	12	12	NC	No connection
8	11	13	13	RDX	X, Y Read Data: Differential read signal out
9	12	14	14	RDY	X, Y Read Data: Differential read signal out
10	13	15	15	V_{CC}	+5V
11	14	16	16	WUS	Write Unsafe: a high level indicates an unsafe writing condition
	17	17	17	H3Y	X, Y Head connections
	18	18	18	H3X	X, Y Head connections
		19	19	H4Y	X, Y Head connections
		20	20	H4X	X, Y Head connections
		21	21	H5Y	X, Y Head connections
		22	22	H5X	X, Y Head connections

Package Pin Description: continued

PACKAGE PIN #				PIN SYMBOL	FUNCTION
SO Wide			PLCC		
18	24	28	28		
14	19	23	23	VCT	Voltage Center Tap: voltage source for head center tap
15	20	24	24	V_{DD_2}	Positive power supply for the center-tap voltage source
16	21	25	25	V_{DD_1}	+12V
17	22	26	26	WDI	Write Data In: negative transition toggles direction of head current
		27	27	HS2	Head Select
	23	28	28	HS1	Head Select

Circuit Description

Circuit Operation

The CS-514 addresses up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, CS, and R/W, as shown in tables 1 & 2. Internal resistor pullups, provided on pins CS and R/W, will force the device into a non-writing condition if either control line is opened accidentally.

Table 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	X	Idle

Table 2: Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0=Low level 1=High level X=Don't care

Write Mode

The write mode configures the CS-514 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor made be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or a power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open connector output pin, WUS.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag. To reduce internal power dissipation, an optional external resistor, RCT, given by RCT≤130Ω x 40/Iw (Iw in mA), is connected between pins V_{DD_1} and V_{DD_2}. Otherwise, connect pin V_{DD_1} to V_{DD_2}.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

Circuit Description: continued

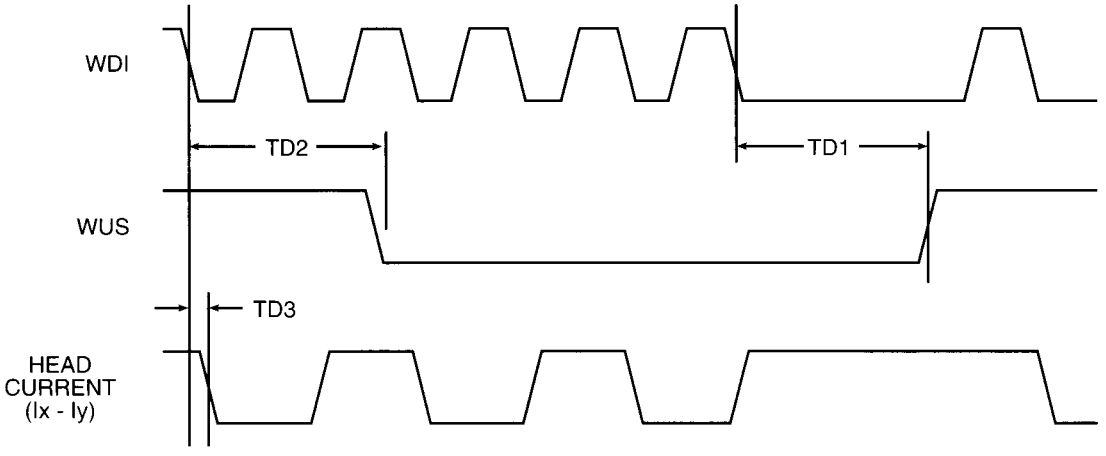
Read Mode

The Read mode configures the CS-514 as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode , minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequence pulse detection circuitry.

Idle Mode

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

Write Mode Timing Diagram



Application Information

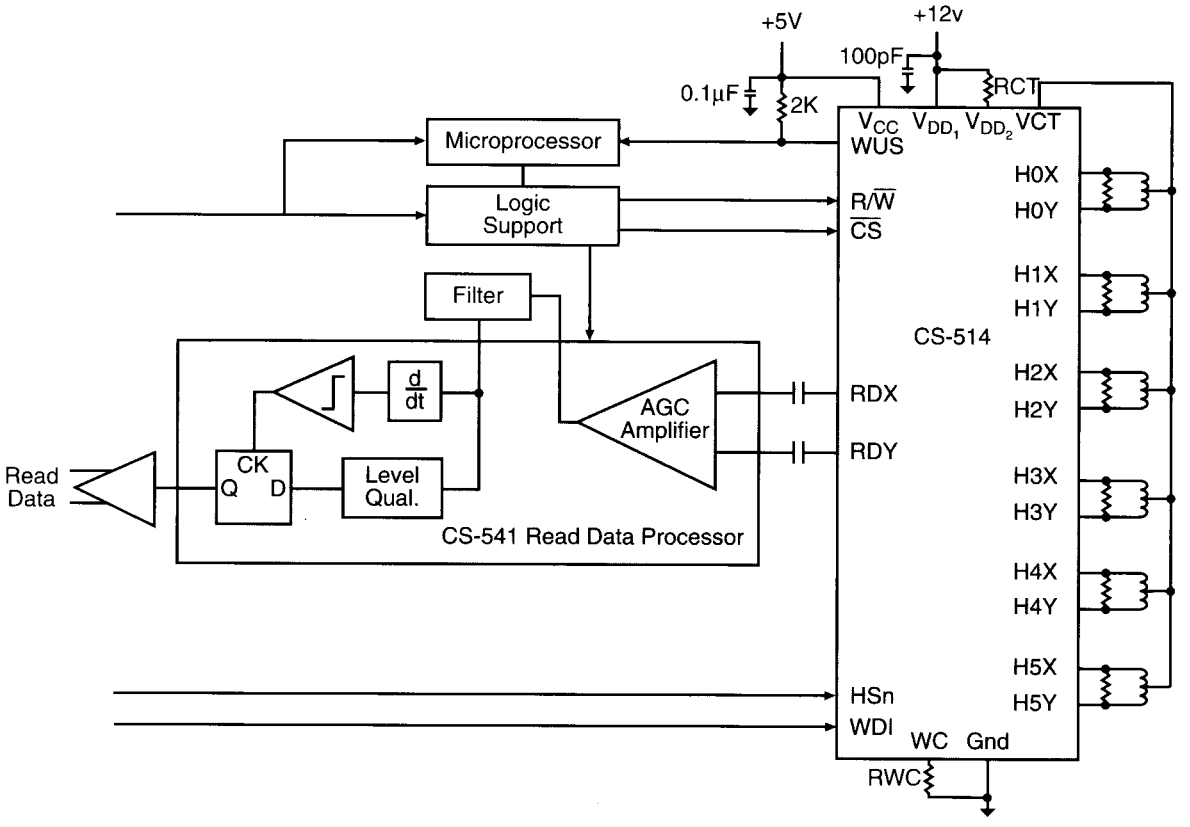
Table 3: Key Parameters Under Worst Case Input Noise Conditions

Parameter		T_J=25°C	T_J=135°C	Units
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	514R	850	1000	Ω
	514	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

Table 4: Key Parameters Under Worst Case Input Impedance Conditions

Parameter		T_J=25°C	T_J=135°C	Units
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	514R	500	620	Ω
	514	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

Application Diagram



Notes:

1. An external resistor, RCT, given by; RCT≤130 (40/Iw) where Iw is the zero peak write current in mA, can be used to limit internal power dissipation. Otherwise connect V_{DD_2} to V_{DD_1}.
2. Damping resistors not required on CS-514R versions.
3. Limit DC current from RDX and RDY to 100µA and load capacitance to 20pF. In multichip application these outputs can be wire-OR'd.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

Package Specification

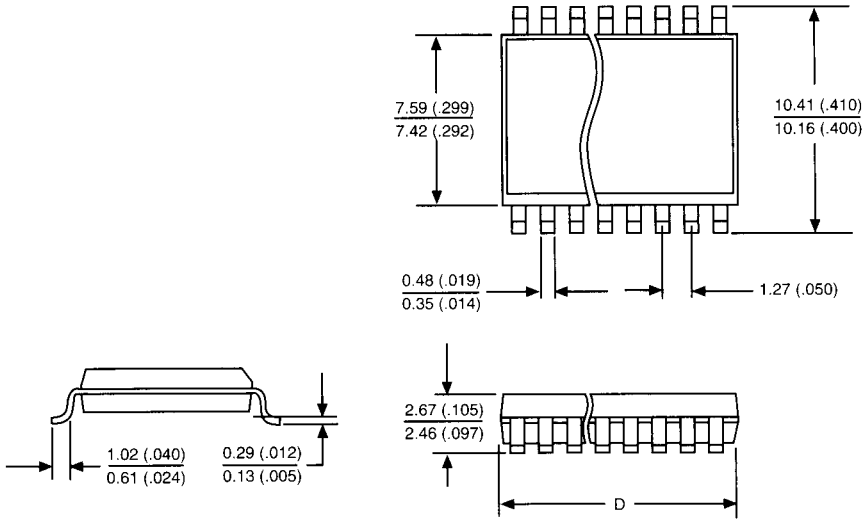
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D Metric Max	D Metric Min	D English Max	D English Min
18L SO WIDE	11.71	11.46	.461	.451
24L SO Wide	15.54	15.29	.612	.602
28L SO Wide	18.06	17.81	.711	.701

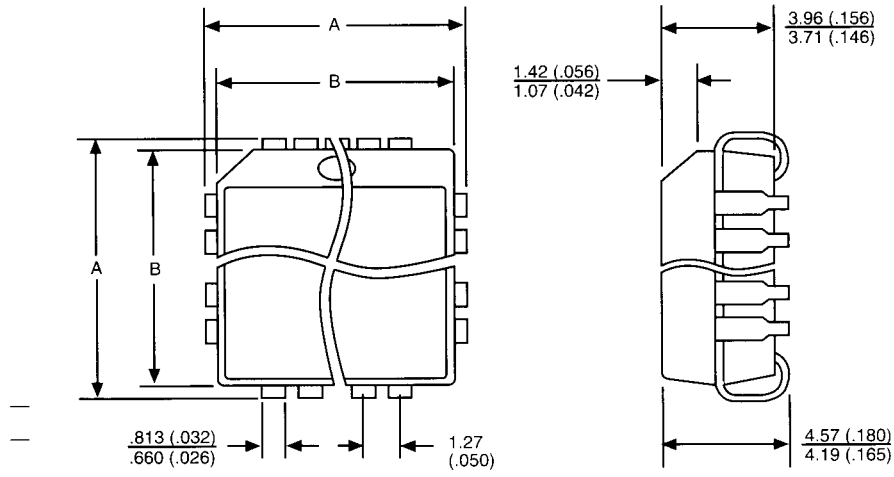
PACKAGE THERMAL DATA

Thermal Data	$R\Theta_{JA}$ typ	$R\Theta_{JC}$ typ	
18L SO	100	21	°C/W
24L SO	80	16	°C/W
28L SO	75	15	°C/W
28L PLCC	70	18	°C/W

SO Wide



PLCC



Ordering Information

Part Number	Description
CS-514-2DW18	18 Lead SO
CS-514-2RDW18	18 Lead SO
CS-514-4DW24	24 Lead SO
CS-514-6DW28	28 Lead SO
CS-514-6FN28	28 Lead PLCC

Preliminary

This product is in the preproduction stages of the design process. The data sheet contains preliminary data. CSC reserves the right to make changes to the specifications without notice. Please contact CSC for the latest available information.

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