



## N-Channel 200-V (D-S) Fast Switching MOSFET

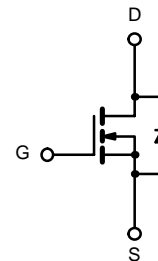
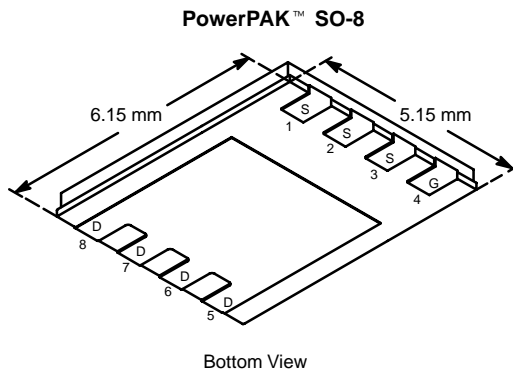
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
200	0.24 @ $V_{GS} = 10$ V	2.8
	0.26 @ $V_{GS} = 6$ V	2.7

### FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching

### APPLICATIONS

- Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	200		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	2.8	1.8	A
		$T_A = 70^\circ\text{C}$	2.2	1.5	
Continuous Source Current	$I_S$	3.5	1.5		
Pulsed Drain Current	$I_{DM}$	8			
Avalanche Current <sup>b</sup>	$I_{AS}$	3			
Single Avalanche Energy <sup>b</sup>	$E_{AS}$	0.45		mJ	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	4.2	1.8	W
		$T_A = 70^\circ\text{C}$	2.6	1.1	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	25	30	$^\circ\text{C/W}$
		Steady State	60	70	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	2.9	3.5		

Notes

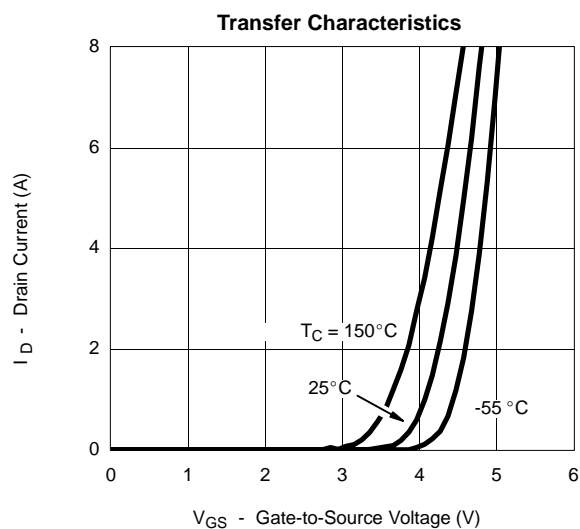
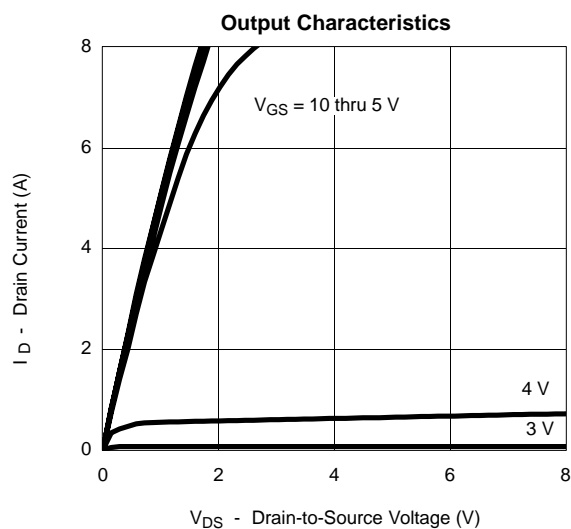
- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Guaranteed by design, not subject to production testing.

**MOSFET SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	8			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.8 A		0.195	0.24	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 2.7 A		0.210	0.26	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.8 A		8		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 3.5 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.8 A		12	18	nC
Gate-Source Charge	Q <sub>gs</sub>			2.5		
Gate-Drain Charge	Q <sub>gd</sub>			3.8		
Gate-Resistance	R <sub>G</sub>			2.5		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, R <sub>L</sub> = 100 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		10	15	ns
Rise Time	t <sub>r</sub>			12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			15	25	
Fall Time	t <sub>f</sub>			15	25	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 3.5 A, di/dt = 100 A/μs		60	90	

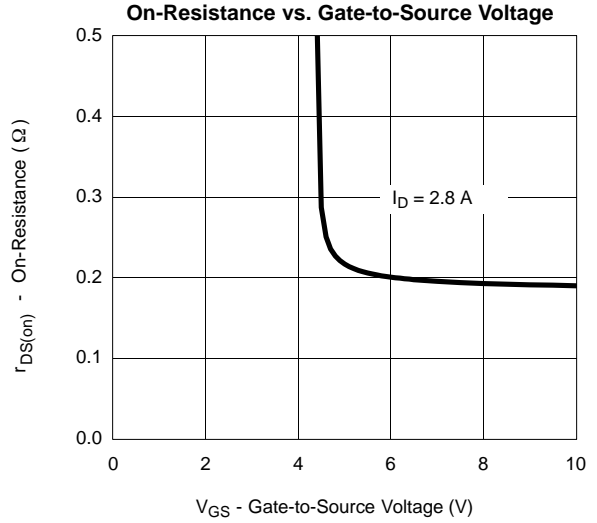
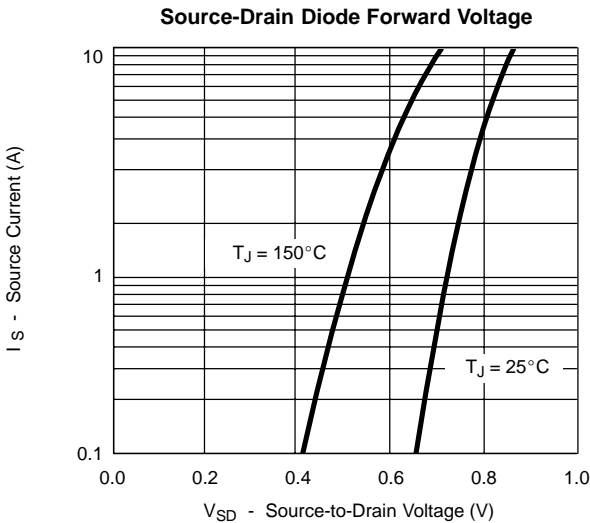
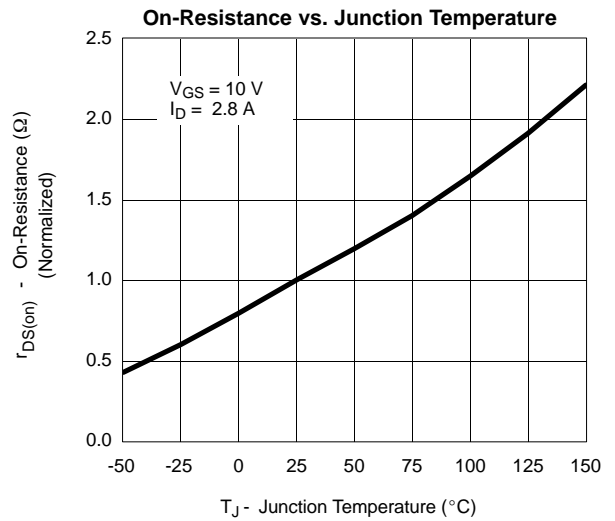
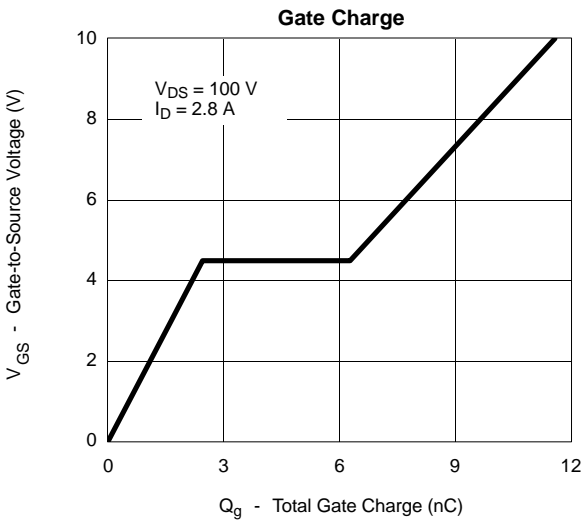
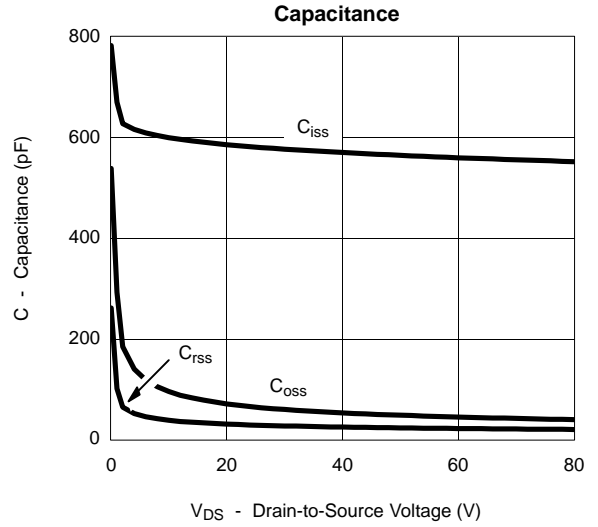
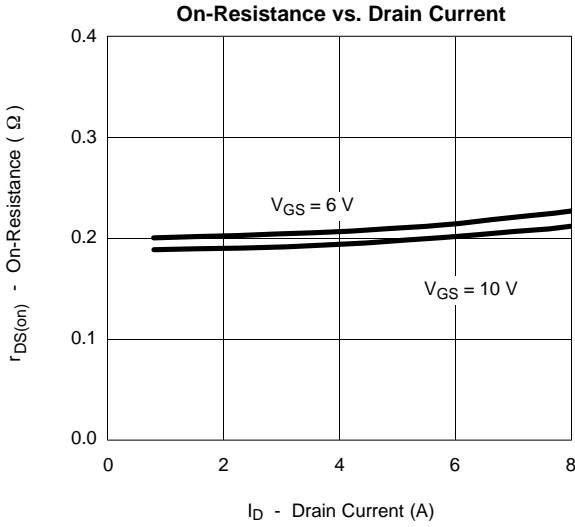
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



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