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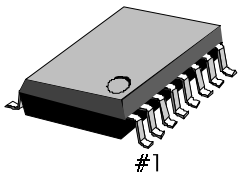
INTRODUCTION

KS8809 is a superior low-power-programmable PLL frequency synthesizer which can be used in high performance / Simple application for a Wide Area Pager system.

KS8809 consists of 2 kinds of divider block including a 19-bit Shift register, 16/18bits Latch, 13/15bits R-counter and 16/18bit N-Counter, 32/33 Prescaler, and a phase detector block including a Phase detector, Lock detector and a Charge pump.
KS8809 also has a battery saving mode which can control each register block by serial control data from the μ-controller (MICOM) and it also has boost up signal output for fast locking.

16-TSSOP-0044



(Magnification = 1 : 4)

FEATURES

- Maximum operating frequency: 330MHz @ 300mV$_{P-P}$, V_{DD1} = 1.0V, V_{DD2} = 3.0V
- On-chip reference oscillator supports external crystal which oscillates up to 23MHz
- Superior supply current:
  - — F_{FIN} = 310MHz, I_{DD1} = 0.8mA (Typ.) @ V_{DD1} = 1.0V, V_{DD2} = 3.0V
- Operating voltage: V_{DD1} = 0.95 to 1.5V and V_{DD2} = 2.0 to 3.3V
- Excellent Divider range:
  - — Ref. Divider:
    FRC (0): 1 / 40 to 1 / 65528 (Multiple 8): Default
    FRC (1): 1 / 5 to 1 / 32767
  - — Rx Divider:
    PBC (0): 1 / 1056 ~ 1 / 65535: Default
    PBC (1): 1 / 1056 ~ 1 / 262143
- Boost-up signal output for Fast Locking
- In the Standby mode, V_{DD1} block can be controlled by BSB pin status
  - — Standby current consumption: 10μA (Max.)
- Programmable control the output of LD to reduce internal noise
- Programmable 17 / 19-bit shift register value controlled by PBC
- Charge pump output circuitry for passive filter
- Package type: 16–TSSOP (0.65mm)

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ORDERING INFORMATION

Device	Package	Operating Temperature
+KS8809	16–TSSOP–0044	–25°C to +75°C

+: New Product

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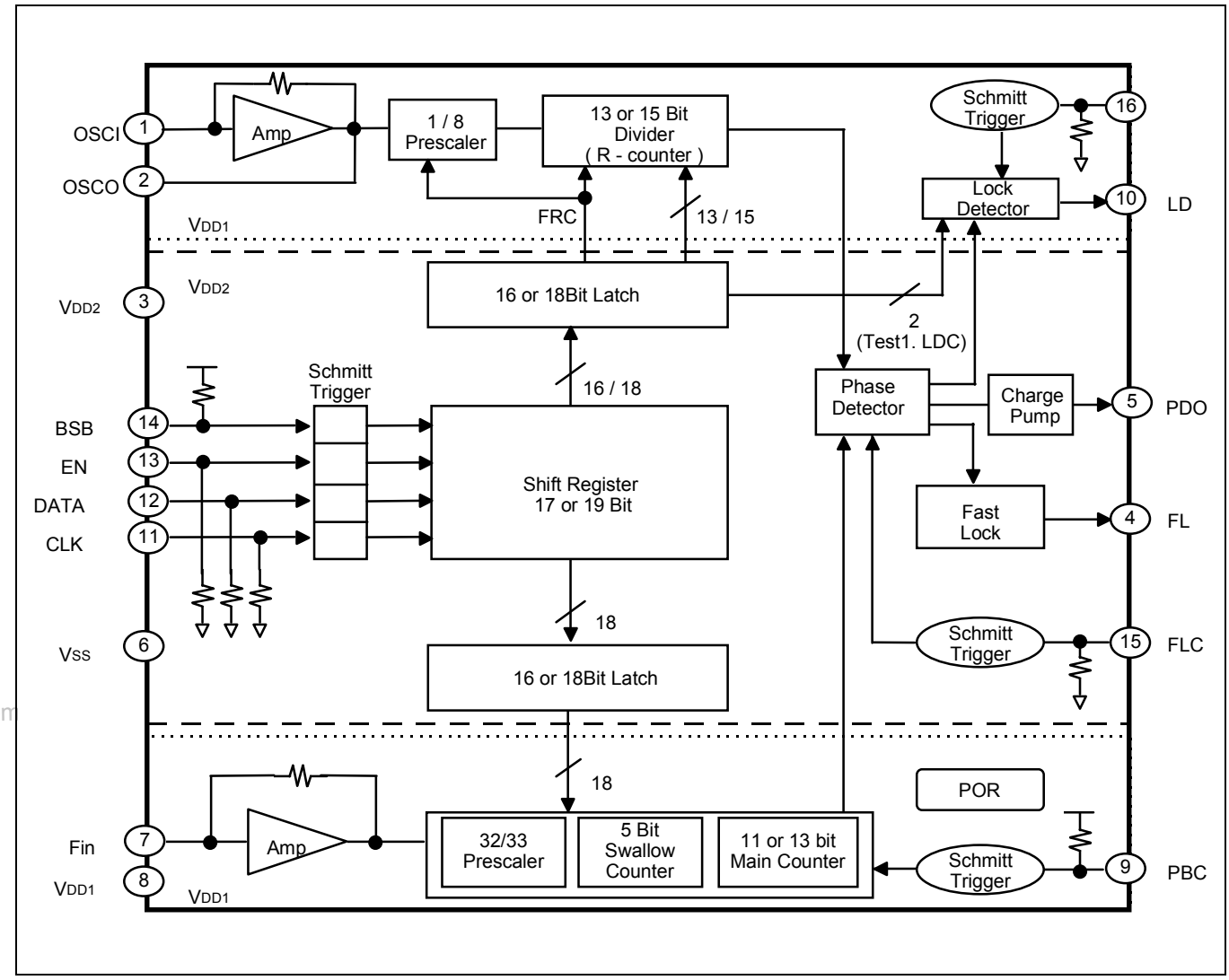
BLOCK DIAGRAM



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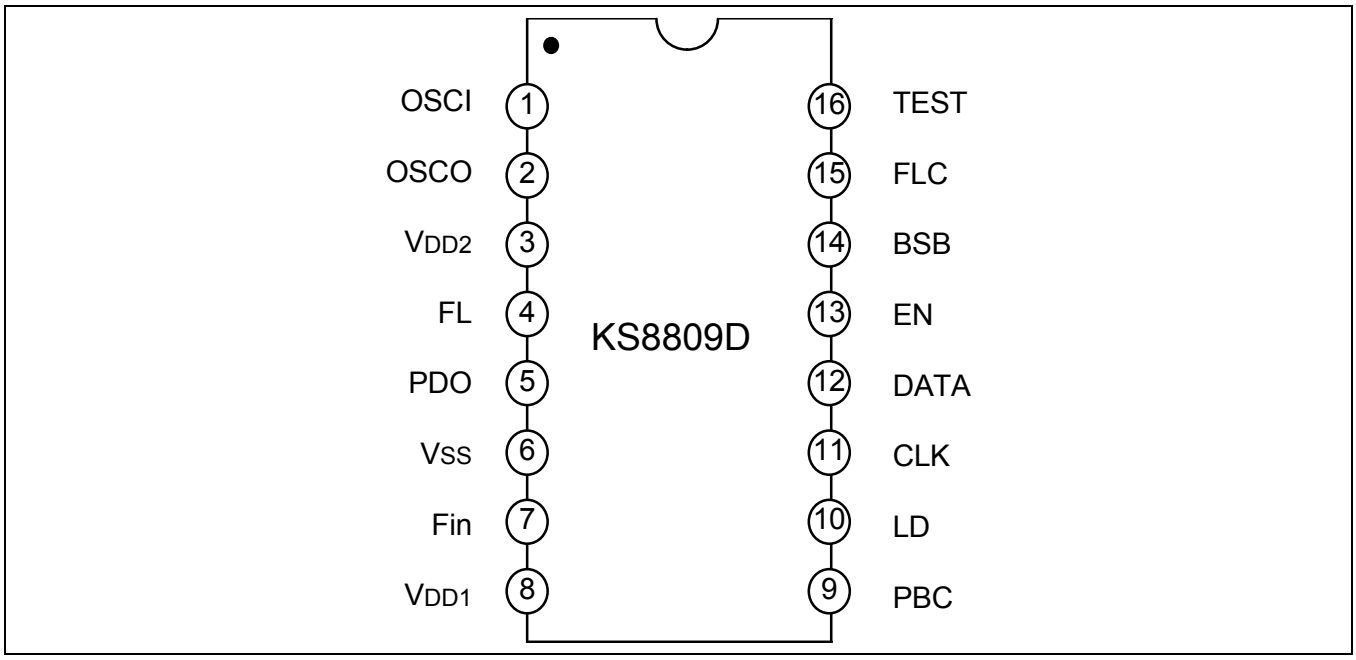
PIN CONFIGURATION



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PIN DESCRIPTION

Pin No	Symbol	Description
1	OSCI	These input / output pins generate the reference frequency. In case of OSCI Pin, external reference frequency can be used through the AC coupling.
2	OSCO	
3	V_{DD2}	The highest potential supply terminal that can be supplied up to 2.0 ~ 3.3V.
4	FL	Booster signal output for fast locking.
5	PDO	The output of RX phase detector terminal for passive loop filter. There are 3-kinds of output signal states according to Rx loop error.
6	V_{SS}	Ground terminal
7	Fin	Input terminal for the 16/18bits divider from VCO. Output frequency from VCO was inputted through AC coupling
8	V_{DD1}	Voltage supply terminal for Oscillator and Fin block. This pin can be supplied up to 0.95 ~ 1.5V from V_{SS}.
9	PBC	This is an input for programmable bit control which has Schmitt Trigger architecture, Internally biased pull-up. High = 16 Bits N-Divider (Default: ND0 ~ ND15) Low = 18 Bits N-Divider (ND0 ~ ND7) cf) R-divider bits will be changed by the FRC bit of program
10	LD	The output of phase detector can be controlled by R-counter register. When the LDC bit of R-counter set to Low, the output will be disabled to reduce a noise problem, but if it is set to High, the output will be enabled to show an lock / unlock status that is the error width between to Ref. signal and the VCO output signal.
11	CLK	These pins are controlled by the μ-controller which has Schmitt Trigger architecture, Internally biased pull-down. The features of these pins are as follows; Clock input for 17 or 19-bit Shift Register, Serial data input (it includes TEST1, FRC and LDC), Latch enable input.
12	DATA	
13	EN	
14	BSB	In the BS mode (set to Low), the V_{DD1} block will be powered off, but the internal latch data is still valid because the V_{DD2} is supplied continuously. This input has Schmitt Trigger architecture & internally biased pull-up.
15	FLC	This is the input pin for Fast Locking Control (FLC) which has Schmitt Trigger architecture, Internally biased pull-down. Low = The Current of PDO Charge pump output is Normal (Default: x1) High = The Current of PDO Charge pump output is increase (x 1.5)
16	TEST	This is the input pin for TEST which has Schmitt trigger architecture. Internally biased Pull-down. Low = All block will be operated as normal state (Default) High = LD and FL state will be TEST mode

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD} ~ V_{DD2}	–0.3 ~ +4.0	V
Input Voltage	V_I	V_{SS} ~ 0.3 ~ V_{DD} + 0.3	V
Power Dissipation	P_D	350	mW
Operating Temperature	T_{OPR}	–25 ~ +75	°C
Storage Temperature	T_{STG}	–40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{DD1} = 1.0V, V_{DD2} = 3.0V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD1}	–	0.95	1.0	1.5	V
	V_{DD2}	–	2.0	3.0	3.3	
Operating current	IDD	F_{OSCI} = 12.8MHz F_{FIN} = 310MHz @ 0.3V_{P-P} V_{DD1} = 1.0V, V_{DD2} = 3.0V, BSB=High	–	0.8	–	mA
Standby current	ISB1	V_{DD1} = 0.0V, V_{DD2} = 3.0V, BSB=Low	–	0.1	10	μA
Input voltage (DATA, CLK, EN, BS)	V_{IL}	–	–	–	0.3	V
	V_{IH}	–	V_{DD2}-0.3	–	–	
Input voltage (TEST, PBC)	V_{IL}	–	–	–	0.2	V
	V_{IH}	–	V_{SS1}-0.2	–	–	
Input current (Fin, Xin)	I_{IH}	V_{IH} = V_{DD1}, BSB = High	–	–	20	μA
	I_{IL}	V_{IL} = 0V, BSB = High	–	–	20	
Input frequency	F_{FIN}	V_{FIN} = 0.3V_{P-P}, V_{DD1} = 1.0V	40	–	330	MHz
	F_{OSCI}	V_{OSCI} = 0.3V_{P-P}, V_{DD1} = 1.0V	7	12.8	23	
Output current (PDO, FL)	I_{OH1}	V_{OH} = 0.4V	1.0	–	–	mA
	I_{OL1}	V_{OL} = V_{DD2} - 0.4V	1.0	–	–	
Output current (LD)	I_{OH2}	V_{OH} = 0.4V	0.1	–	–	mA
	I_{OL2}	V_{OL} = V_{DD2} - 0.4V	0.1	–	–	
Setup-time (DATA-CLK, CLK-EN)	ts	–	2	–	–	μS
Hold time	t_H	–	2	–	–	μS

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FUNCTIONAL DESCTRIPTION

Table 1. N-Counter Register Program Scheme (19 bit)

Bit	Bit 18 (ND 17) ~ Bit 1 (ND 0)	Bit 0 (LSB)
Name	ND	PMC
Description	N-Counter Data (ND 17 ~ ND 0)	Program Mode Control
Function	16/18 Bit Program Data PBC = 1 : 16 bits (ND 15 ~ ND 0) will be valid PBC = 1 : 18 bits (ND 17 ~ ND 0) will be valid	0: N-Counter Program 1: Ref. R-Counter Program

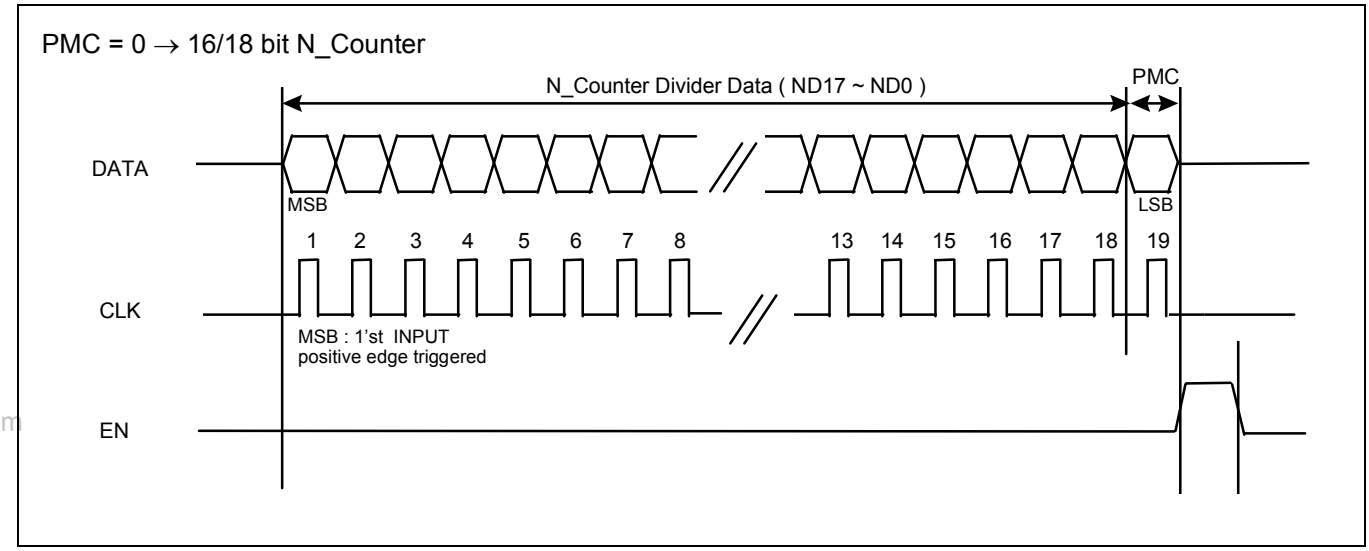

Figure 1. Rx. N - Counter Register Programming Timing

- Programmable N-counter consists of 5-bits Swallow Counter, Dual moduars Prescaler and 11-bits Main Counter (if [PBC = 0], than 13-bits Main Counter)
- The Divide Ratio is;
  $N = (P + 1) \times S + P (M - S) = PM + S;$

  P = Dual Modulars Prescaler (32)
  S = 5-bits Swallow Counter value (0 ~ 31)
  M = 11-bits (PBC = High, 32 ~ 2047) or 13-bits (PBC = Low, 32 ~ 8291)
  N = Programmable N-Counter value (N > S)
- The Main Counter can be controlled by PBC pin, when the PBC (pin 9) state set to Low, the Programmable N-counter range will be extended up to 262143

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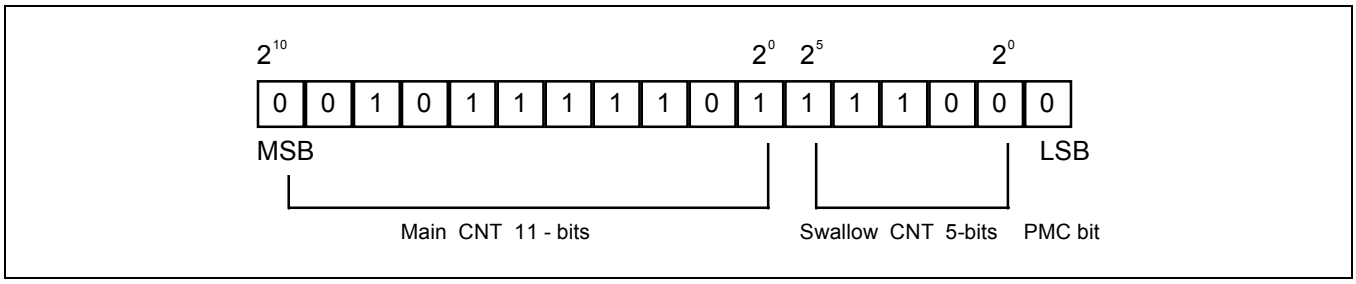
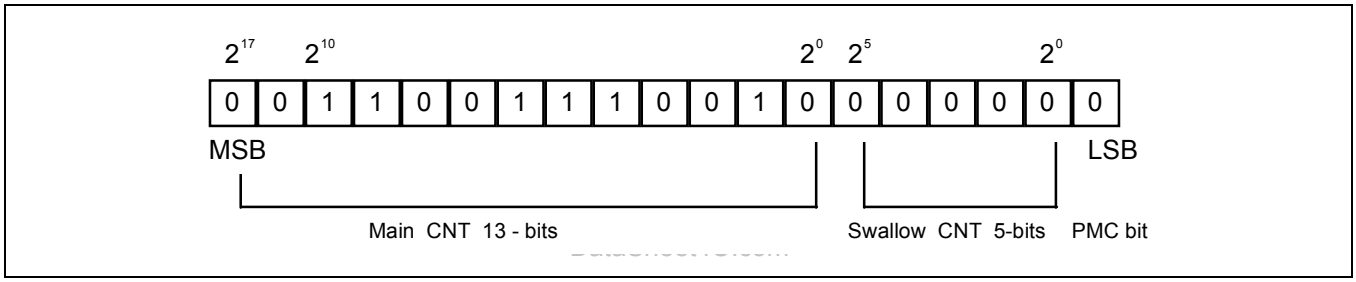
- Ex 1) In case of 16-bits program [PBC = High], Fc = 325.300MHz, Multiplier = 4, Fin = 75.975MHz
  [Fin Freq. / Ref. Frequ.] = 75.975MHz / 6.25kHz = 1256



NOTE: According to the above equation, 12156 / 32(P) = 379, and left = 28
that means, Swallow CNT value is "11100", Main CNT value is "379"

- Ex 2) In case of 18-bits program [PBC = Low], Fin = 330MHz
  [Fin Freq. / Ref. Freq.] = [330MHz / 6.25kHz] = 52800



NOTE: The PMC bit is program mode control bit, if [0], the N-counter will be enabled

Table 2. R-Counter Register Program Scheme (19 bits)

Bit	Bit 18 ~ Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Name	RD	LDC	FRC	TEST 1	PMC
Description	Ref. R-Counter Data (RD 14 ~ RD 0)	Lock Detector Control	Frequency of Reference Control	TEST mode control	Program mode control
Function	15 Bit Programmable Ref. R-Counter FRC = 0 : 13 bits (RD12 ~ RD0) FRC = 1 : 15 bits (RD14 ~ RD0)	0: Disable LD out 1: Enable LD out	0: R_CNT div. = 8 × RD 1: R_CNT div. = RD (15bit)	Mainly for the product Test	0: ND Program 1: RD Program

- The Input Reference Frequency (X-tal Oscillator) will be divided by 1/8 Prescaler, and then divided by pre-programmed R-counter value once more.
- Programmable R-Counter consists of Fixed 1/8 Prescaler, 13 / 15-bits Programmable Counter
  When FRC = 0, Fixed 1/8 Prescaler and 13-bits counter (Min. Divide value: 5) are enabled
  RD = 8, R = 40 (= 8 × 5) ~ 65528 [Multiple 8]
  When FRC = 1, Fixed 1/8 Prescaler is disabled, but using 15-bits counter (Min. Divide value: 5)
  RD = R = 5 ~ 32767 [All value]

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CONTROL MODE FOR R-COUNTER REGISTER

LDC	LDC Pin State	Description
0	Low	LDC function is independent of the other Control Bit
1	Normal Operation	

FRC	R-Counter Value	Description
0	8 × R_Cnt value (OSCI / 8 × R), Use 13 bits R-Counter	FRC function is independent of the other Control Bit
1	R-Cnt value (OSC / R), Use 15 bits R-Counter	

TEST1	TEST	LD state	FL state	Description
0	0	Normal	Normal	• FRC is independent of the other control bit • Test is internal register control bit but, Test is external control pin • Test is related with Test, when Test = High → Test Mode
1	0	Normal	Normal	
0	1	Fn (N-CNT)	High state	
1	1	Fr (N-CNT)	Normal	

PMC = 1 → 13/15 bit R-Counter, LDC, FRC, TEST1

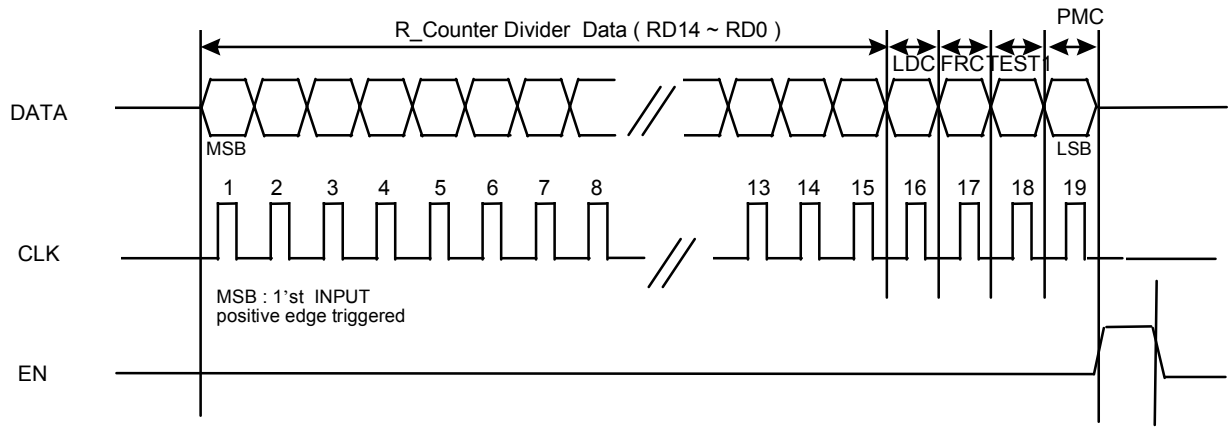

Figure 2. Ref. R-Counter Register Programming Timing

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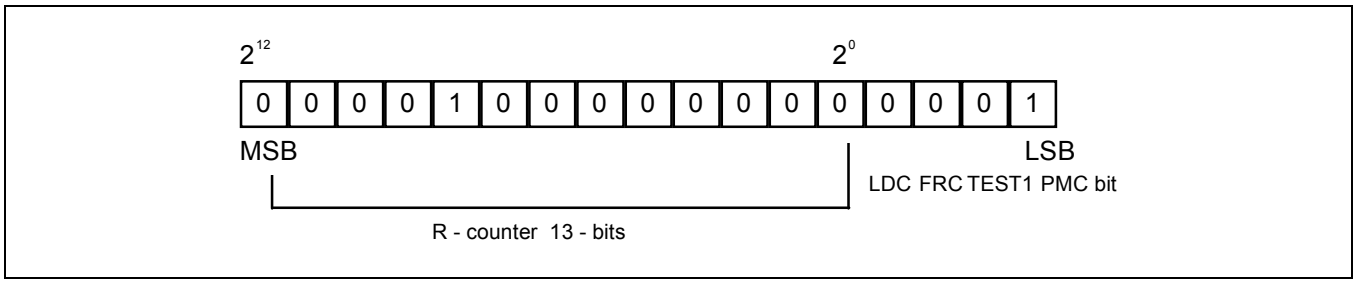
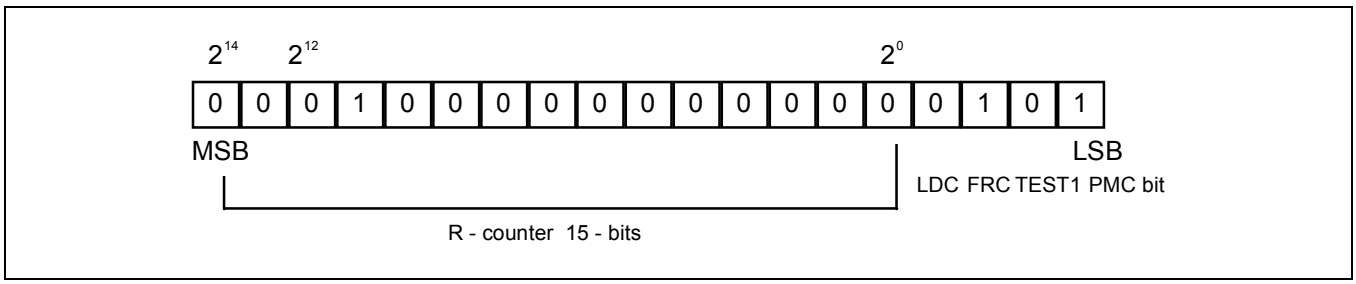
- Ex 1) FRC = 0, In case of 13bits Program, Fosc = 12.8MHz and 1/8 prescaler is used
  [(Osc. Freq. / Prescaler) / Ref. Freq.] = [(12.8MHz / 8) / 6.25kHz] = 256



- Ex 2) FRC = 1, In case of 15bits Program, Fosc = 12.8MHz and 1/8 prescaler is used
  [Osc. Freq. / Ref. Freq.] = [12.8MHz / 6.25kHz] = 2048



NOTE: The PMC bit is Program Mode Control Bit, if [1], the R-Counter will be Enabled

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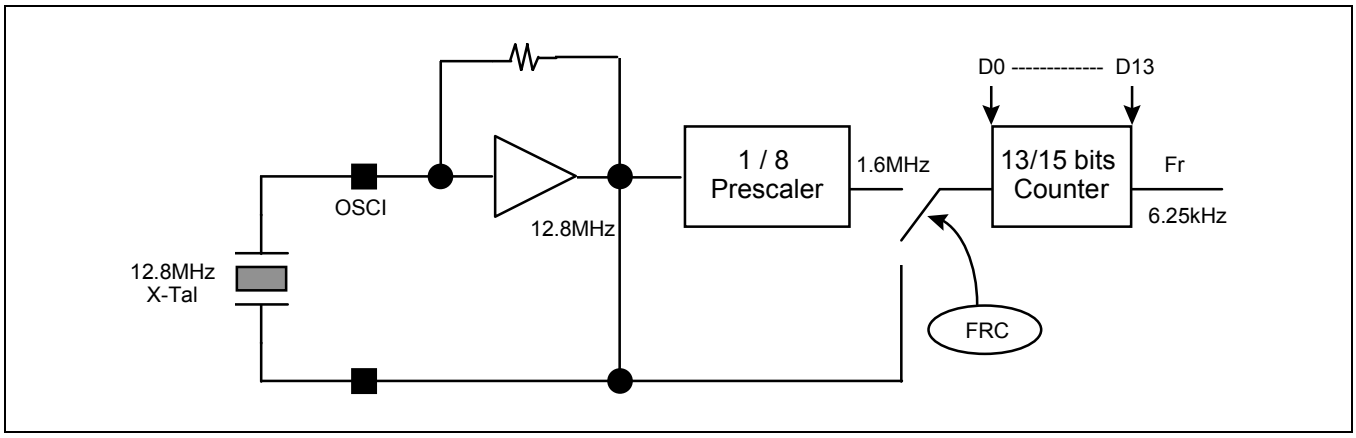

Figure 3. The architecture of R-Count Divider

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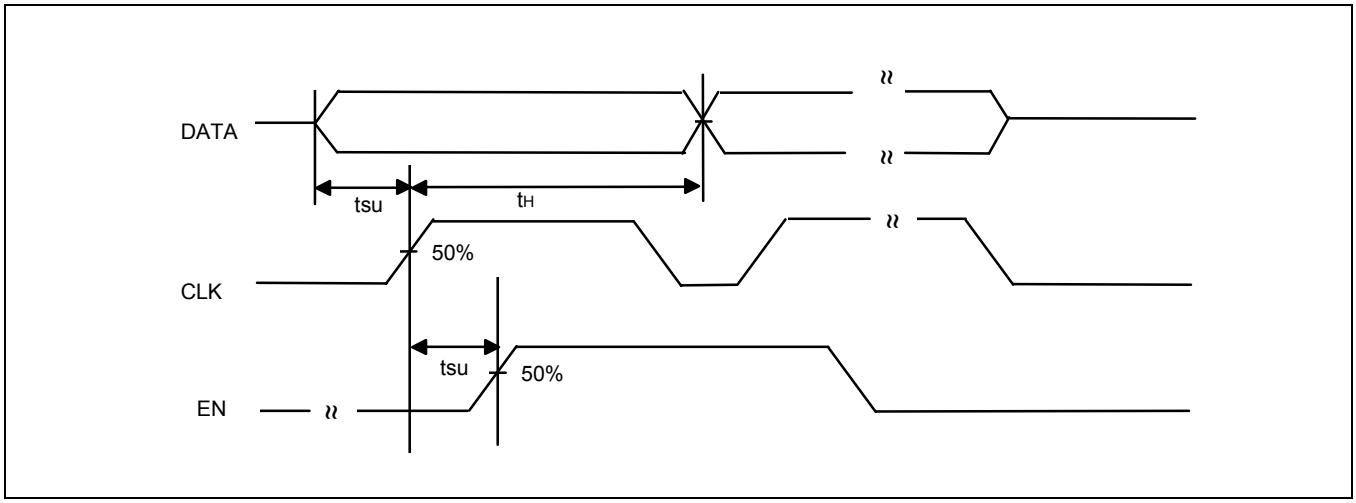

Figure 4. Serial DATA Input Timing

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PHASE DETECTOR / LOCK DETECTOR

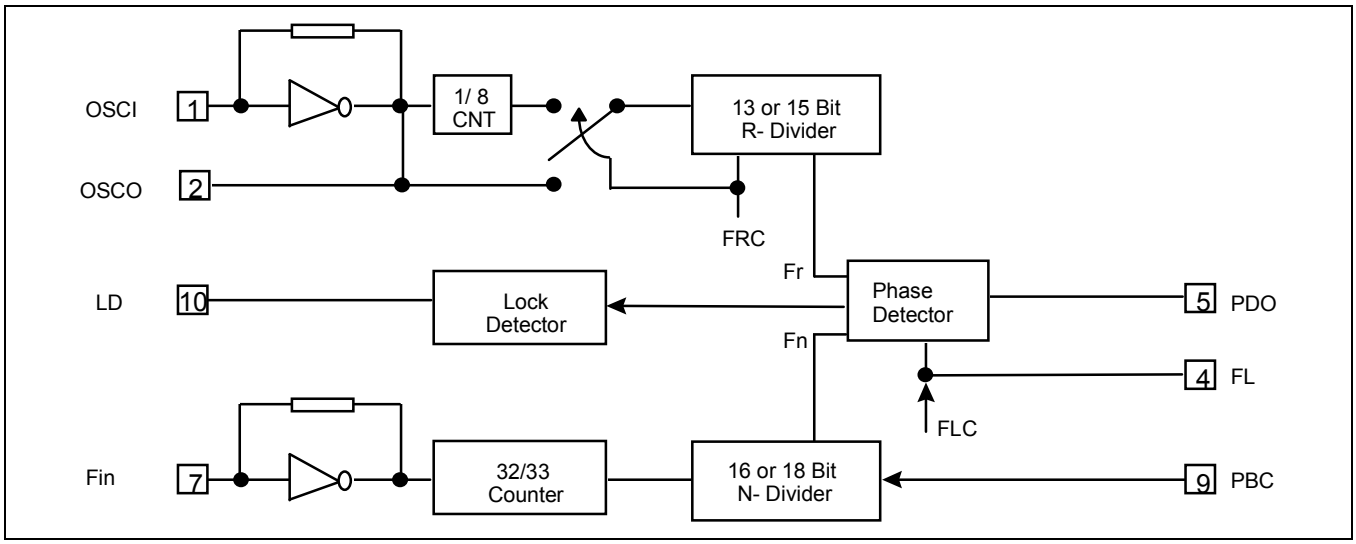

Figure 5. Phase Detector / Lock Detector

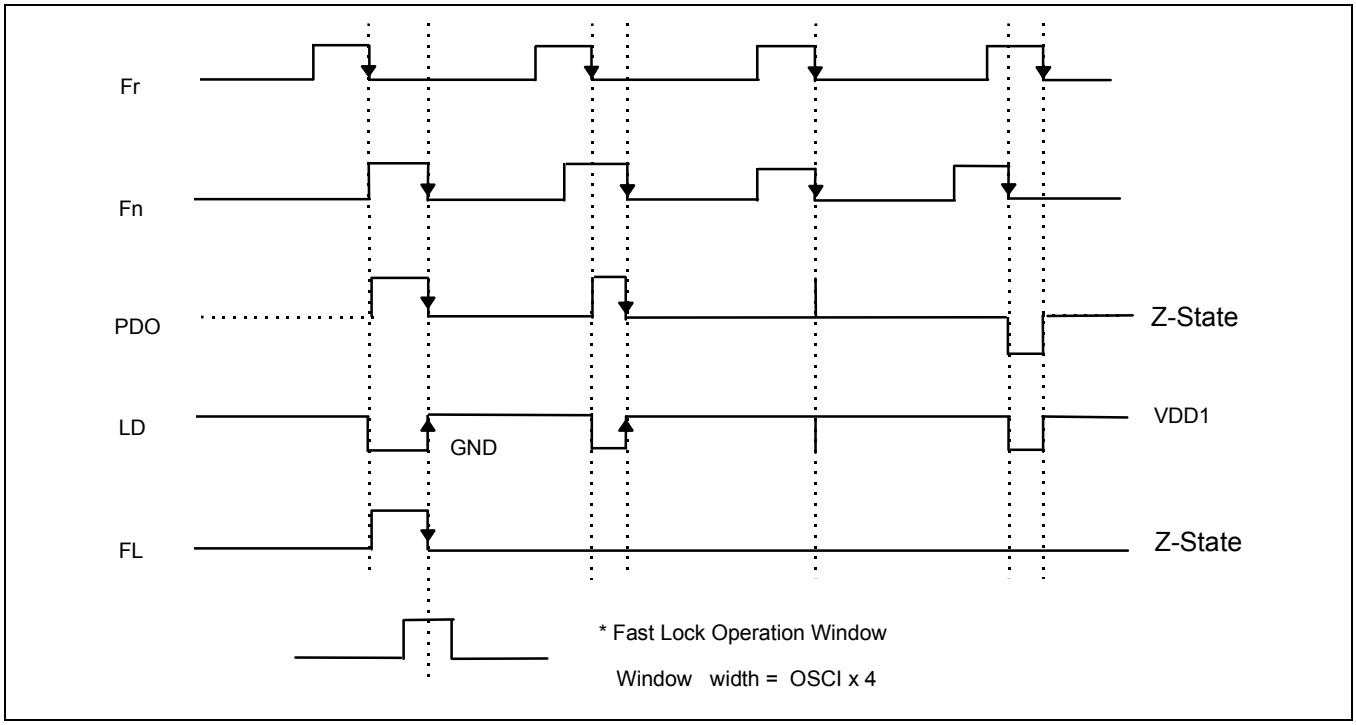

Figure 6. Figure 5-2. Phase Detector / Lock Detector / Fast Lock Output Waveforms

NOTES:

1. Phase detector always compares the Phase difference of N-counter with R-counter, and generates High or Low State as much as the phase difference
2. The LD output is set to Low level same as Phase detector error width

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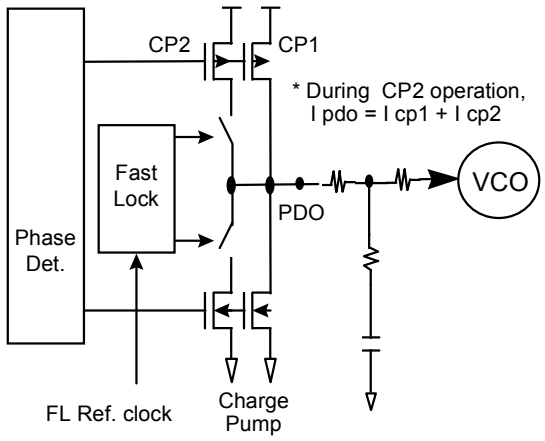
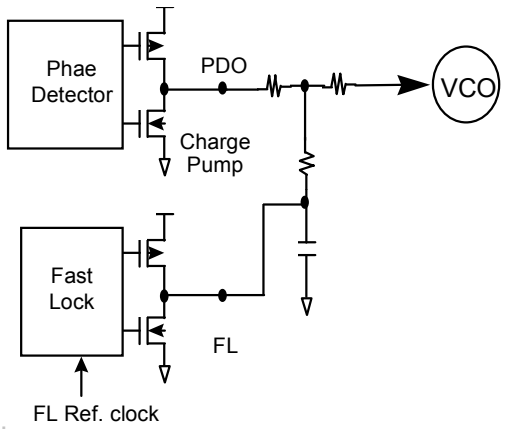
FAST LOCK

The Fast lock can gives faster Acquisition time when the KS8809 starts up.

If Fast Lock signal was generated one time, this circuitry do not operate again even though PLL goes into unlock state.

KS8809 has two kinds of Fast lock ; one is to control the Loop band width of Loop filter, the other one is to control the charge pump current.

Mode 1	Mode 2
	
• CP1: Default charge pump output TR • CP2: When FLC = High, CP2 goes [On] state, the Timming & Phase is just same as FL signal • Mode 1 does not used FL pin, only increase PDO output current same as the width of 1'st phase error	• Expeding a Loop Band width during Fast Lock operation • When the FLC pin set to High level, this function will be available

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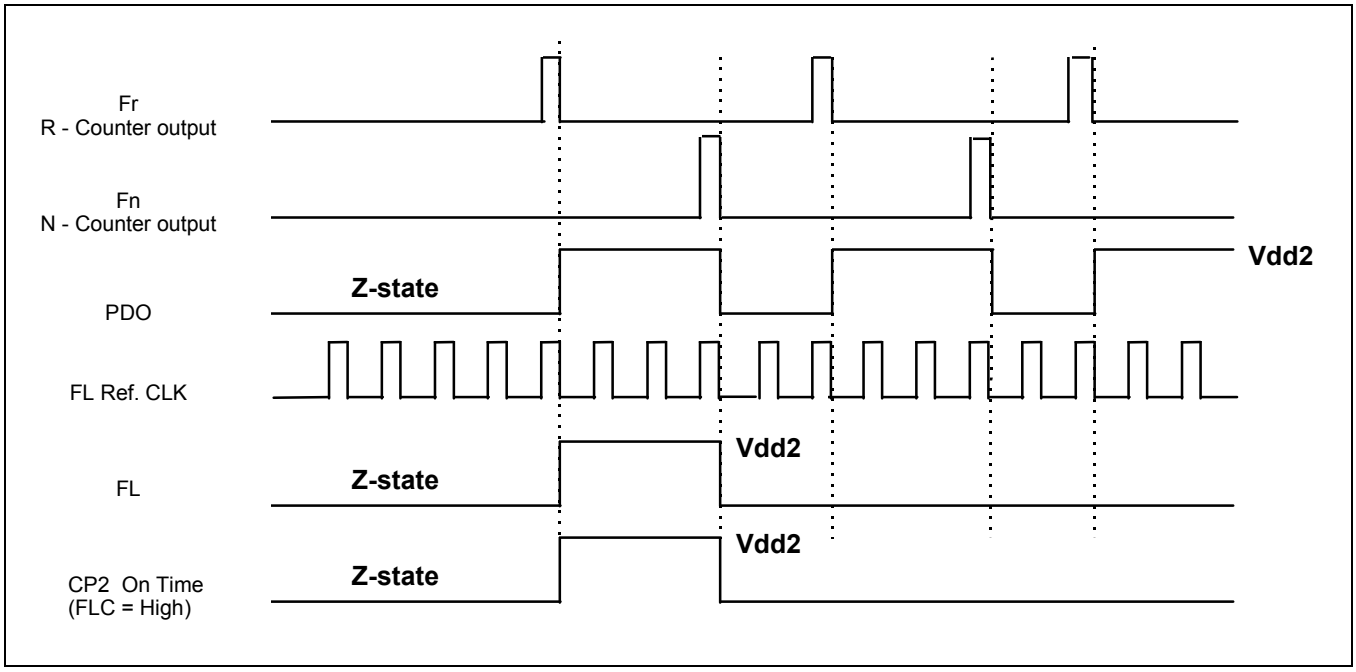

Figure 7.

APPLICATION CIRCUIT

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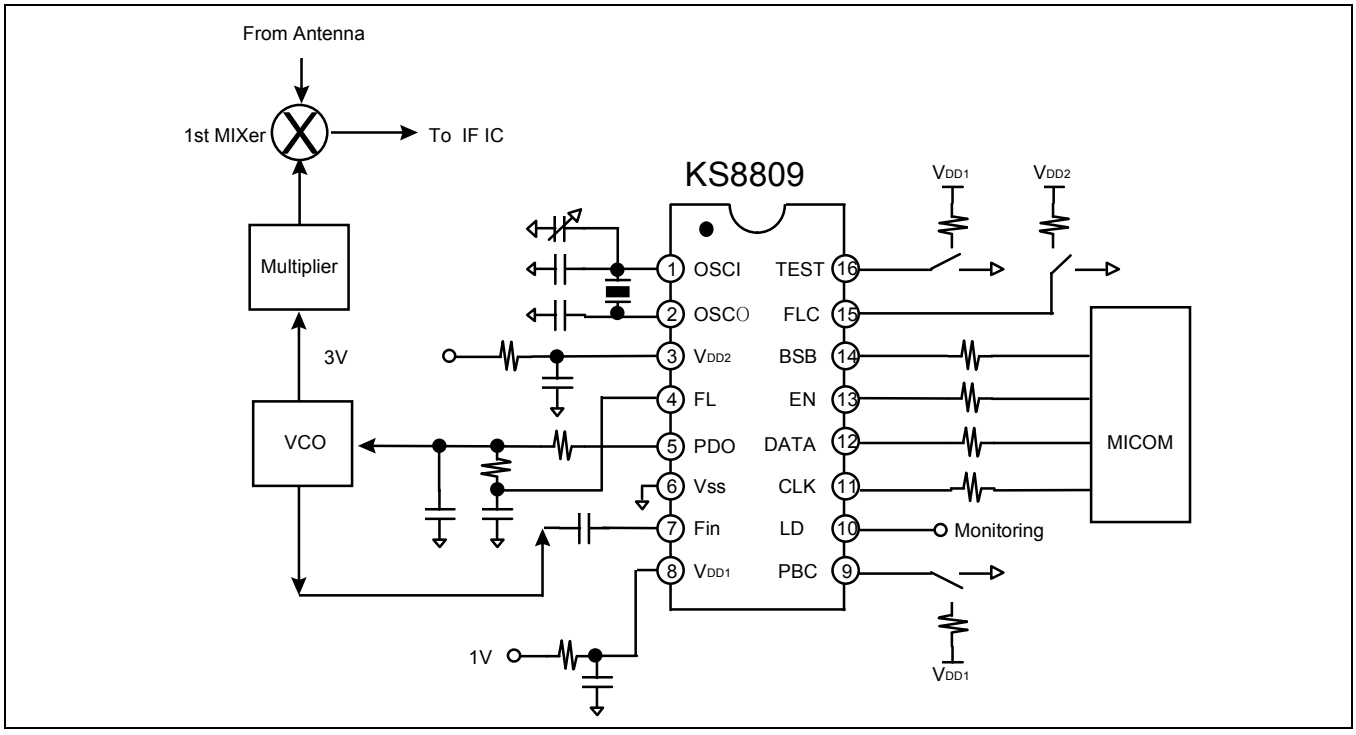

Figure 8.

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NOTES

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