california micro devices

Triple Linear Voltage Regulator for DDR-I Memory and CPU

Features

- Fully integrated power solution for a CPU/SOC core and DDR-I memory ICs
- Lowest system cost and smallest footprint with just three external output capacitors
- Three linear regulators for V_{CORE} (1.5A), V_{DDQ} (1.5A), and V_{TT} (0.5A, source-sink)
- V_{DDQ} = 2.5V, $V_{TT} = V_{DDQ}/2 \pm 25$mV
- V_{CORE} is adjustable, with a default output of 1.5V
- Over-temperature and reverse current protection
- Overcurrent protection for all regulators
- PSOP-8 package with integrated heat spreader
- Lead-free version available

Applications

- Core CPU and DDR-I memory power for:
  - Set Top Boxes, DVD Players, Games
  - Digital TVs, Flat Panel Displays
  - Printers, Digital Projectors
  - Embedded systems
  - Communications systems

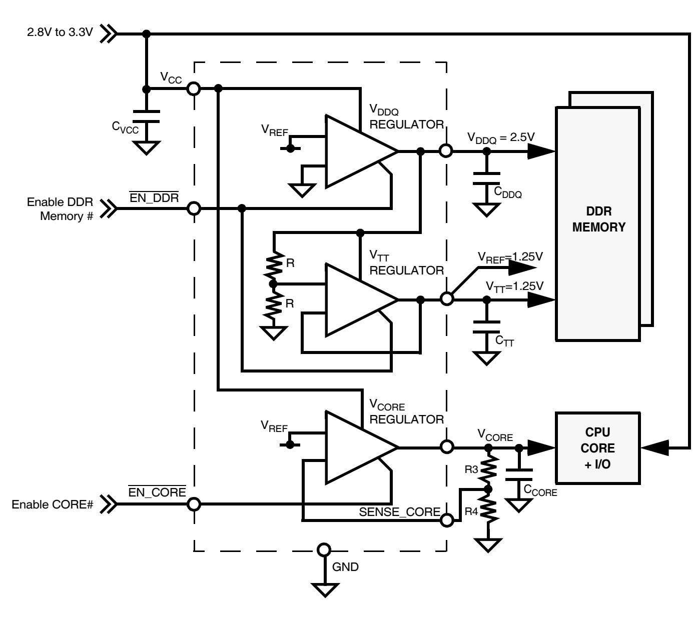
Product Description

The CM3132 provides an integrated power solution for a CPU core and DDR-I memory for consumer and other embedded applications. It features three independent linear regulators for V_{CORE}, V_{DDQ} and V_{TT} supply regulation. The default voltage for V_{CORE} is 1.5V. The SENSE_CORE pin can be tied to GND for the default voltage, or through a resistor divider for setting the CPU core in the range 1.2V to 1.8V. V_{DDQ} is internally set to 2.50V and the V_{TT} voltage is always half the V_{DDQ} voltage. A capacitor should be connected to each of the three outputs.

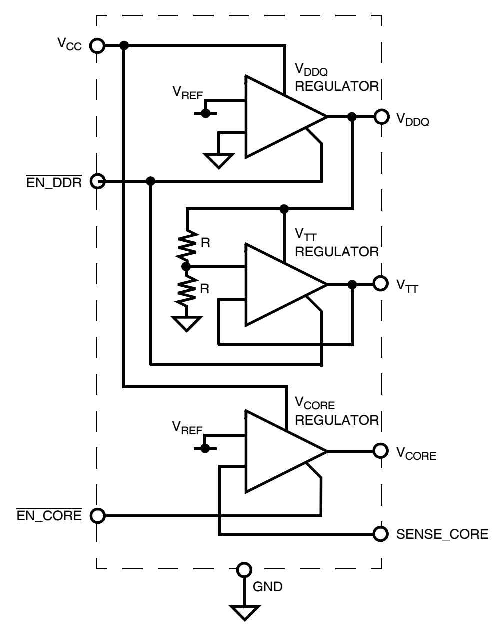
There are two enable pins, $\overline{\text{EN\_CORE}}$ and $\overline{\text{EN\_DDR}}$. When $\overline{\text{EN\_CORE}}$ is set high, the CORE regulator is disabled. When $\overline{\text{EN\_DDR}}$ is set high, the two DDR regulators are disabled to minimize overall system power dissipation when memory is in standby mode. These two enable pins allow power sequencing of the DDR and CORE regulator blocks independently.

The CM3132 is available in a PSOP-8 package that has excellent thermal dissipation. It is available with optional lead-free finishing.

Typical Application Circuit

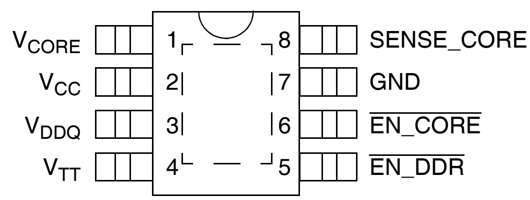


Circuit Schematic



PACKAGE / PINOUT DIAGRAM

TOP VIEW



8-Lead PSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS		
PSOP-8 LEAD	NAME	DESCRIPTION
1	V_{CORE}	V_{CORE} output.
2	V_{CC}	Input supply.
3	V_{DDQ}	V_{DDQ} output.
4	V_{TT}	V_{TT} output for termination resistors or V_{REF}
5	$\overline{\text{EN\_DDR}}$	Enable DDR power. Active low input.
6	$\overline{\text{EN\_CORE}}$	Enable V_{CORE}. Active low input.
7	GND	Ground reference.
8	SENSE_CORE	Sense input. Adjusts V_{CORE} output voltage using external resistor divider. When tied to GND, V_{CORE} = 1.5V.
PAD	GND	Tied to ground reference.

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Leads	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	PSOP-8	CM3132-02SB	CM3132 02SB	CM3132-02SH	CM3132 02SH

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD (Human Body Model)	±2000	V
Pin Voltages V_{CC} $\overline{EN\_CORE}$, $\overline{EN\_DDR}$, SENSE_CORE V_{DDQ}, V_{TT}	 [GND - 0.6] to [+6.5] [GND - 0.6] to [V_{CC} + 0.6] [GND - 0.6] to [V_{CC} + 0.6]	 V V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 0 to +85 0 to +125	 °C °C

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Ambient Operating Temperature Range	0 to +85	°C
1. V_{DDQ} Regulator		
DDR-I Supply Voltage V_{CC}	[V_{DDQ} + 0.3] to 3.6	V
Load Current	0 to 1500	mA
C_{CC}, C_{DDQ}	10, 10	µF
2. V_{TT} Regulator		
DDR-I Supply Voltage V_{DDQ}	2.3 to 2.8	V
DDR-I Load Current	0 to ±500	mA
C_{TT}	47	µF
3. V_{CORE} Regulator		
Core Supply Voltage V_{CC}	[V_{DDQ} or V_{CORE} + 0.3] to 3.6	V
DDR-I Load Current	0 to 1500	mA
C_{CORE}	10	µF

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
General Parameters						
T_{OVER}	Shutdown Junction Temperature		-	150	-	°C
T_{HYST}	Junction Temp Hysterisis	IC in shutdown	-	25	-	°C
I_{CCN}	Normal Mode V_{CC} Supply Current	$\overline{\text{EN\_DDR}}$ = logic "0", $\overline{\text{EN\_CORE}}$ =logic "0"		400	800	µA
I_{CCQ}	Shutdown Mode V_{CC} Supply Current	$\overline{\text{EN\_DDR}}$ = logic "1", $\overline{\text{EN\_CORE}}$ =logic "1"		2	10	µA
$I_{SENSE\ IN}$	SENSE_CORE Input Current	V_{SENSE_CORE}=0.6V		0.1	1.0	µA
V_{IH}	$\overline{\text{EN\_DDR}}$, $\overline{\text{EN\_CORE}}$ Input High Threshold	V_{CORE}=3.3V	2.0			V
V_{IL}	$\overline{\text{EN\_DDR}}$, $\overline{\text{EN\_CORE}}$ Input Low Threshold	V_{CORE}=3.3V			0.4	V
UVLO	Under Voltage Lock-Out	I_{DDQ} = 10mA			1.8	V
t_{RISE}	V_{DDQ}, V_{CORE} Rise TIme	V_{CC} = 3.3V, C_{LOAD} = 10µF		0.5		ms
V_{DDQ} Regulator Parameters						
$V_{CC\ MIN}$	Input Voltage	V_{DDQ} = 2.5V, I_{DDQ} = 1.5A, Note 2	2.80			V
$V_{DDQ\ DEF}$	Default Output Voltage	I_{DDQ} = 0.01A, 2.8V ≤ V_{CC} ≤ 3.6V, Note 2	2.45	2.50	2.55	V
$V_{DDQ\ LD}$	Load Regulation	T_A = 25°C, V_{CC} = 3.3V, 0.01A ≤ I_{DDQ} ≤ 1.5A, Note 2	-	-	2.5	%
$V_{DDQ\ LINE}$	Line Regulation	T_A = 25°C, I_{DDQ} = 0.01A, 2.8V ≤ V_{CC} ≤ 3.6V, Note 2	-1.0	-	1.0	%
$e_{N\ DDQ}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{DDQ} = 10µF		49		µVrms
$I_{DDQ\ LIM}$	Current Limit	Note 2	1.7	2.0		A
$I_{DDQ\ SC}$	Short Circuit Current	V_{DDQ} < 0.3V		0.5		A

ELECTRICAL OPERATING CHARACTERISTICS (CONT'D) (SEE NOTE1)

V_{TT} Regulator Parameters						
V_{TT}	Output Voltage Range	V_{DDQ} = 2.5V, I_{TT} = 0.01A, I_{DDQ} = 0A	1.20	1.25	1.30	V
$V_{TT\ REF}$	Output Voltage Range	V_{CC} = 0V, V_{DDQ} = 2.500V, I_{TT} = 0.01A	1.225	1.250	1.275	V
$V_{TT\ LD}$	Load Regulation	T_A = 25°C, V_{DDQ} = 2.5V, 0.01A $\leq I_{TT} \leq \pm$0.5A	-1.0	-	1.0	%
$e_{N\ TT}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{TT} = 10µF		51		µVrms
$I_{TT\ LIM}$	Current Limit		0.6	0.8		A
$I_{TT\ SC}$	Short Circuit Current	V_{TT} < 0.7V		0.3		A
V_{CORE} Regulator Parameters						
$V_{CC\ MIN}$	Input Voltage	V_{CORE} = 1.5V, I_{CORE} = 1.5A, SENSE_CORE = 0V, Note 3	2.2			V
$V_{CORE\ DEF}$	Default Output Voltage Range	V_{CC} = 3.3V, I_{CORE} = 0.01A, SENSE_CORE = 0V	1.45	1.50	1.55	V
$V_{CORE\ ADJ}$	Adjustable Output Voltage Range	V_{CC} = 3.3V, SENSE_CORE from resistors R3 & R4, Note 4	1.2		1.8	V
$V_{CORE\ LD}$	Load Regulation	T_A = 25°C, V_{CC} = 3.3V, 0.01A $\leq I_{CORE} \leq \pm$1.5	-	-	2.5	%
$V_{CORE\ LINE}$	Line Regulation	T_A = 25°C, 2.8V $\leq V_{CC} \leq$ 3.6V, I_{CORE} = 0.01A	-1.0	-	1.0	%
$e_{N\ CORE}$	Output Noise Voltage	BW = 10Hz - 100kHz, C_{CORE} = 47µF		59		µVrms
$I_{CORE\ LIM}$	Current Limit		1.7	2.0		A
$I_{CORE\ SC}$	Short Circuit Current	V_{CORE} < 0.3V		0.5		A

Note 1: All parameters specified at T_A = 0°C to +85°C unless otherwise noted.

Note 2: Note that the I_{DDQ} current specified is the load current output from the V_{DDQ} pin. V_{DDQ} also supplies current internally to the V_{TT} regulator when it is sourcing current. The maximum source current can be up to 0.5A.The maximum total current from the V_{DDQ} regulator is the external V_{DDQ} current I_{DDQ} added to the maximum V_{TT} sourcing current I_{TT}. All load currents are specified as such, but the V_{DDQ} current limit is specified at a current just above the total maximum current.

Note 3: V_{CORE} regulator only. Refer to V_{DDQ} regulator parameters for V_{DDQ} regulator.

Note 4: $V_{CORE} = 1.15V \times (1 + \frac{R3}{R4})$

VCC(1)	$\overline{EN\_DDR}$	$V_{DDQ\ OUT}$	$V_{TT\ OUT}$
2.8V to 3.6V	Low	V_{DDQ}	V_{DDQ} / 2
X	High	0V	0V

Table 1: Truth Table for CM3132

Performance Information

Power Supply Ripple Rejection
C_{CC} = 10μF, V_{CC} = 3.3V, I_{LOAD} = 50mA, PSRR measured with 50mV pk-pk sin wave on V_{CC}.

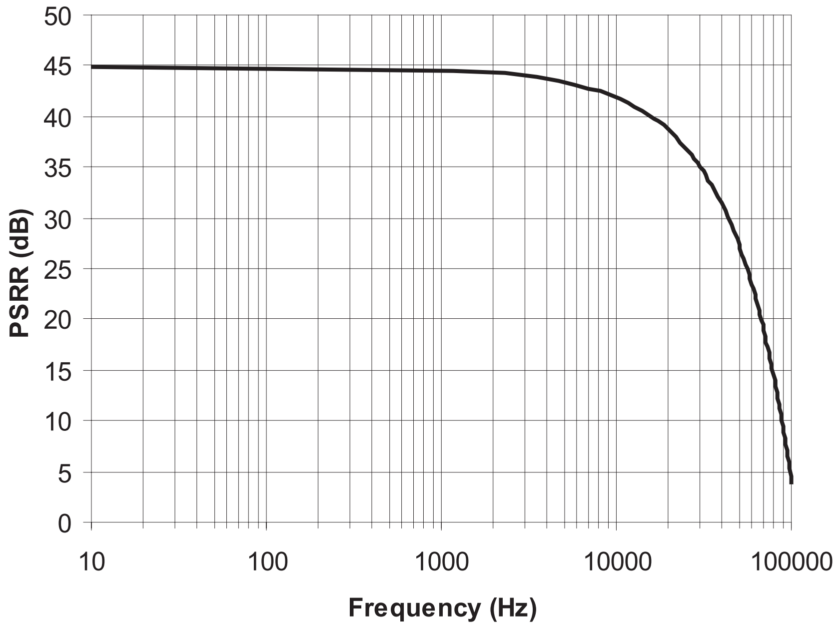


Figure 1. V_{CORE} PSRR (V_{CORE} = 1.5V)

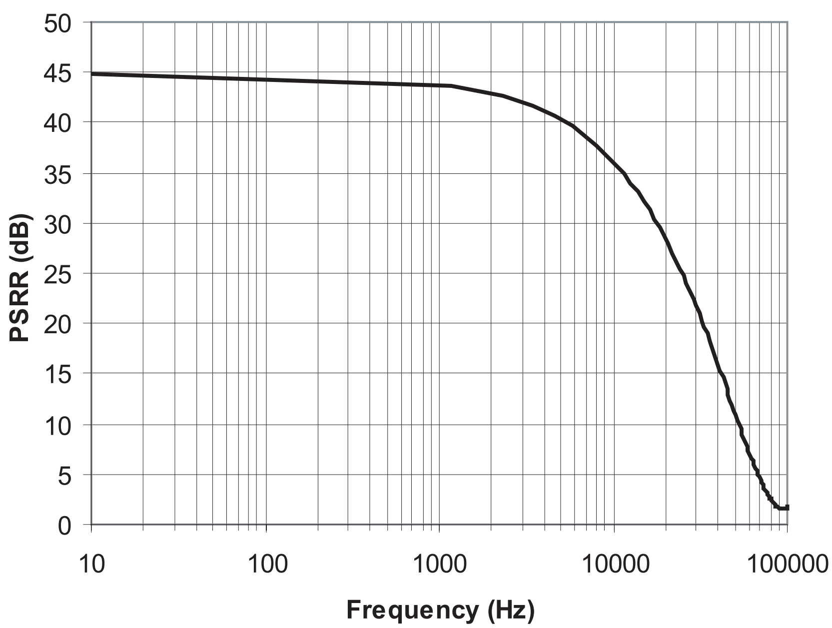


Figure 2. V_{DDQ} PSRR (V_{DDQ} = 2.5V)

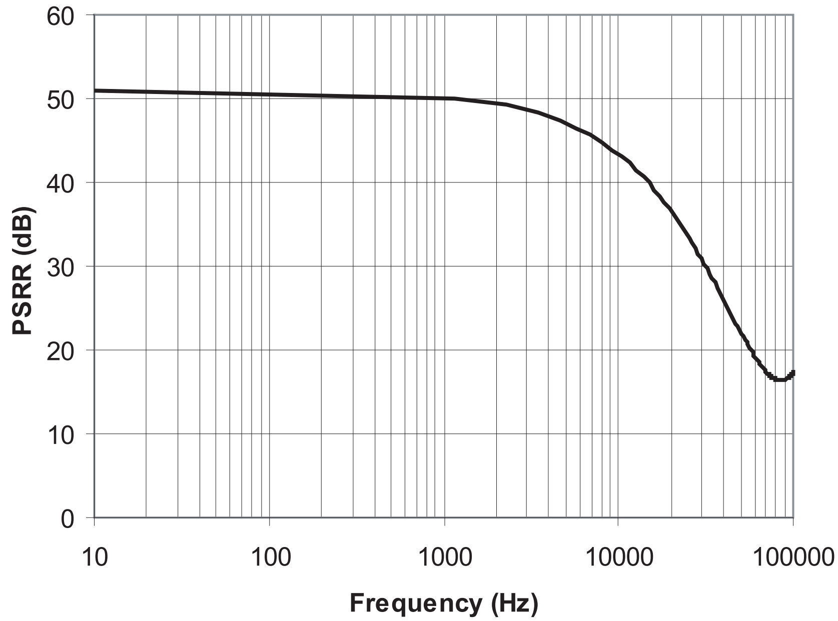


Figure 3. V_{TT} PSRR (V_{TT} = 1.25V)

Performance Information (cont'd)

Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D\ (\ \theta_{JC}\ ) + P_D\ (\ \theta_{CA}\ )$$

$$= T_{AMB} + P_D\ (\ \theta_{JA})$$

When a CM3132-02SB (PSOP-8) is mounted on a double-sided printed circuit board with two square inches of copper allocated for "heat spreading," the resulting θ_{JA} is 40°C/W. Based on the over temperature limit of 150° C with an ambient of 70°C, the available power of this package will be:

$$P_D = \frac{150°\ C - 70°\ C}{40°\ C/\ W} = 2W$$

PCB Layout Considerations

The CM3132-02SB/SH has a heat spreader attached to the bottom of the PSOP-8 package in order for heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. The drawing below shows the recommended PCB layout. Note that there are six vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can cause blockage of the solder. The ground and power planes should be at least 2 sq in. of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3132 package to ambient, θ_{JA}, of around 40°C/W.

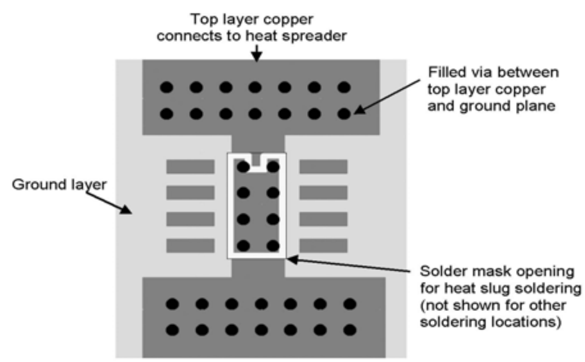


Figure 4. Recommended Heat Sink PCB Layout

Application Information

Other Applications

The CM3132 can be used without any external resistors if a core voltage of 1.5V is required, the SENSE_CORE pin is connected to GND.

In applications where a reference voltage (V_{REF}) is required, the V_{TT} pin can be used. The V_{TT} output pin has an error relative to $V_{DDQ}/2$ of up to ±25mV, which is well within most DDR system specs of ±50mV. This is because the V_{TT} output internally tracks the V_{DDQ} output very closely due to the matched on-chip resistors R that tap down from the V_{DDQ} rail, and the low offset voltage of the V_{TT} regulator. It is recommended that the V_{REF} trace be connected directly to the V_{TT} pin, as shown in Figure 5, to eliminate noise and ripple on the V_{TT} trace caused by current switching.

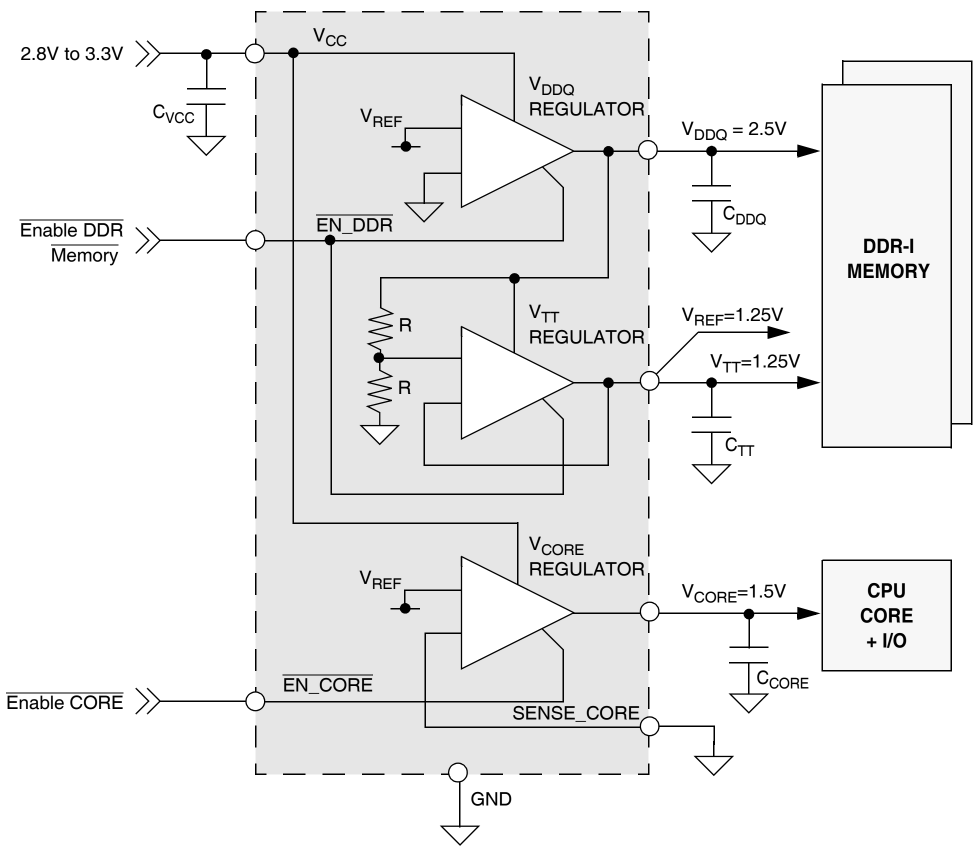
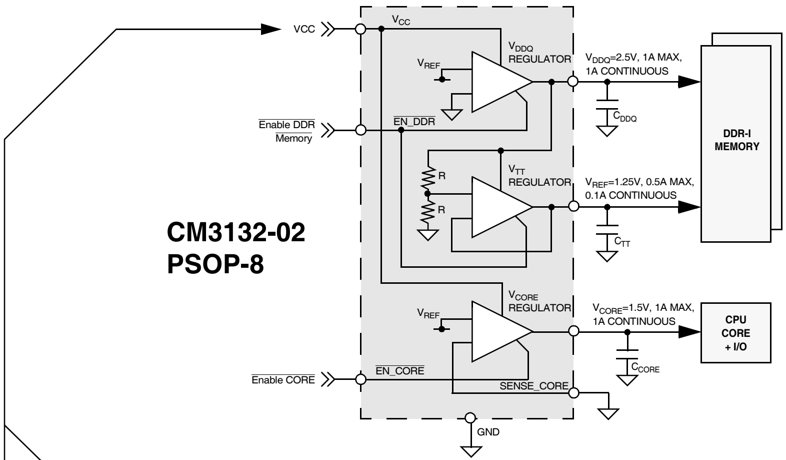


Figure 5. Minimal cost solution for CM3132 supplying DDR memory and core CPU.

Application Information (cont'd)

1 PSOP-8 IC drives 1-DIMM single channel DDR-I and CPU Core VCORE rail



With 3.3V_{CC} @ 1A (V_{DDQ}), 0.1A (V_{TT}), 1A (V_{CORE}),
P_D = (3.3-2.5) * 1.05 + (2.5-1.25) * 0.1 + (3.3-1.5) * 1 = 0.84 + 0.125 + 1.8 = **2.765W**

With 3.0V_{CC} @ 1A (V_{DDQ}), 0.1A (V_{TT}), 1A (V_{CORE}),
P_D = (3.0-2.5) * 1.05 + (2.5-1.25) * 0.1 + (3.0-1.5) * 1 = 0.525 + 0.125 + 1.5 = **2.15W**

With 2.8V_{CC} @ 1A (V_{DDQ}), 0.1A (V_{TT}), 1A (V_{CORE}),
P_D = (2.8-2.5) * 1.05 + (2.5-1.25) * 0.1 + (2.8-1.5) * 1 = 0.315 + 0.125 + 1.3 = **1.74W**

Figure 6. Power Dissipation Calculations

$T_{JUNC} = T_{AMB} + P_D * (\theta_{JA})$

$P_D = (T_{AMB} - T_{JUNC}) / (\theta_{JA})$

P_D = (Vcc-2.5)*Iddq + (2.5-1.25)*0.1 + (Vcc-Vcore)*Icore
P_D - (Vcc-2.5)*Iddq - 0.125 = (Vcc-Vcore)*Icore
Icore = [P_D - (Vcc-2.5)*Iddq - 0.125] / (Vcc-Vcore)

	Derating (degC/W)	40	40	40	40	40	40	40	40	40
	Ambient (degC)	85	85	85	60	60	60	40	40	40
θ_{JA}= 40 °C/W	Max Power (W)	1.6	1.6	1.6	2.3	2.3	2.3	2.8	2.8	2.8
	Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8
	Min Vcore (V)	1.5	1.5	1.5	1.5	1.4	1.0	1.5	1.2	1.1
	Max Iddq (A)	1.0	0.8	0.5	1.0	1.0	1.0	1.0	1.0	1.0
	Max Icore (A)	0.4	0.7	1.0	0.7	1.0	1.0	1.0	1.0	1.4
	Derating (degC/W)	60	60	60	60	60	60	60	60	60
	Ambient (degC)	85	85	85	60	60	60	40	40	40
θ_{JA}= 60 °C/W	Max Power (W)	1.1	1.1	1.1	1.5	1.5	1.5	1.8	1.8	1.8
	Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8
	Min Vcore (V)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.4
	Max Iddq (A)	0.3	0.5	0.6	1.0	0.7	0.5	0.5	0.7	1.0
	Max Icore (A)	0.4	0.5	0.6	0.3	0.7	0.9	0.7	1.0	1.0
	Derating (degC/W)	80	80	80	80	80	80	80	80	80
	Ambient (degC)	85	85	85	60	60	60	40	40	40
θ_{JA}= 80 °C/W	Max Power (W)	0.8	0.8	0.8	1.1	1.1	1.1	1.4	1.4	1.4
	Vcc (V)	3.3	3.0	2.8	3.3	3.0	2.8	3.3	3.0	2.8
	Min Vcore (V)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
	Max Iddq (A)	0.3	0.3	0.3	0.5	0.5	0.5	0.5	0.7	0.5
	Max Icore (A)	0.2	0.4	0.5	0.3	0.5	0.7	0.5	0.6	0.8

Figure 7. Power Derating Table

Mechanical Details

PSOP-8 Mechanical Specifications

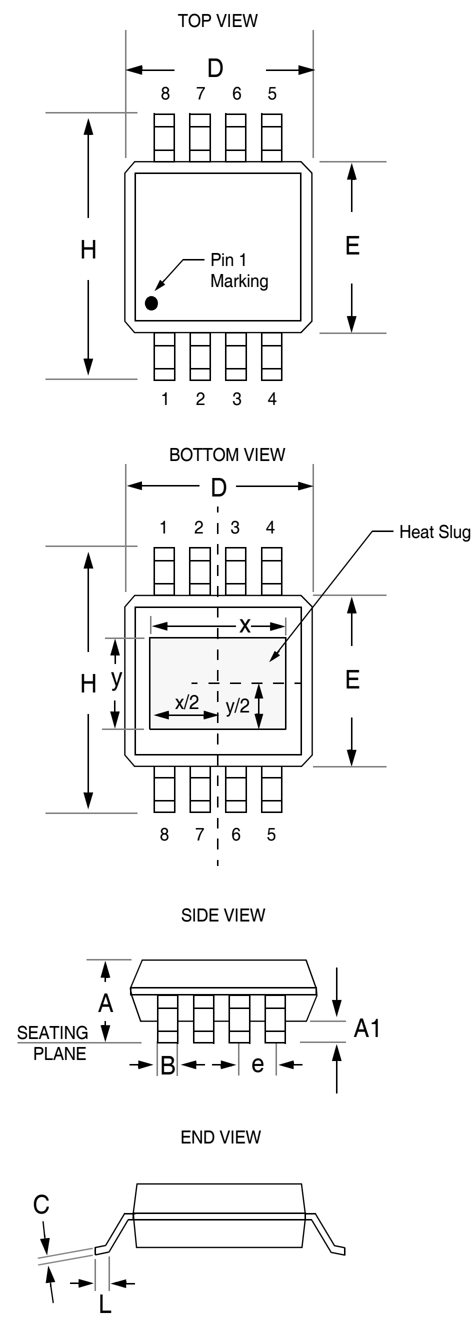
Dimensions for CM3132 devices packaged in an 8-lead PSOP package with a heatspreader are shown below.

PACKAGE DIMENSIONS				
Package	PSOP-8			
Leads	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.30	1.62	0.051	0.064
A_1	0.03	0.10	0.001	0.004
B	0.33	0.51	0.013	0.020
C	0.18	0.25	0.007	0.010
D	4.83	5.00	0.190	0.197
E	3.81	3.99	0.150	0.157
e	1.02	1.52	0.040	0.060
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
x**	3.30	3.81	0.130	0.150
y**	2.29	2.79	0.090	0.110
# per tube	100 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: inches				

* This is an approximate number which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for PSOP-8