Drivers for Large LCD Panels

6bit RSDS™ Source Driver

BU95408

No.10043EAT04

●Description

ROHMLCD drivers for large panels are display drivers optimized for large LCDs in a variety of applications, including desktop PCs, laptops, and TVs. The broad lineup is offered in low amplitude differential transmission interface type (RSDS™) featuring low EMI, 6bit gradation precision, and different output configurations (720 and up) for wide compatibility.

●Features

1) 684/690/702/720 output channels
2) 6bit 9pair RSDS™ inputs
3) Dot & n-line inversion available
4) Built-in 2ch repair amplifiers
5) γ correction is possible
6) Built-in input data reversing function (INV)
7) Output voltage range: AV_{SS}+0.1V ~ AV_{DD}−0.1V
8) High speed data transfer: $f_{CLK(MAX)}$=85MHz
9) Logic power supply voltage (DV_{DD}) : 2.3 ~ 3.6V
10) Driver power supply voltage (AV_{DD}) : 8.0 ~ 13.5V
11) Package: COF48

●Applications

TFT LCD Panels

●Line up matrix

	BU95101	BU95303	BU95306	BU95408
Number of outputs	384	384 / 414 / 420 / 432	600 / 618 / 630 / 642	684 / 690 / 702 / 720

●Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Logic power supply voltage	DV_{DD}	-0.3 ~ +4.5	V
Driver power supply voltage	AV_{DD}	-0.3 ~ +14.0	V
Logic input voltage	V_{I1}	-0.3 ~ DV_{DD}+0.3	V
Logic output voltage	V_{O1}	-0.3 ~ DV_{DD}+0.3	V
Driver input voltage	V_{I2}	-0.3 ~ AV_{DD}+0.3	V
Driver output voltage	V_{O2}	-0.3 ~ AV_{DD}+0.3	V
Storage temperature range	T_{stg}	-55 ~ +125	℃

●Recommended operating range

Parameter	Symbol	Ratings	Unit
Logic power supply voltage	DV_{DD}	+2.3 ~ +3.6	V
Driver power supply voltage	AV_{DD}	+8.0 ~ +13.5	V
γ-correction reference voltage	V_0 ~ V_6	0.5 AV_{DD} ~ AV_{DD}-0.1	V
	V_7 ~ V_{13}	0.1 ~ 0.5 AV_{DD}	V
Driver output voltage	V_O	0.1 ~ AV_{DD}-0.1	V
Output load capacitance	C_L	80	pF
Maximum clock frequency	$f_{CLK(MAX)}$	85	MHz
Operating temperature range	T_{opr}	-10 ~ +85	℃

* AV_{SS}=DV_{SS}=0V

●Electrical characteristics (DC)

(Unless otherwise noted, Ta=−10 ~ +85℃, DV_{DD}=2.3 ~ 3.6V, AV_{DD}=8.0 ~ 13.5V, DV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Limits			Unit	Conditions	
		Min.	Typ.	Max.			
Logic Part							
Logic supply current	I_{DDL}	−	−	8	mA	DV_{DD}=3.3V, Data=00h-3Fh(dot), fclk=65MHz, fstb=50kHz, 1Line-inverison	
Input “H” voltage	V_{1H}	0.7DV_{DD}	−	DV_{DD}	V		R/L,SFTR,INV,SFTL, POL,STB,SEL0,SEL1, LPC0, LPC1
Input “L” voltage	V_{1L}	0	−	0.3DV_{DD}	V		
Input “H” current	I_{1H1}	−	−	+1	μA	V_{IN}=DV_{DD}	Dxx, SFTR, POL, INV, SFTL,CLK,STB,R/L
Input “L” current	I_{1L1}	-1	−	−	μA	V_{IN}=DV_{SS}	
Input “H” current 2	I_{1H2}	−	20	40	μA	V_{IN}=DV_{DD} DV_{DD}=3.3V	LPC0,LPC1 Built-in Pull down R
Input “L” current 2	I_{1L2}	-3	−	+3	μA	V_{IN}=DV_{SS}	
Input “H” current 3	I_{1H3}	-3	−	+3	μA	V_{IN}=DV_{DD}	SEL0,SEL1 Built-in Pull up R
Input “L” current 3	I_{1L3}	-40	-20	−	μA	V_{IN}=DV_{SS} DV_{DD}=3.3V	
Output “H” voltage	V_{OH}	DV_{DD}-0.5	−	−	V	I_{OH}=−1.0mA	SFTR,SFTL
Output “L” voltage	V_{OL}	−	−	0.5	V	I_{OL}=1.0mA	
Driver part							
Driver supply current	I_{DDA}	−	−	14	mA	AV_{DD}=12V, Data=00h-3Fh(dot), fclk=65MHz, fstb=50kHz,1Line-inverison, noLoad, LPC:normal	
γ correction resistance	$R_{\gamma UP}$	0.7Typ	11.27	1.3Typ	kΩ	V0 ~ V6	
	$R_{\gamma LOW}$	0.7Typ	11.27	1.3Typ	kΩ	V7 ~ V13	
Output voltage deviation	V_{OD1} *1	−	±25	−	mV	AV_{DD}=12V Yout=0.1V~1.5V,Yout=10.5V~11.9V	
		−	±15	±25	mV	AV_{DD}=12V, Yout=1.5V~10.5V	
Output swing voltage Deviation	V_{RMS} *2	−	±25	−	mV	AV_{DD}=12V Yout=0.1V~1.5V,Yout=10.5V~11.9V	
		−	±5	±10	mV	AV_{DD}=12V, Vout=1.5V~10.5V	
Output voltage deviation 2 (between chips)	V_{OD2} *3	−	−	±7.5	mV	AV_{DD}=12V, Data=32-gray	
Repair input voltage	V_{1NB}	0.1	−	AV_{DD}-0.1	V		IREP1,2
Repair input “H” current	I_{1BH}	-1	−	+1	μA	V_{IN}=AV_{DD}=13.5V	
Repair input “L” current	I_{1BL}	-1	−	+1	μA	V_{IN}=AV_{SS}	
Driver output “H” current	I_{VOHY}	−	−	-0.4	mA	Y1 ~ Y720, AV_{DD}=12V, Vx=6 V,Yout=11V	
	I_{VOHR}	−	−	-0.8	mA	OREP1,2 ,AV_{DD}=12V, Vx=6 V, Yout=11V	
Driver output“L” current	I_{VOLY}	0.4	−	−	mA	Y1 ~ Y720, AV_{DD}=12V, Vx=6 V,Yout=1V	
	I_{VOLR}	0.8	−	−	mA	OREP1,2 ,AV_{DD}=12V, Vx=6 V, Yout=1V	
RSDS™ input part							
RSDS™ input “H” voltage	V_{IHRSDS}	100	200	−	mV	VCM_{RSDS}=+1.2V *4	$CLK_{P/N}$,$D_{XXP/N}$ (X=0,1,2)
RSDS™ input “L” voltage	V_{ILRSDS}	−	-200	-100	mV		
RSDS™ common input voltage	V_{CMRSDS}	0.4	−	DV_{DD}-1.2	V	V_{DIFF}=200mV *5	

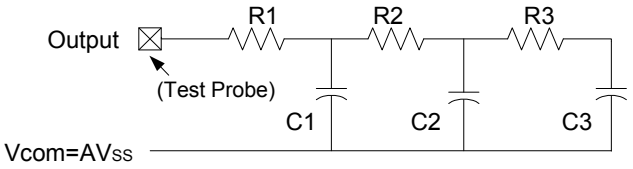
*1 V_{OD1}=measured output voltage - averaged output voltage of all outputs
*2 V_{RMS}=measured output swing voltage - averaged output swing voltage of all outputs
*3 V_{OD2}=averaged output voltage - target value
*4 VCM_{RSDS} = ($VCLK_P$+$VCLK_N$)/2 or (VD_{XXP}+VD_{XXN})/2
*5 V_{DIFF} = $VCLK_P$- $VCLK_N$ or VD_{XXP}-VD_{XXN}

●Electrical Characteristics (AC)

(Unless otherwise noted, Ta=−10 ~ +85℃, DV_{DD}=2.3 ~ 3.6V, AV_{DD}=8.0 ~ 13.5V, DV_{SS}=AV_{SS}=0V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Clock pulse width	tw	1/85MHz	−	−	ns	
Clock pulse "H" period	th	5	−	−	ns	
Clock pulse "L" period	tl	5	−	−	ns	
Data setup time	tsu1	2	−	−	ns	
Data hold time	thd1	0	−	−	ns	
Start pulse setup time	tsu2	1	−	−	ns	
Start pulse hold time	thd2	2	−	−	ns	
Start pulse width	t_{WSFT}	1	−	2	CLK period	
Carry output delay time	tdc	−	−	11	ns	C_L=15pF
STB pulse width	t_{WSTB}	1	−	−	CLK period	
Final data timing	t_{LDT}	1	−	−	CLK period	
Time between STB ↑ and start pulse ↑	$t_{STB-SFT}$	6	−	−	CLK period	
Time between STB ↑ and CLK ↓	$t_{STB-CLK}$	4	−	−	ns	
POL/STB setup time	tsp	14	−	−	ns	
Output delay time	tdout	−	−	3	μs	LPC:normal *1*3
		−	−	5	μs	LPC:normal *2*3
		−	−	5	μs	LPC:low power *1*3
		−	−	7	μs	LPC:low power *2*3

*1 The value is specified when the drive voltage value reaches the target output voltage level of 90%.
*2 The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
*3 Output load condition:
R1=R2=R3=10kΩ, C1=C2=C3=20pF



●Block diagram

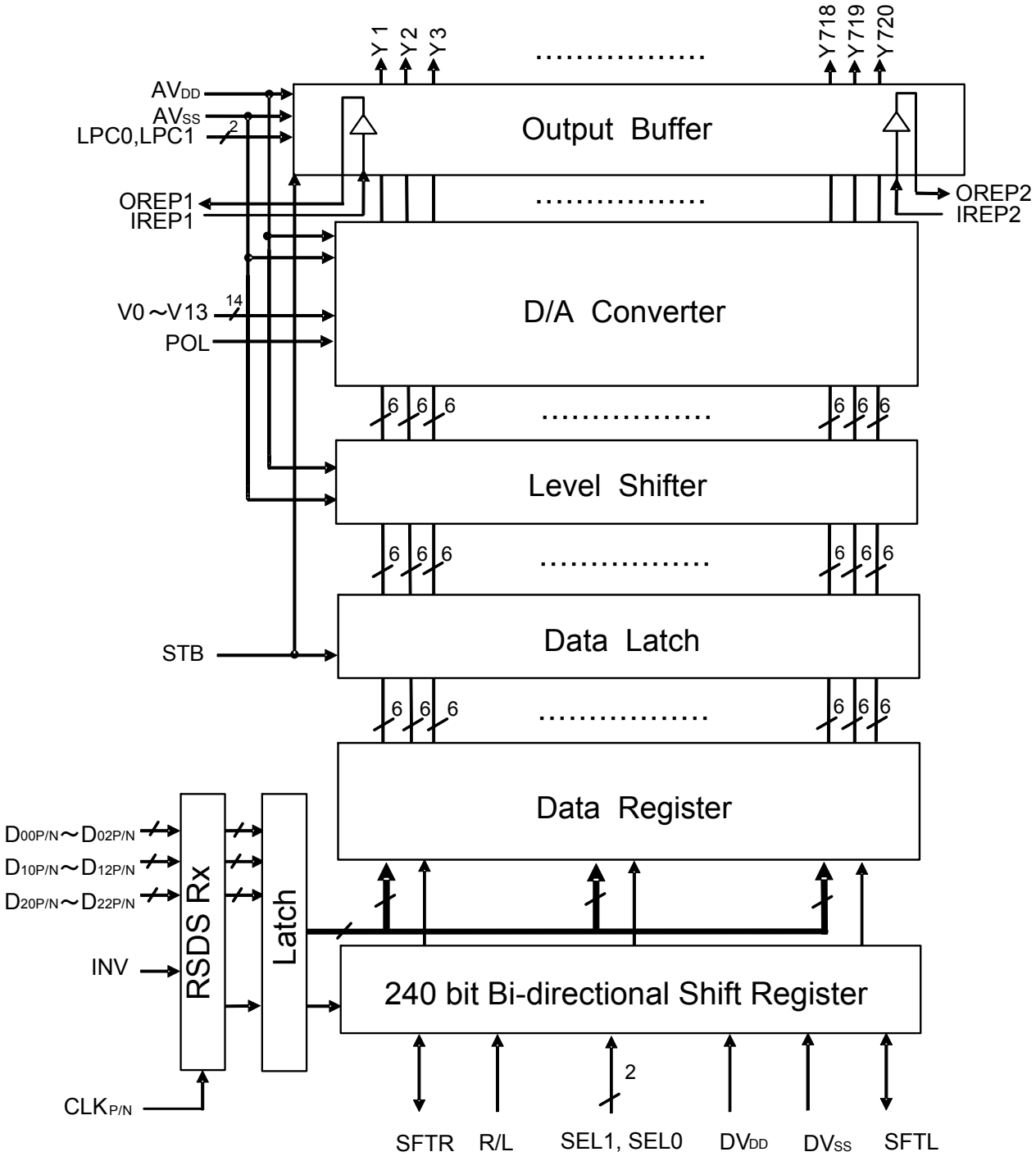


Fig.1 Block diagram

●Pin configuration

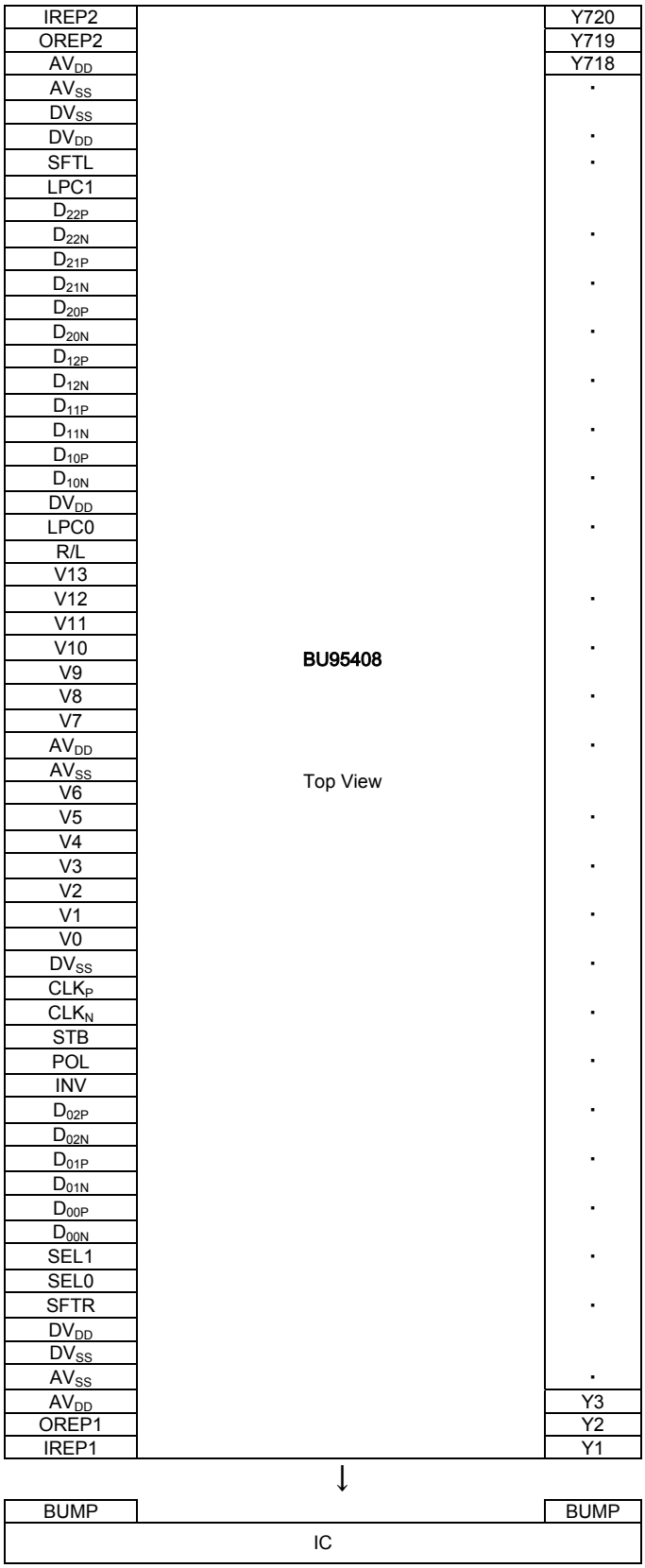


Fig.2 Pin configuration (Top View)

●Pin Descriptions

<table>
<tr><th>Pin Name</th><th>In/Out</th><th>Active</th><th>Descriptions</th></tr>
<tr><td>$D_{00P/N}$ ~ $D_{02P/N}$
$D_{10P/N}$ ~ $D_{12P/N}$
$D_{20P/N}$ ~ $D_{22P/N}$</td><td>In</td><td>Differential</td><td>RSDS™ input terminals of display data
The 3-bit differential input pairs generate the internal 6-bit data through the comparison between D_{XXP} and D_{XXN}.</td></tr>
<tr><td>$CLK_{P/N}$</td><td>In</td><td>Differential</td><td>The RSDS™ clock input pair generate the internal shift clock through the comparison between CLK_P and CLK_N.</td></tr>
<tr><td>Y1 ~ Y720</td><td>Out</td><td>-</td><td>Driver outputs for D/A converted 64 gray scale analog voltage.</td></tr>
<tr><td>R/L</td><td>In</td><td>-</td><td>The shift direction of internal shift register is controlled by this pin as shown below.
R/L=H : Right shift SFTR→Y1→Y720→SFTL
R/L=L : Left shift SFTL→Y720→Y1→SFTR</td></tr>
<tr><td>SEL0
SEL1</td><td>In</td><td>-</td><td>The output channel number is controlled by this pin as shown below.
<table>
<tr><th>SEL1</th><th>SEL0</th><th>Number of effective output terminal</th><th>Invalid output terminal</th></tr>
<tr><td>H</td><td>H</td><td>720(default)</td><td>-</td></tr>
<tr><td>H</td><td>L</td><td>702</td><td>Y355 ~ Y372 become Hi-Z</td></tr>
<tr><td>L</td><td>H</td><td>690</td><td>Y349 ~ Y378 become Hi-Z</td></tr>
<tr><td>L</td><td>L</td><td>684</td><td>Y349 ~ Y384 become Hi-Z</td></tr>
</table>
This pin is pulled up to the DV_{DD} inside the IC.</td></tr>
<tr><td>LPC0
LPC1</td><td>In</td><td>H</td><td>Low power control pin
<table>
<tr><th>LPC1</th><th>LPC0</th><th>power condition</th></tr>
<tr><td>H</td><td>H</td><td>Strong power</td></tr>
<tr><td>H</td><td>L</td><td>Normal power</td></tr>
<tr><td>L</td><td>H</td><td>Ultra-low power</td></tr>
<tr><td>L</td><td>L</td><td>Low power(default).</td></tr>
</table>
This pin is pulled down to the DV_{SS} inside the IC.</td></tr>
<tr><td>SFTR</td><td>In/Out</td><td>H</td><td>SFTR=H: Right shift start pulse input terminal in cascade connection.
SFTR=L: Carry output terminal in cascade connection.</td></tr>
<tr><td>SFTL</td><td>In/Out</td><td>H</td><td>SFTL=H: Carry output terminal in cascade connection.
SFTL=L: Left shift start pulse input terminal in cascade connection.</td></tr>
<tr><td>STB</td><td>In</td><td>↓</td><td>The data in the data register are transferred to the data latch at the rising edge of STB, then the gray scale voltages are output from the buffer at the falling edge of STB.</td></tr>
<tr><td>INV</td><td>In</td><td>H</td><td>Terminal to specify inverting or non-inverting of display data
INV:H : Input data are inverted in the IC.
INV:L : Input data are not inverted.</td></tr>
<tr><td>V0 ~ V13</td><td>In</td><td>-</td><td>Input for the γ-correction reference voltage
The following external reference voltages are input.</td></tr>
<tr><td>POL</td><td>In</td><td>-</td><td>At the rising edge of STB, the state of POL are transferred to the driver.
POL=H : The reference voltage for odd number outputs are V0 to V6 and those for even number outputs are V7 to V13.
POL=L : The reference voltage for odd number outputs are V7 to V13 and those for even number outputs are V0 to V6</td></tr>
<tr><td>IREP1,2</td><td>In</td><td>-</td><td>Repair amplifier input</td></tr>
<tr><td>OREP1,2</td><td>Out</td><td>-</td><td>Repair amplifier output</td></tr>
<tr><td>AV_{DD}</td><td>In</td><td>-</td><td>Power supply for driver block</td></tr>
<tr><td>AV_{SS}</td><td>In</td><td>-</td><td>Ground for AV_{DD}</td></tr>
<tr><td>DV_{DD}</td><td>In</td><td>-</td><td>Power supply for digital block</td></tr>
<tr><td>DV_{SS}</td><td>In</td><td>-</td><td>Ground for DV_{DD}</td></tr>
</table>

●Relationship between Input Data and Output Terminals

R/L=H (Right Shift)

	First			→	Last		
Data	D_{00P} ~ D_{02N}	D_{10P} ~ D_{12N}	D_{20P} ~ D_{22N}	…	D_{00P} ~ D_{02N}	D_{10P} ~ D_{12N}	D_{20P} ~ D_{22N}
Output	Y1	Y2	Y3	…	Y718	Y719	Y720

R/L=L (Left Shift)

	First			→	Last		
Data	D_{00P} ~ D_{02N}	D_{10P} ~ D_{12N}	D_{20P} ~ D_{22N}	…	D_{00P} ~ D_{02N}	D_{10P} ~ D_{12N}	D_{20P} ~ D_{22N}
Output	Y718	Y719	Y720	…	Y1	Y2	Y3

●Relationship between R/L , SFTR , SFTL and Output Direction

R/L pin controls the shift direction of the internal shift resistor as shown below.

Terminal	Right Shift Mode	Left Shift Mode
R/L	“H”	“L”
SFTR	Input	Output
SFTL	Output	Input
Output direction	Y1,Y2,Y3→Y718,Y719,Y720	Y720,Y719,Y718→Y3,Y2,Y1

●Relationship between POL and Output Polarity

POL	“H”	“L”
Y1	+*1	–*1
Y2	–	+
Y3	+	–
Y4	–	+
Y5	+	–
Y6	–	+
・ ・	・ ・	・ ・
Y715	+	–
Y716	–	+
Y717	+	–
Y718	–	+
Y719	+	–
Y720	–	+

*1 +: The reference voltage are V0 ~ V6
-: The reference voltage are V7 ~ V13

●Relationship between Input Data and Output Voltage

The LCD driver output voltages are determined by the input data and 14 γ -corrected power supply.

$0.1V \leqq V13 \leqq V12 \leqq V11 \leqq V10 \leqq V9 \leqq V8 \leqq V7 \leqq 0.5AV_{DD}$
$0.5\ AV_{DD} \leqq V6 \leqq V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 \leqq V0 \leqq AV_{DD} - 0.1V$

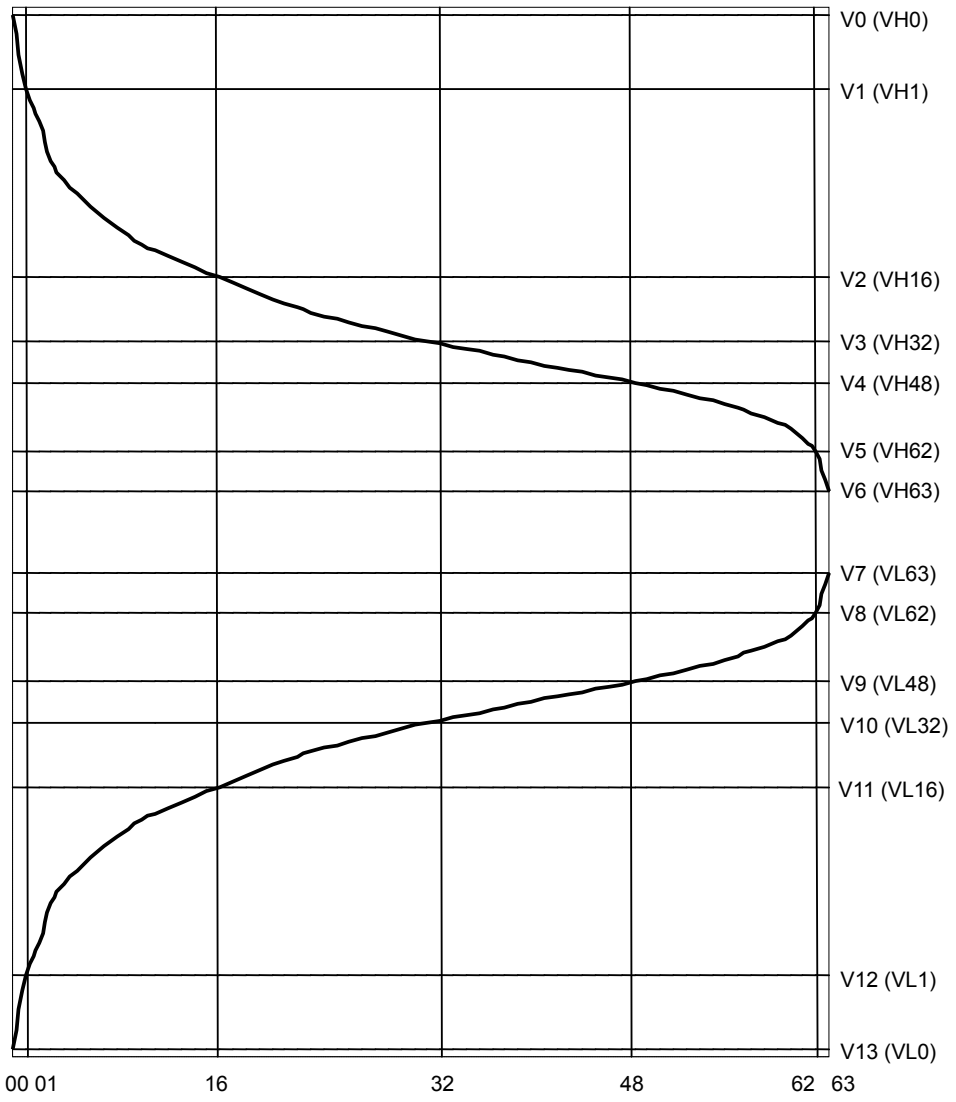


Fig.3 Input data – γ correction curve

● γ correction Power Supply Circuit

14 external γ-corrected power supply is connected to ladder resistors inside IC.

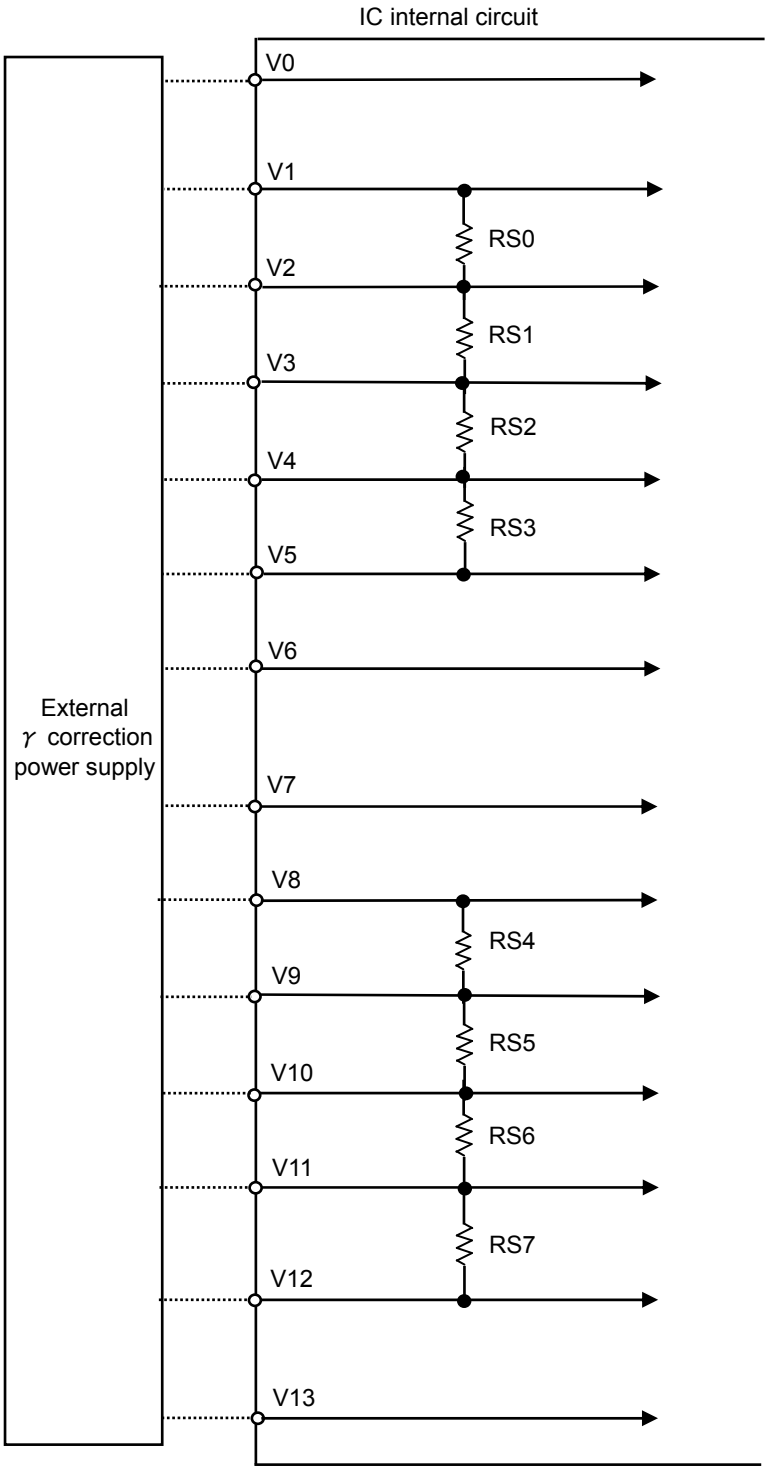


Fig.4 γ correction power supply circuit

●RSDS™ data timing

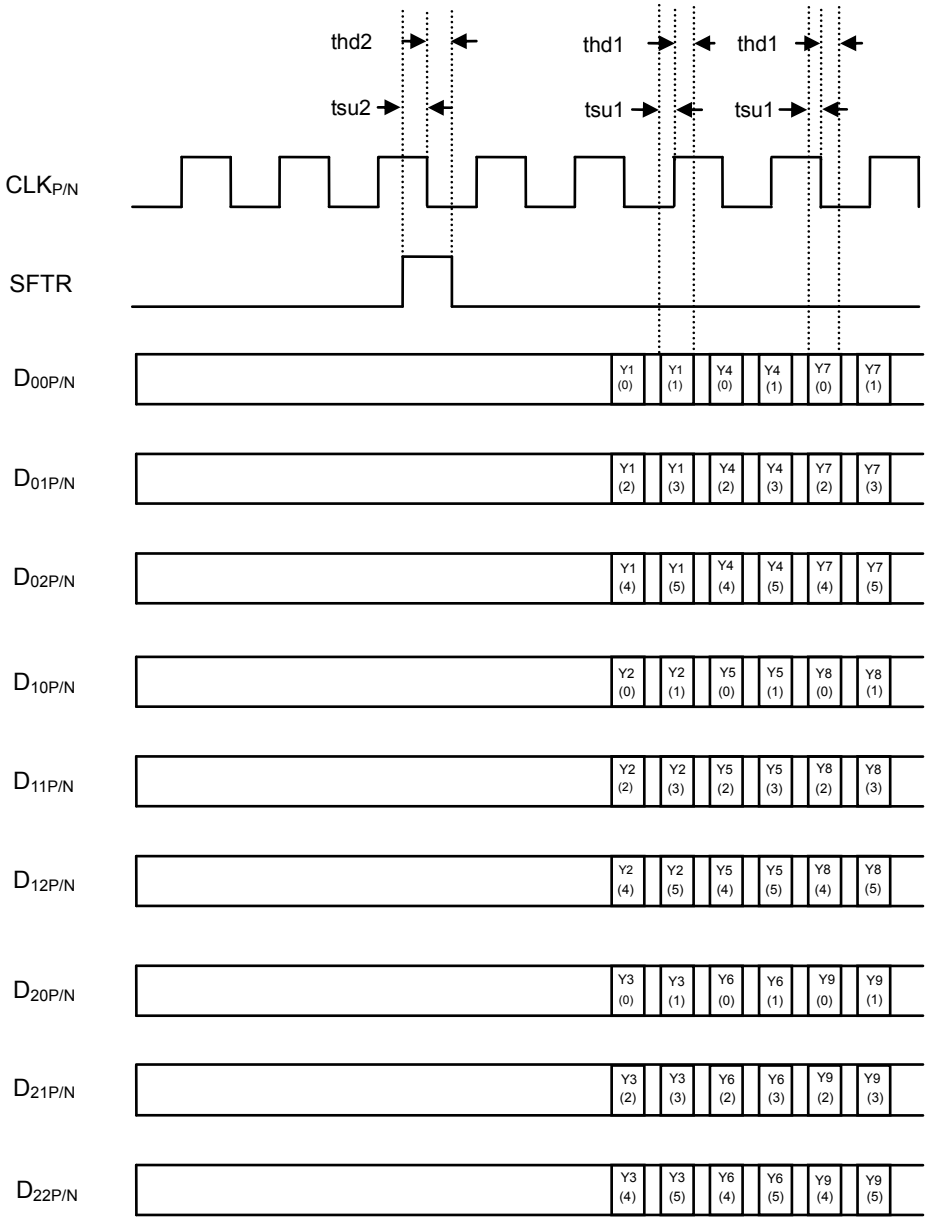


Fig.5 RSDS™ data timing

●Timing chart

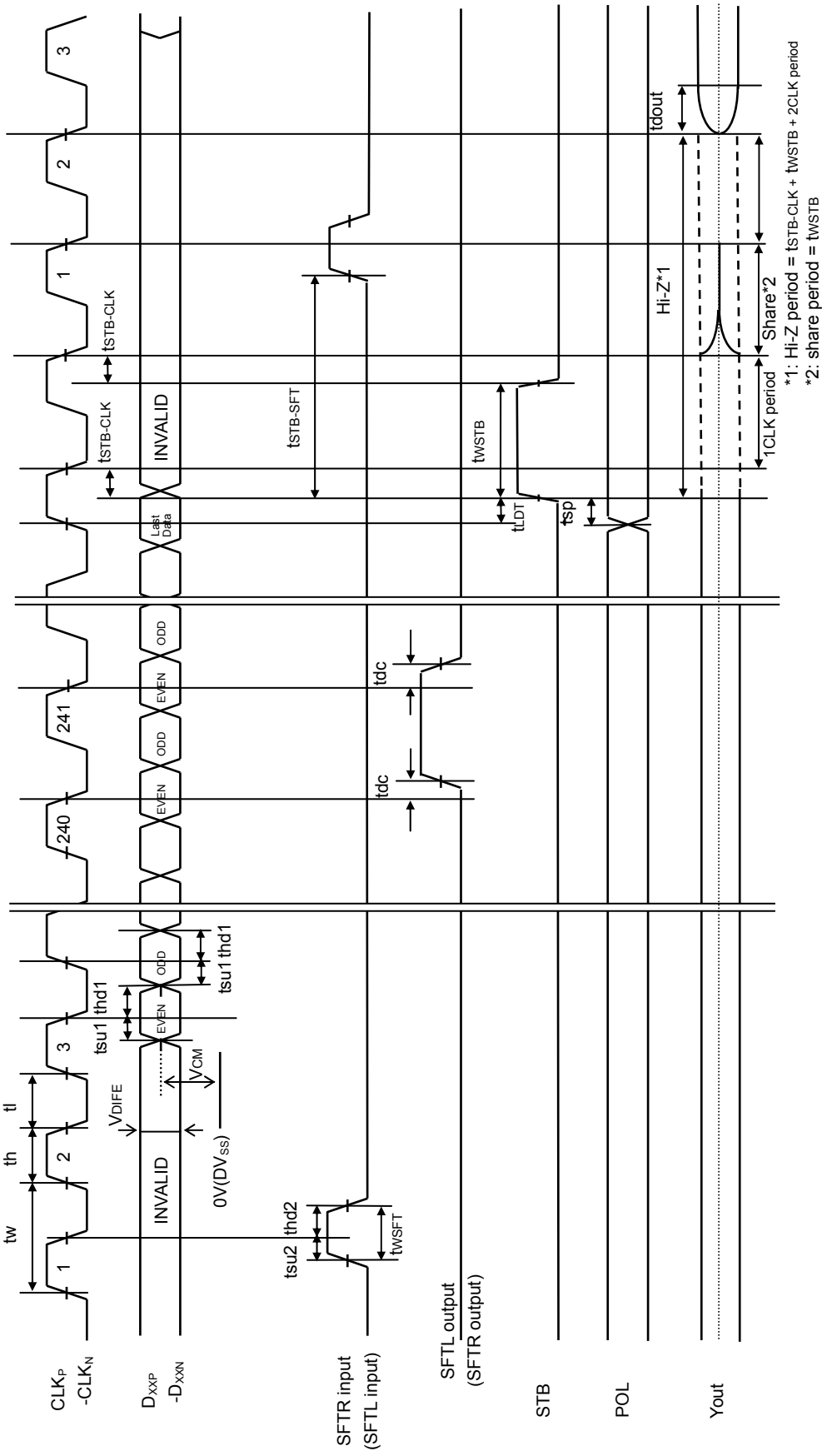
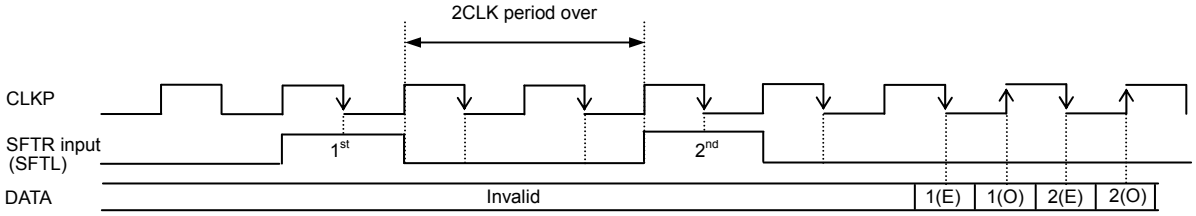


Fig.6 Timing chart

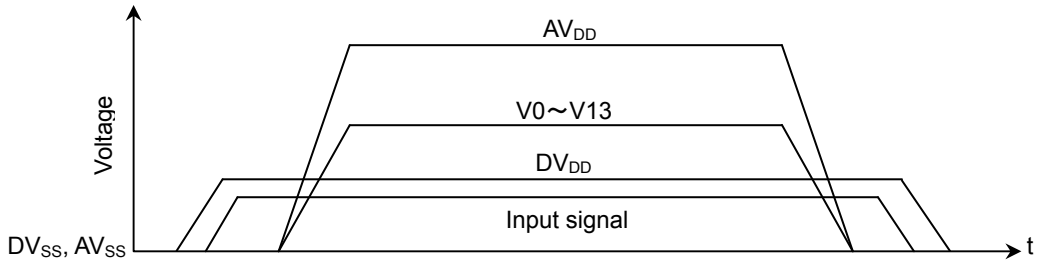
●Start pulse timing



When the start pulse (SFTR, SFTL) is input two times, the data is sampled based on the second start pulse.

●Power Supply Sequence

Maintain the following power supply order to prevent the device from being destroyed.
Turn on power order : DV_{DD} → Input signal → AV_{DD}, V0~V13
Turn off power order : AV_{DD}, V0~V13 → Input signal → DV_{DD}



●Notes for use

1. When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously.
   Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

2. For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays.
   Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

●Ordering part number

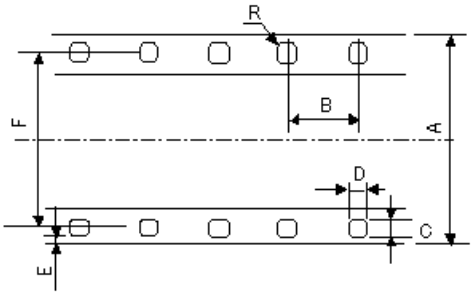
B	U	9	5	4	0	8	-	S	R

Part No. Part No.

Reel packing specification
SR: A pattern side is an inner arrow.
The output side is the right side.
SL: A pattern side is an inner arrow.
The output side is the left side.
BR: A pattern side is an outside arrow.
The output side is the right side.
BL: A pattern side is an outside arrow.
The output side is the left side.

COF48

<Tape dimensions>



No.	Item	48SW
A	Tape width	48.175±0.20
B	Perforation pitch	4.75±0.05
C	Perforation width	1.42±0.05
D	Perforation length	1.42±0.05
E	Edge to perforation	0.947±0.25
F	Width between perforation	44.86±0.07
R	Perforation corer radius	0.20±0.10

Unit : mm

<Packing specifications>

Shipment form	Reel
Standard amount	Maximum 60m per 1 reel . Maximum quantity 3100pcs per 1 reel . ※Quantity varies with tape length and yield.
Consecutive failures	Less than 9pcs
Tape direction	See Fig.7.

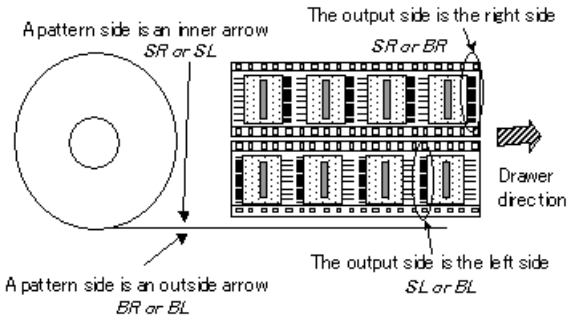


Fig.7 Tape direction

Notes

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