Rev.	Date	From	Description
V.002	10/3/2005	R2200	Original
V.003	10/31/2005	R2200	Modify the following items: 1. Add pin 17 PD_REG1D8 description; 1 for power down and 0 for power on 2. Add Absolute Maximum Ratings
V.004	12/1/2005	R2200	1.Add “SPI Digital Timing Diagram” and revised date code.
V.004	12/2/2005	R2100	2.Update output power data. 3.Removed RX IF input in Absolute Maximum Ratings.
		R2200	4.Add mini. Audio SNR.

Applicant:

R2200

Approvals:

R2000: S.C. Wong

R2500: C.J. Chao

R2100: J.Y. Tsai

Marketing: Jack Chang

R2200: W.K. Deng

R2300: T.S. Liou

☆ Signature on file in DC ☆

Document Title:
Data Sheet
of
RTC6701

Document No.: RTC6701-DST-004

Contents: 8
Attach: 0
Total Page: 9
File Format: Word

RTC6701 CMOS 2.4GHz FM/FSK Transmitter

Product Description

The RTC6701 is a FM/FSK transmitter intended for application on 2.4GHz ISM band analog FM or digital FSK transmission. The chip includes a RF modulator, two channels of audio modulator and a power amplifier with up to +11.5dBm power output. The RF modulator block, which is frequency-synthesizer based with an integrated 2.4GHz VCO, generates the 2.4GHz FM signal modulated from stereo audio L(left)/R(left) signals. On-chip two audio modulators with stereo audio input signals provide the FM audio modulated signal at 6 MHz and 6.5MHz, respectively. Monaural application is also possible by turning off one of two audio modulators.

Transmission frequency can be set by internal register via SPI programming, or by selecting among 4 fixed channels using three dedicated pins. Output power of +1.5dBm or +11.5dBm can be configured via pins 28 and 29 to fit CE/FCC requirement easily. The device is available in a 32-pin QFN package.

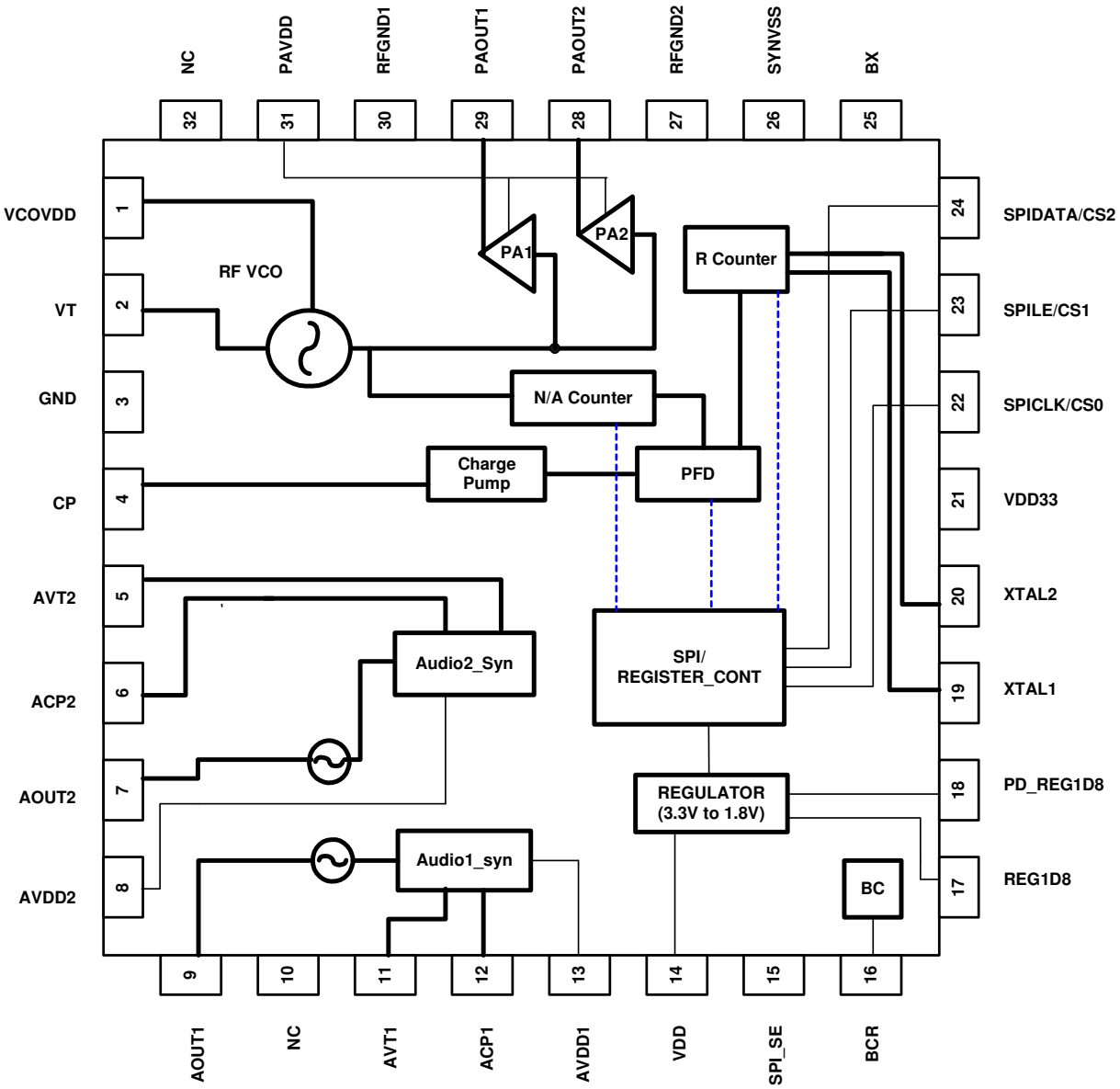
Features

- 3.3V power supply
- 2.4GHz ISM band FM modulator
- FM/FSK transmitter operation
- Simple three digital pins setting 4 fixed channels to eliminate external micro-controller
- Output Power +1.5dBm or +11.5dBm, selected by pin connection
- FM sound carriers at 6 and 6.5MHz
- CMOS technology
- On-chip VCO and PLL
- Transmitter frequency programmability by SPI
- 32-pin leadless QFN package

Application

- AV Sender
- FSK transmitter
- Baby Monitor
- Wireless Camera
- Wireless Audio
- Wireless Earphone

Block Diagram



Pin Descriptions

PIN	NAME	I/O	FUNCTION
1	VCOVDD	Supply In	VDD for VCO[1]
2	VT	Analog In	Vtune for VCO
3	GND	Analog GND	Analog GND
4	CP	Analog Out	Synthesizer charge pump output
5	AVT2	Analog In	Vtune for audio 2 PLL
6	ACP2	Analog Out	Charge pump for audio 2
7	AOUT2	Analog Out	FM modulated audio 2 output
8	AVDD2	Supply In	3.3V power supply for audio 2 modulator
9	AOUT1	Analog Out	FM modulated audio 1 output
10	NC	NC	NC
11	AVT1	Analog In	Vtune for audio1 PLL
12	ACP1	Analog Out	Charge pump for audio 1
13	AVDD1	Supply In	3.3V power supply for audio 1 modulator
14	VDD	Supply In	3.3V Digital DC power supply
15	SPI_SE	Digital In	Switch mode or SPI selection (Internal pull high)
16	BCR	Analog I/O	Reference current by connecting 10k resistor
17	REG1D8	Analog Out	Regulator OUT 1.8V regulator output
18	PD_REG1D8	Digital In	Power down for 1.8V regulator 1: Power Down; 0: Power On
19	XTAL1	Analog I/O	Crystal connection
20	XTAL2	Analog I/O	Crystal connection
21	VDD33	Supply In	3.3V DC power supply for digital circuits
22	CS0	Digital In	Easy channel selection[2] (Internal pull high)
	SPICLK	Digital In	SPI bus clock input
23	CS1	Digital In	Easy Channel selection[2](Internal pull high)
	SPILE	Digital In	SPI bus latch enable input
24	CS2	Digital In	Easy Channel selection[2] (Internal pull high)
	SPIDATA	Digital In	SPI bus data input
25	BX	Digital In	Alternative band selection[2] (Internal pull high)
26	SYNVSS	Digital GND	Digital GND for synthesizer
27	RFGND2	Analog GND	RF GND
28	PAOUT2	Analog Out	Connect with PAOUT1 for +12dBm output
29	PAOUT1	Analog Out	PA output for 0dBm
30	RFGND1	Analog GND	RF GND
31	PAVDD	Supply In	3.3V VDD for PA ESD
32	NC	NC	NC

Note 1. Connect to 3.3V supply through a resistor. Nominal voltage at this pin=2.5V.
Note 2. Digital pins (15, 22, 23, 24, 25) with internal pull-high circuits can be left floating for logical high.

ELECTRICAL SPECIFICATIONS

(1) Absolute Maximum Ratings

SYMBOL	PARAMETER	Ratings	UNIT
Tstr	Storage Temperature Range	-65 to +150	°C
Totr	Operating Temperature Range	-40 to +85	°C
Vdd	Supply Voltage	-0.5 to +5	V
Vlog	Logic control signal	-0.5 to +5	V

The maximum rating must not be exceeded at any time. Do not operate the device under conditions outside the above ratings.

(2) DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Tj	Temperature Range	-	-40	25	85	°C
VDD	Supply Voltage		3.1	3.3	3.5	V
I_RF	Power consumption for chip (+12dBm output)	TT 25C, 3.3V		49		mA
I_module	Power consumption for module	TT 25C, 3.3V		54		mA
I_pd	Power down current leakage	TT 25C, 3.3V		1	10	uA
Fref	Oscillator operating frequency			8		MHz
V_IH	High Level Input Voltage for Digital Interface	V_IO=3V	0.7xV_IO		V_IO+0.3	V
V_IL	Low Level Input Voltage for Digital Interface		-0.3		0.3xV_IO	V

(3) Transmitter Specifications

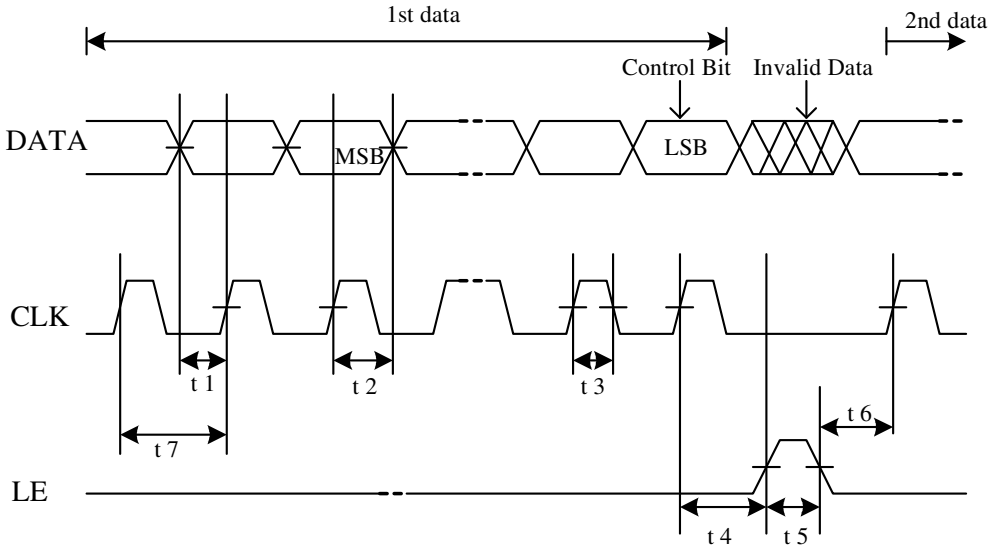
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Fc	Frequency Range		2.37		2.51	GHz
Pout_H*	Maximum output power at high power mode	Connect PAOUT1 and PAOUT2	10.5	11.5	12.5	dBm
Pout_L*	Maximum output power at low power mode	Connect PAOUT1 only	0.5	1.5	2.5	dBm
2ndH_H*	The 2nd Harmonic referenced with the fundamental signal at high power mode	With reference filter design		-30		dBc
PN	The phase noise at 2414GHz	100KHz offset 1MHz offset		-85 -110		dBc/Hz
3rdH_H*	The 3rd Harmonic referenced with the fundamental signal at high power mode	With reference filter design		-40		dBc
2ndH_L*	The 2nd Harmonic referenced with the fundamental signal at low power mode	With reference filter design		-30		dBc
3rdH_L*	The 3rd Harmonic referenced with the fundamental signal at low power mode	With reference filter design		-40		dBc

* All with proper match at the PA output, before further ceramic filtering.

(3) Transmitter Specifications (continued)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Video						
Zin_video	Video input impedance (as reference design)			75		Ω
Vin_video	Video peak to peak input voltage (as reference design)	75 ohm load		1		Vpp
Audio						
VTAA	Video carrier to audio carrier ratio (as reference design)	No video and audio signal in	24	27	30	dBc
fau	Audio carrier frequency	Left sound Right sound		6 6.5		MHz
Vin_audio	Audio peak to peak voltage at audio Vtune pin	@1KHz tone input with ±25KHz frequency deviation		30		mVpp
THD	Total harmonic distortion measurement by RTC6711 receiver	@1KHz tone input with ±25KHz frequency deviation		0.6	0.9	%
F_corner	3dB corner frequency of pre-emphasis (as reference design)			4		kHz
SNR_A	Audio SNR (as reference design,) With pre-emphasis/ de-emphasis,	@1KHz tone input with ±25KHz frequency deviation	45	47		dB

(4) SPI Digital Timing Diagram



Parameter	Min.	Typ.	Max.	Unit
t1	20	-	-	ns
t2	20	-	-	ns
t3	30	-	-	ns
t4	30	-	-	ns
t5	100	-	-	ns
t6	20	-	-	ns
t7	100	-	-	ns

Note:
1.) On the rising edge of the clock, one bit of data is transferred into the shirt register.
2.) LE should be *L* when the data is transferred into the shirt register.

Channel Selection

There are two principle modes for channel selection.

SPI_SE (Pin 7)	High	Low
Mode	SPI Mode	Easy Channel Selection Mode

(1) Easy channel selection mode

When pin 15 (SPI_SE) is set at low (0V), the chip operates in easy channel selection mode. Operation frequency can be selected by the pins 25(BX), 24(CS2), 23(CS1) and 22(CS0). The selected channel frequencies are listed in the table below.

BX=0

Pin25 (BX) is pulled to low for normal ISM band, and operation frequency table show as following Table.

BX	**SPI_SE**	**Pin22/Pin23/Pin24 CS0/CS1/CS2**			
		011	101	110	111
0	0	2414MHz	2432MHz	2450MHz	2468MHz

BX=1

Reserved for alternative band selection

(2) SPI mode

When pin 15 (SPI_SE) is set at high (3.3V), the chip works as in the SPI mode and the pins 24(SPIDATA), 23(SPILE) and 22(SPICLK) are used for 'SPI' inputs for 3-wire programming interface. The BX is "don't care".

SPI REGISTER DEFINITION

Address 00: Synthesizer Register A

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Syn_RF_R_Reg															Syn_RF_A_Reg							address	
PIN	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	A6	A5	A4	A3	A2	A1	A0		
Default	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	1	1	1	1	0	0	0	0

Syn_RF_R_Reg : R counter divider ratio control register [14:0]
Syn_RF_A_Reg : A counter divider ratio control register [6:0]

R14=MSB, R0=LSB

For integer N Synthesizer, the RF LO frequency is calculated by $(N*64+A)*f_{ref}/R$, where f_{ref} is the frequency of external reference oscillator (8 MHz). Ex for channel 1 operation (f = 2414MHz)
Default: R=400; N=1885; A=60
2414MHz=(1885*64+60)*8MHz/400

Address 01: Synthesizer Register B

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Syn_RF_N_Reg													CP_RF			SC _trl	Not used					address	
PIN	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0											
Default	0	0	1	1	1	0	1	0	1	1	1	0	1	0	0	1	0	X	X	X	X	X	0	1

Syn_RF_N_Reg : N counter divider ratio control register [12:0] (default R ratio=400)
CP_RF [2:0] RF charge pump current control (from 50uA to 6mA, default=100uA)
SC_ctrl: external/internal SC_select control pin (LOW=internal). If set "1" in RTC67 series then charge pump will enter the testing mode ----Only for internal testing

Address 10: Synthesizer Register C

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Not Used			Not Used									Mout		PRE_control			Not used			PA_Bias		address	
PIN				8	7	6	5	4	3	2	1	0	1	0	2	1	0				1	0		
Default	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	X	X	X	1	0	1	0

Mout : Multi-function output select
(00,01,11,10)=(gnd, lock in detect ,RF divider output, reference clk output)
PRE_control[2:0]: prescalar current control (20~140uA)
PA_Bias[1:0]: PA bias resistor selection

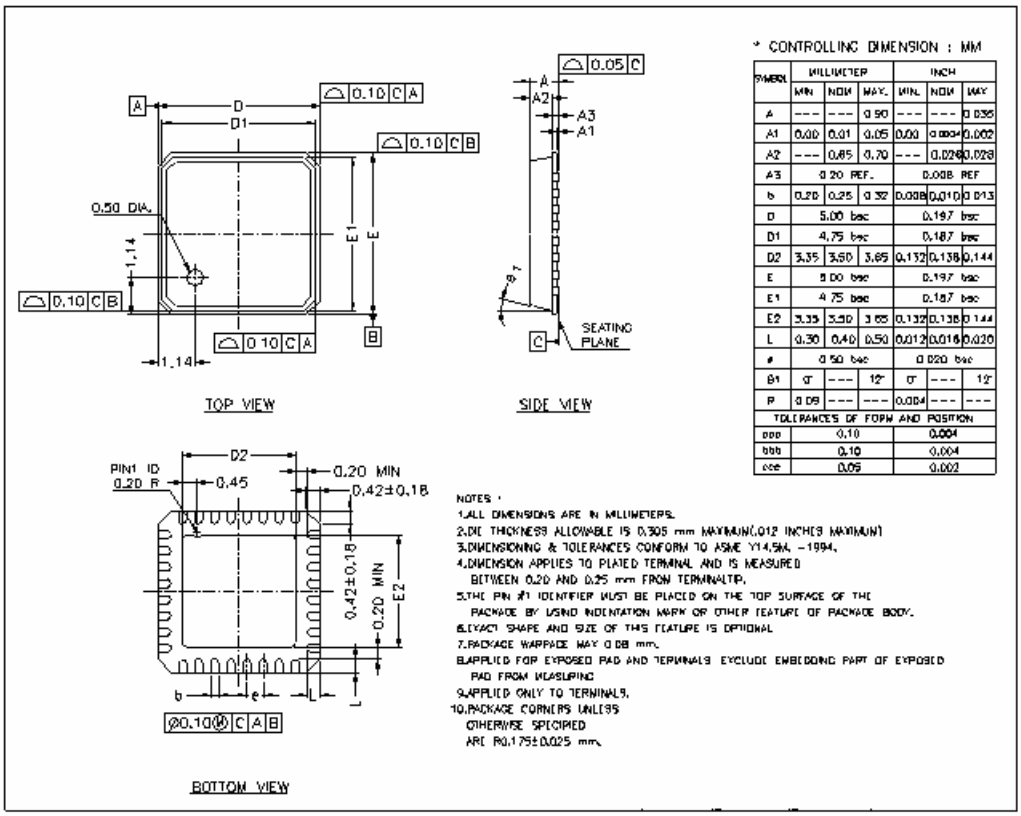
Address 11: Synthesizer Register D

Bits	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Not Used											VCOSC		PA_ PD	Audio_div					Not use d	ACP		address	
PIN												1	0		7	6	5	4	3	2	1	0		
Default	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	1	0	0	1	0	0	0	1	1

VCOSC[1:0]: 2-bit RF VCO switch capacitor control in RTC6701
PA_PD 1: PA power down control, 0 for power on and 1 for power down
Audio_div[5:0]: Reference clock division ratio in audio carrier frequency synthesizer.
ACP[1:0]: Audio charge pump current control (default 00:20uA, 01:50uA, 10: 110uA, 11: 140uA)

PACKAGE

QFN 5X5 32 pins



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.000	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.20	0.25	0.32	0.008	0.010	0.013
D	5.00 BSC.			0.197 BSC.		
D1	4.75 BSC.			0.187 BSC.		
D2	3.35	3.50	3.65	0.132	0.138	0.144
E	5.00 BSC.			0.197 BSC.		
E1	4.75 BSC.			0.187 BSC.		
E2	3.35	3.50	3.65	0.132	0.138	0.144
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 BSC.			0.020 BSC.		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL
7.PACKAGE WARPAGE MAY 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING
9.APPLIED ONLY TO TERMINALS.
10.PACKAGE CORNERS UNLESS OTHERWISE SPECIFIED ARE R0.175±0.025 mm.