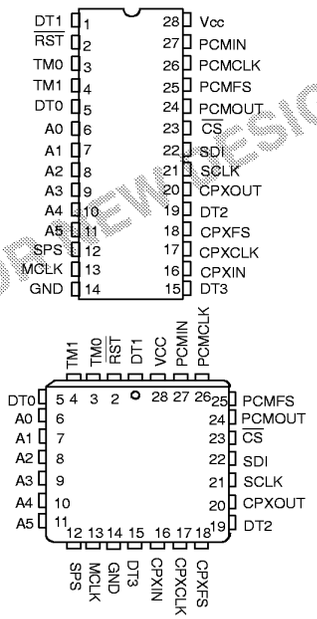
DALLAS SEMICONDUCTOR

DS2130Q
Voice Messaging Processor

FEATURES

- Per–channel voice messaging processor for digitized voice storage and retrieval
- High fidelity speech recording and playback at 8, 12, 16, 24 and 32 Kbits/sec
- Integral DTMF transceiver for remote touch-tone control and dialing
- Connects to popular PCM codec/filters for analog interfacing
- Direct PCM serial data bus interfaces to any of 32 possible TDM time slots
- Monitors and reports audio energy levels for call progress and voice detection
- Selectable beep generator for sound prompts
- 3–wire synchronous serial control port
- 28–pin DIP or PLCC (DS2130Q) packages

PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGN

DESCRIPTION

The DS2130 Voice Messaging Processor is a CMOS DSP processor that serves as a voice messaging engine for digitized voice storage and retrieval applications. It offers half–duplex speech compression or expansion at either 8, 12, 16, 24 or 32 Kbits/sec. The advanced speech compression algorithm maintains excellent audio clarity even at low bit rates. The algorithm also incorporates a DTMF transceiver for decoding or generating touch–tone signals for remote control and automatic dialing. The tone generator can be used to create single–tone beeps used in popular answering machines. Voice and call progress detection can be easily implemented using the energy threshold detect outputs.

The DS2130 can be used together with a low–cost codec/filter device for analog interfacing in standalone applications such as answering machines or feature phones. It can also interface directly to a serial PCM bus on any of up to 32 possible time slots using an internal software–selectable time slot assigner circuit (TSAC). This configuration can be used in digital switching systems for adding voice messaging services to existing backplane designs.

Applications include digital answering machines, embedded voice response, speech annunciators, voice mail, key telephone systems and automatic operator services.

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PIN DESCRIPTION Table 1

PIN	SYMBOL	TYPE	DESCRIPTION
5 1 19 15	DT0 DT1 DT2 DT3	O O O O	**Detect outputs 0–3.** These are the four output detect lines that report energy threshold levels and DTMF tones. DTMF tone detection always has precedence over energy level reporting.
2	RST	I	**Reset input.** When this pin is low, the internal DSP algorithm is in a reset state for proper initialization. The DS2130 should always be reset for at least 1 ms after each power–up occurrence.
3 4	TM0 TM1	I I	**Test mode pins.** These pins are used for factory testing and must be tied to GND for proper operation.
6 7 8 9 10 11	A0 A1 A2 A3 A4 A5	I I I I I I	**Address Select.** Provides serial address ID of the DS2130. The states of A0–A5 must match the address sent in the command byte to enable the serial port. A0 = LSB.
12	SPS	I	**Serial Port Select.** This pin must be tied to V_{CC} for proper operation of the serial port. The hardware mode is not supported on the DS2130.
13	MCLK	I	**Master processing clock.** This is the clock used for the internal DSP engine and should be in the range of 10.5 – 13 MHz. MCLK can be asynchronous to any other clock signal on the DS2130. The duty cycle should be nominally 50%.
14	GND	–	**Ground.** Tie this pin to the system logic ground.
16	CPXIN	I	**Compressed data in.** This is the serial data input for the compressed audio data sampled on falling edges of CPXCLK during selected time slots. This data is expanded to 8–bit PCM that is output on PCMOUT except in PCM bypass mode.
17	CPXCLK	I	**Compression/expansion side data clock.** This is the clock used to sample data at CPXIN, to output data at CPXOUT and to determine the proper time slot. CPXCLK must be synchronous with CPXFS. See “Special Clock Requirements” section for more details.
18	CPXFS	I	**Compression/expansion side frame sync.** This input must be an 8 KHz clock for proper operation. CPXFS must be the same frequency as PCMFS (normally they are tied together).
20	CPXOUT	O	**Compressed data out.** This is the serial data output for the compressed audio data, updated on rising edges of CPXCLK during selected time slots.
21	SCLK	I	**Serial port clock.** This is the clock used to write configuration data to the serial port registers.
22	SDI	I	**Serial data input.** Data source for the serial port registers.
23	CS	I	**Chip select input.** This pin must transition high to low before each write operation to the serial port.
24	PCMOUT	O	**PCM output.** This is the output for expanded data which is in the standard 8–bit PCM u/A–law format. Data is updated on rising edges of PCMCLK.

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PIN	SYMBOL	TYPE	DESCRIPTION
25	PCMFS	I	**PCM side frame sync.** An 8 KHz clock signal must be applied for the PCM data interface. Lower sample rates can be used to reduce the effective bit rate but may result in unusable DTMF detection and generation as well as lower voice quality. PCMFS is normally tied to CPXFS.
26	PCMCLK	I	**PCM side data clock.** This is the clock used to sample PCM serial data at PCMIN, to output data at PCMOUT and to determine the proper time slot. PCMCLK must be synchronous with PCMFS.
27	PCMIN	I	**PCM data input.** This is the input for the 8–bit serial PCM data which would normally be supplied by a codec/filter device. Data is sampled on falling edges of PCMCLK.
28	V_{CC}	–	**Positive supply input.** Tie to system +5 volt supply.

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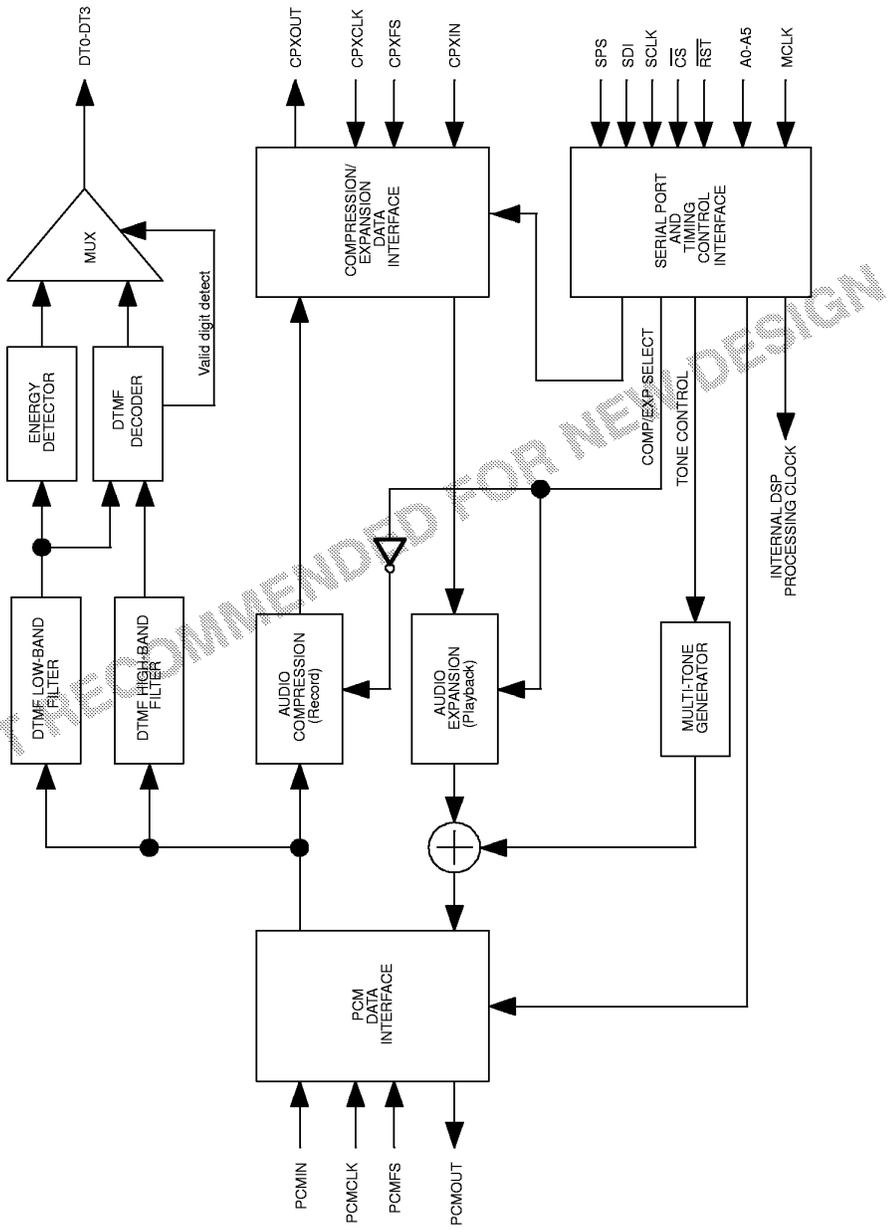
DS2130 SIGNAL FLOW DIAGRAM Figure 1



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HARDWARE RESET

$\overline{RST}$ allows the host to reset the DSP algorithms and the contents of the serial port control registers. This pin must be held low for at least 1 ms on system power–up after MCLK is stable to ensure that the device has initialized properly. $\overline{RST}$ clears all bits of both control registers except the CPD1 and CPD2 bits, which are set to one. However, these bits are ignored until they have been reset by the host; that is, the DS2130 will not power up in the power–down mode. This permits the host to communicate through the serial port at full speed after power–up.

SERIAL PORT CONTROL

An external host controller writes configuration data to the DS2130 via the serial port through inputs SCLK, SDI, and $\overline{CS}$ as shown in Figure 2 (read operations are not supported). Each write to the DS2130 is either a 2–byte write or a 4–byte write. A 2–byte write consists of the Address/Command Byte (ACB) followed by a byte to configure either the Voice Control Register (VCR) or the Tone Control Register (TCR). The 4–byte write consists of the ACB followed by a byte to configure the appropriate control register and then two bytes for input and output time slot mapping. When writing to the VCR, the next two bytes program the input and output time slots respectively for the compression/expansion (CPX) side interface. When writing to the TCR , the next two bytes program the input and output time slots respectively for the PCM side interface.

ADDRESS/COMMAND BYTE

The address/command byte is the first byte written to the serial port; it identifies which of the 64 possible DS2130's sharing the serial bus is to be accessed. Address data must match that at inputs A0 to A5. If no match occurs, the DS2130 ignores the following data at SDI. If an address match occurs, the next three bytes written are accepted as control, input and output time slot data. Bit ACB.6 determines whether the Voice or Tone Control register is to be updated.

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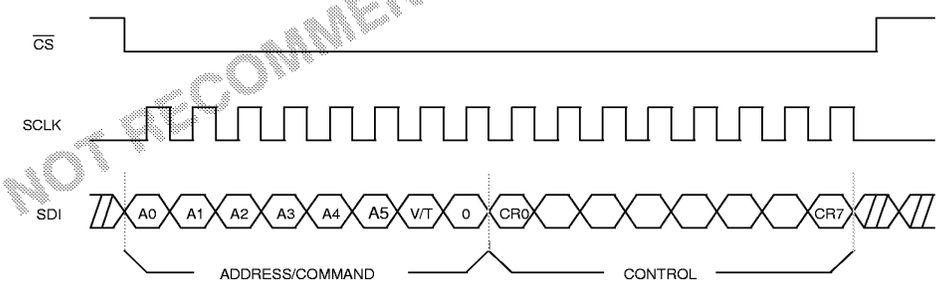
SERIAL PORT WRITE Figure 2



NOTE:
A 2–byte write is shown.

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ADDRESS/COMMAND BYTE Figure 3

(MSB)							(LSB)
–	V/T	A5	A4	A3	A2	A1	A0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	ACB.7	Reserved; must be zero for proper operation.
V/T	ACB.6	Voice/Tone command byte select. 0 = write to Tone Generator Control register 1 = write to Voice Control register
A5	ACB.5	MSB of Device Address.
A4	ACB.4	
A3	ACB.3	
A2	ACB.2	
A1	ACB.1	
A0	ACB.0	LSB of Device Address.

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VOICE CONTROL REGISTER

The Voice Control Register (VCR) determines the compression/expansion bit rate and PCM data format. It also provides power–down and algorithm reset control.

The u/A bit selects either μ–law or A–law PCM data encoding for PCMIN and PCMOUT pins. When u/A = 1, μ–Law is selected; when u/A = 0, A–Law is selected.

Compression or expansion bit rates are determined by bits CXS1, CXS2 and CXS3. See Table 2 for the mapping of these bits. For the reduced bandwidth modes, the incoming PCM data is internally filtered with a 1.7 KHz low–pass and sampled at one–half of the CPXFS/PCMFS frequency. The PCM Bypass mode (CXS1=1, CXS2=0 and CXS3=1) permits input PCM data at either PCMIN or CPXIN to be routed out to CPXOUT or PCMOUT respectively, bypassing normal compression/expansion.

Voice compression/expansion can be disabled by setting CPD1 to a 1. In this mode, the compression/expansion algorithm is idled and CPXOUT is tri–stated. This mode should be used when only DTMF/tone generation and detection are desired. When CPD1 and CPD2 (CPD2 is in the Tone Control register) are both equal to a 1, the device enters a low-power standby mode in which all DSP operation is halted. *In this mode, the serial port must not be operated faster than 39 KHz.*

CPXRST resets the algorithm coefficients for the expansion/compression algorithm to their initial values. CPXRST will be cleared by the device when the algorithm reset is complete.

The compression/expansion loopback feature is enabled when CXLB is set and CPD1 is cleared. During this loopback, no expansion or compression occurs and input data at CPXIN is looped back to the appropriate time slot at CPXOUT.

Compression or expansion operation is selected via the CP/EX bit (the DS2130 cannot perform both simultaneously).

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VOICE CONTROL REGISTER Figure 4

(MSB)							(LSB)
CP/EX	CXS1	CPD1	CXRST	CXLB	U/A	CXS2	CXS3

SYMBOL	POSITION	NAME AND DESCRIPTION
CP/EX	VCR.7	Compression/expansion select. 1 = compress (record) 0 = expand (playback)
CXS1	VCR.6	Compression/expansion bit rate select 1; see Table 2.
CPD1	VCR.5	Compression/Expansion power–down 1. 0 = Compression/expansion enabled 1 = Compression/expansion disabled
CXRST	VCR.4	Compression/expansion algorithm reset. 0 = normal operation 1 = reset algorithm to initial coefficients
CXLB	VCR.3	Compression/expansion interface loopback. 0 = normal operation 1 = bypass selected channel
U/A	VCR.2	PCM input/output data format. 0 = A–Law 1 = μ–Law
CXS2	VCR.1	Compression/Expansion bit rate select 2; see Table 2.
CXS3	VCR.0	Compression/Expansion bit rate select 3.

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COMPRESSION/EXPANSION BIT RATE SELECT Table 2

ALGORITHM SELECTED	CXS1	CXS2	CXS3
64K bps to/from 32 Kbps	0	0	0
64K bps to/from 24 Kbps	1	1	0
64K bps to/from 16 Kbps	0	1	0
Reserved for future operation	1	0	0
64K bps to/from 16 Kbps[1]	0	0	1
64K bps to/from 12 Kbps[1]	1	1	1
64K bps to/from 8 Kbps[1]	0	1	1
64K bps to/from 64 Kbps (PCM Bypass mode)	1	0	1

NOTE:

1. These reduced bandwidth modes use an internal low–pass filter at 1.7 KHz to permit a lower bit rate. The normal bandwidth otherwise is 300 Hz to 3.4 KHz due to the filters typically present in the codec/filter device used with the DS2130.

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TONE CONTROL REGISTER

The Tone Control register provides access to the tone generator and controls power–down and reset functions.

The tone generator is controlled by bits TS0–3, which cause either transmission of a DTMF digit or one of three possible single–tone sine waves. The DTMF digits that can be transmitted are 0–9, # and *. The single tones available are 350, 620 and 1004 Hz, any of which can be used as beeps for user prompting. Tone generation lasts for as long as the particular state is programmed; all tone generation ceases when TS0–3 equal 1111 (the power–up state). When writing a new value for TS0–3 (including the 1111 state), the TRST bit must be simultaneously set to a 1; otherwise, the old value of TS0–3 will continue to be used. It is recommended that DTMF digits be sustained for at least 50 mS for proper network recognition.

The CPD2 bit is used in conjunction with CPD1 (in the VCR) to enable a power–down mode in which power consumption is reduced to a minimum. CPD1 and CPD2 must both equal a 1 to enter this mode. The PCMOUT output is three-stated when CPD2 = 1.

Testing of the DTMF generation and detection circuitry can be accomplished by setting TLB to a 1. In this mode, transmit DTMF tones are internally looped back to the DTMF receiver for test purposes (the DT0–3 pins can be monitored for proper operation). Also in this mode, input PCM data is looped back to the appropriate time slot on PCMOUT. This permits isolation and testing of the external codec/filter used with the DS2130.

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TONE CONTROL REGISTER Figure 5

(MSB)							(LSB)
TS3	TS2	CPD2	TRST	TLB	TS1	TS0	–

SYMBOL	POSITION	NAME AND DESCRIPTION
TS3 TS2 TS1 TS0	TCR.7 TCR.6 TCR.2 TCR.1	Tone selects 0–3. See Table 3 for tone bit mapping. TRST must be written to a 1 when a new tone value is to be written.
CPD2	TCR.5	Compression/Expansion power–down 2. 0 = Normal operation 1 = Power–down all DSP operation. CPD1 must equal 1 as well. CPD1=0 while CPD2=1 should not be programmed.
TRST	TCR.4	Tone generation reload enable for TS0–3. 0 = normal operation/ready for new value 1 = load new tone value
TLB	TCR.3	Tone generation loopback. 0 = normal operation 1 = loopback tone signals to DTMF receiver
–	TCR.0	Should always be set to 1.

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TONE GENERATION BIT MAPPING[1] Table 3

TS3–TS0	SIGNAL	LEVEL (dBm0)
0000	DTMF “0”	–3
0001	DTMF “1”	–3
0010	DTMF “2”	–3
0011	DTMF “3”	–3
0100	DTMF “4”	–3
0101	DTMF “5”	–3
0110	DTMF “6”	–3
0111	DTMF “7”	–3
1000	DTMF “8”	–3
1001	DTMF “9”	–3
1010	DTMF “*”	–3
1011	DTMF “#”	–3
1100	1004 Hz	0
1101	350 Hz	–12
1110	620 Hz	–12
1111	Silence	OFF

1. States 0000 through 1011 generate DTMF digit signals; states 1100, 1101 and 1110 generate single frequency tones; state 1111 disables all tone generation (DTMF or single tone).

NOT RECOMMENDED FOR NEW DESIGN

INPUT TIME SLOT REGISTER Figure 6

(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	ITR.7	Reserved; must be zero for proper operation.
–	ITR.6	Reserved; must be zero for proper operation.
D5	ITR.5	MSB of input time slot register.
D4	ITR.4	
D3	ITR.3	
D2	ITR.2	
D1	ITR.1	
D0	ITR.0	LSB of input time slot register.

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OUTPUT TIME SLOT REGISTER Figure 7

(MSB)							(LSB)
–	–	D5	D4	D3	D2	D1	D0

SYMBOL	POSITION	NAME AND DESCRIPTION
–	OTR.7	Reserved; must be zero for proper operation.
–	OTR.6	Reserved; must be zero for proper operation.
D5	OTR.5	MSB of output time slot register.
D4	OTR.4	
D3	OTR.3	
D2	OTR.2	
D1	OTR.1	
D0	OTR.0	LSB of output time slot register.

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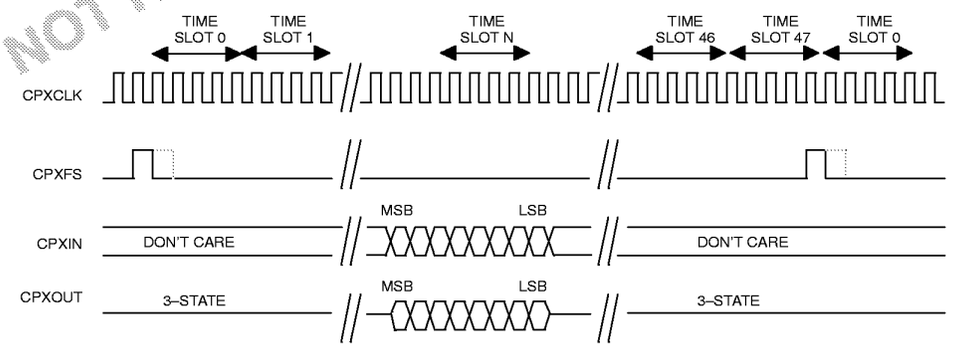
TIME SLOT ASSIGNMENT/ORGANIZATION
Onboard counters establish when PCM and compression/expansion I/O occurs. The counters are programmed via the time slot registers. Time slot size (number of bits wide) is 8 bits for PCMIN PCMOUT and 4 bits for CPXIN, CPXOUT (except if CXS3=1; CPXIN and CPXOUT use 8–bit time slots in this case). The number of time slots available is 32 for the PCM–side interface and 64 for the CPX–side interface (32 if CXS3=1). However, the data clocks PCMCLK and CPXCLK must be at least 256 X PCMFS to properly access all 32 or 64 time slots (for example, PCMCLK must equal 2.048 MHz if PCMFS=8 KHz). The time slot organization is independent of the compression/expansion bit rate selected. NOTE: Time slots are counted from the first rising edge of either PC MCLK or CPXCLK after the frame sync rising edge at PCMFS or CPXFS.

DS2130 CPX–SIDE INTERFACE Figure 8



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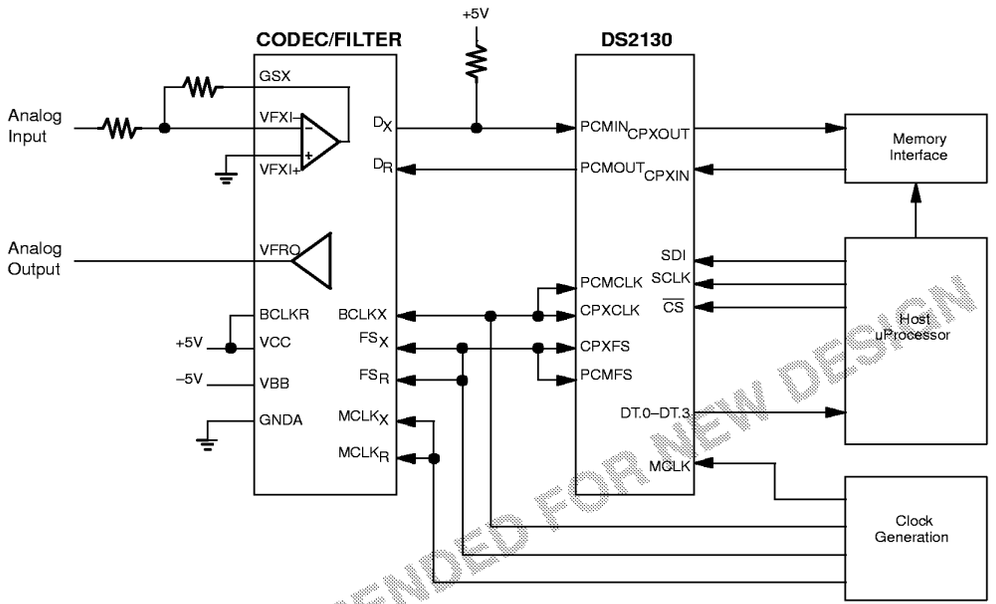
DS2130 CONNECTION TO CODEC/FILTER Figure 9



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NOTE:
Suggested Codec/Filters

TP305X	National Semiconductor
ETC505X	SGS–Thomson Microelectronics
MC1455XX	Motorola
TCM29CXX	Texas Instruments
HD44238C	Hitachi

*other generic Codec/Filter devices can be substituted.

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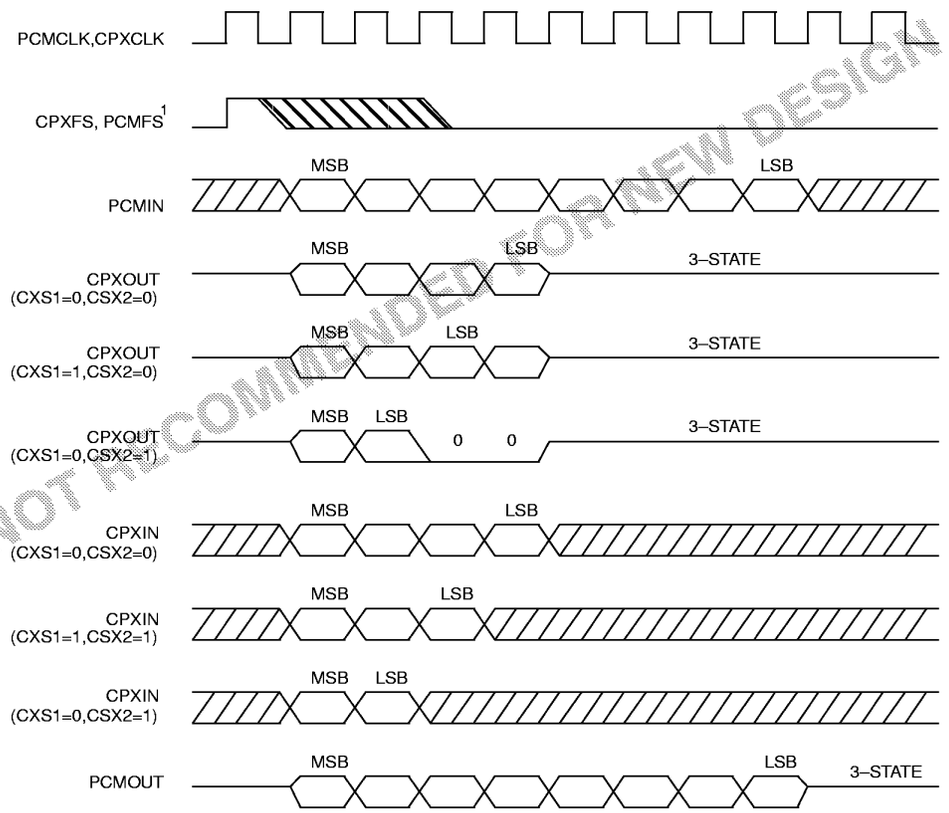
PCM AND CPX INPUT/OUTPUT

The organization of the CPX–side input and output time slots on the DS2130 depends upon the state of bit CXS3 in the VCR. When CXS3=0, all time slots for CPXOUT and CPXIN are four bits wide; when CXS=1,all time slots are eight bits wide. Also, when CXS3=1, all CPXOUT data is repeated in the next CPXFS sample; therefore, only one out of every two CPXOUT samples needs to be actually used. However, CPXIN data must be repeated twice when CXS3=1.

PCM–side time slots are always eight bits wide, regardless of CXS3. Figure 10 demonstrates how the DS2130 handles the I/O when CXS3=0; Figure 11 likewise shows the I/O when CXS3=1. It is assumed in both figures that the input and output time slots for both channels are set to zero.

PCM/CPX I/O (CXS3=0) Figure 10



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NOTE:

1. The CPXFS and PCMFS frame sync pulses must be at least 1 CPXCLK or PCMCLK high.

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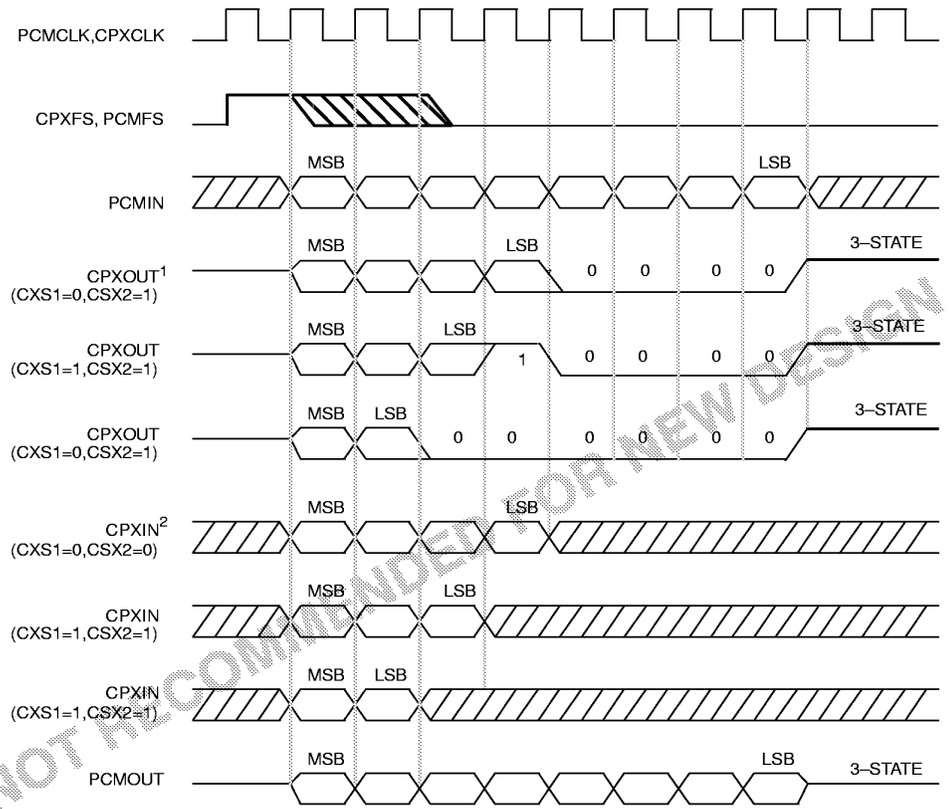
PCM/CPX I/O (CXS3=1) Figure 11



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NOTES:

1. When CXS3=1, all CPX–side time slots are eight bits wide and CPXOUT data samples are repeated in the next CPXFS frame sync during the same time slot. Therefore, only alternate data samples need to actually be used for host processing.
2. When CXS3=1, all CPXIN data must be repeated in next frame sync (CPXFS).

INPUT TO OUTPUT DELAY

With all compression algorithms, the total delay from the time the PCM data sample is captured by the DS2130 to the time it is output is always less than 375 µs. The exact delay is determined by the input and output time slots selected for each channel.

ON–THE–FLY ALGORITHM SELECTION

The user can switch between the three available algorithms on–the–fly. That is, the DS2130 does not need to be reset or stopped to make the change from one algorithm to another. However, the CXRST bit in the Voice Control register must be set to a one when making the algorithm change. The DS2130 reads the Control register before it starts to process each PCM or CPX sample. If the user wishes to switch algorithms, then the Voice Control register must be updated via the serial port before the first input sample to be processed with the new algorithm arrives at either PCMIN or CPXIN. PCM and ADPCM outputs will tristate during register updates.

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SPECIAL CLOCK REQUIREMENTS

The minimum number of clock transitions at CPXCLK and PCMCLK is nine per every CPXFS and PCMFS period (one for clocking the frame sync pulse and eight for the PCM or CPX data bits). When using this minimum number, please note that all nine clocks must occur within 1/3 of the total PCMFS/CPXFS period. For example, if CPXFS=8 KHz, then nine CPXCLK clocks must be received within 41.7 µs after the rising edge of CPXFS. The CPXCLK pin can remain idle until the next CPXFS rising edge.

When the DS2130 is placed in the power–down mode (CPD1=CPD2=1), the serial port must be subsequently clocked at less than 39 KHz (at SCLK) to write new data. Once the power–down mode is exited, the serial port can be operated at full speed again.

DTMF/ENERGY DETECTION

The DS2130 provides continuous detection of DTMF signals as well as monitoring of signal levels received at PCMIN. The only exception is when CPD1 and CPD2 are both set to one, which disables all DSP activity. The detect outputs, DT0–DT3 as shown in Table 5, indicate when DTMF digits have been detected and when certain energy thresholds have been exceeded. DTMF digits always take precedence over energy monitoring. For example, if a voice signal is present, only the states 1100 through 1111 are possible since DTMF signals are not present. When a DTMF digit is detected, the code for that digit will appear at DT0–DT3 for the duration of the signal. When the digit is no longer present, DT0–DT3 will return to one of the four possible energy detect states (1100 – 1111). It is recommended that these outputs be scanned at a rate no slower than 30 mS to avoid missing a digit since a DTMF burst may be as short as 50 ms. If the digit is generated only by a keypad depression, then a slower sample rate can be used.

As shown in Figure 1, the energy detector monitors the output of the DTMF low–band filter, which is a low–pass filter with a breakpoint at 1 KHz. The fundamental power spectrum of speech is typically in the range of 500 – 1000 Hz so that the energy detector can be used as an indication of voice level strength. This information can be used to determine if the gain in the analog front–end needs to be increased or when to stop recording. The energy detector integrates the signal over a 10 mS period.

As shown in Figure 9, a Data Valid signal for interrupting a processor can be created by simply ANDing the DT2 and DT3 outputs together. The output of the AND gate will go low whenever a DTMF digit is detected.

NOT RECOMMENDED FOR NEW DESIGN

DETECT OUTPUT CODING[1] Table 4

DT3–DT0	DESCRIPTION
0000	DTMF digit “0” detected.
0001	DTMF digit “1” detected.
0010	DTMF digit “2” detected.
0011	DTMF digit “3” detected.
0100	DTMF digit “4” detected.
0101	DTMF digit “5” detected.
0110	DTMF digit “6” detected.
0111	DTMF digit “7” detected.
1000	DTMF digit “8” detected.
1001	DTMF digit “9” detected.
1010	DTMF digit “*” detected.
1011	DTMF digit “#” detected.
1100	Vin > -15 dBm0
1101	-15 > Vin > -25 dBm0
1110	-25 > Vin > -40 dBm0
1111	-40 > Vin

1. Zero dBm0 is defined as the PCM signal level, which is 3 dB below the maximum PCM level.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	
Logic 0	V_{IL}	–0.3		+0.8	V	
Supply	V_{CC}	4.5		5.5	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			10	pF	

NOT RECOMMENDED FOR NEW DESIGN

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{DDA}		20		mA	1, 2
Power-Down Current	I_{DDPD}		1		mA	1, 2, 3
Input Leakage	I_{ILK}	–1.0		+1.0	µA	
Output Leakage	I_{OLK}	–1.0		+1.0	µA	4
Output Current (2.4V)	I_{OH}	–1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. PCMCLK= CPXCLK = 2.048 MHz; MCLK = 12 MHz.
2. Outputs open; inputs swinging full supply levels.
3. Control register bits CPD1= CPD2 = 1.
4. PCMOUT and CPXOUT are tri-stated.

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DTMF RECEIVER CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid Detect Amplitude Range		–40		0	dBm0	1, 2
Frequency Deviation Accept		±1.5			%	3
Frequency Deviation Reject		±3.5			%	3
Minimum Twist Accept Range		–10		+10	dB	4
Talk Off (Mitel Test Tape #CM7291)			5		Hits	5
Noise Tolerance (Mitel Test Tape #CM7291)			–12		dB	6

NOTES:

1. All DTMF receiver tests performed using test circuit shown in Figure 12.
2. Individual tone level of the DTMF pair.
3. Percent of nominal frequency for the individual tone.
4. Twist = 20 LOG (Hi tone/Lo tone).
5. Talk Off is a measure of the speech immunity of a DTMF receiver; the lower the number of hits, the better the immunity.
6. Three KHz bandlimited white noise, referenced to lowest amplitude tone in the DTMF pair.

NOT RECOMMENDED FOR NEW DESIGN

DTMF RECEIVER TIMING

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Tone Duration Accept	t_{TAC}	40			ms	1
Tone Duration Reject	t_{TRJ}			20	ms	
Interdigit Pause Accept	t_{PAC}	40			ms	
Interdigit Pause Reject	t_{PRJ}			20	ms	
Detect Delay (DT0–3)	t_{DTD}	25		45	ms	

NOTE:

1. See Figure 13 for DTMF receiver timing diagrams.

DTMF/TONE GENERATOR CHARACTERISTICS

(0°C to 70°C; V_{CC} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DTMF Frequency Deviation (each tone of the pair)				±1.0	%	1, 2
DTMF High Tone Level			–6.0		dBm0	
DTMF Low Tone Level			–6.0		dBm0	
Output Twist (DTMF only)			0.0		dB	
1004 Hz Tone Level			0.0		dBm0	
620, 350 Hz Tone Level			–12.0		dBm0	
Output Distortion (single tone)				–25	dB	3

NOTES:

1. All tests performed using test circuit in Figure 12. Zero dBm0 = 1.231 Vrms with the Hitachi HD44238 codec/filter device.
2. PCMFS = CPXFS = 8.0 KHz ± 0.1%.
3. Total harmonic distortion relative to test tone signal.

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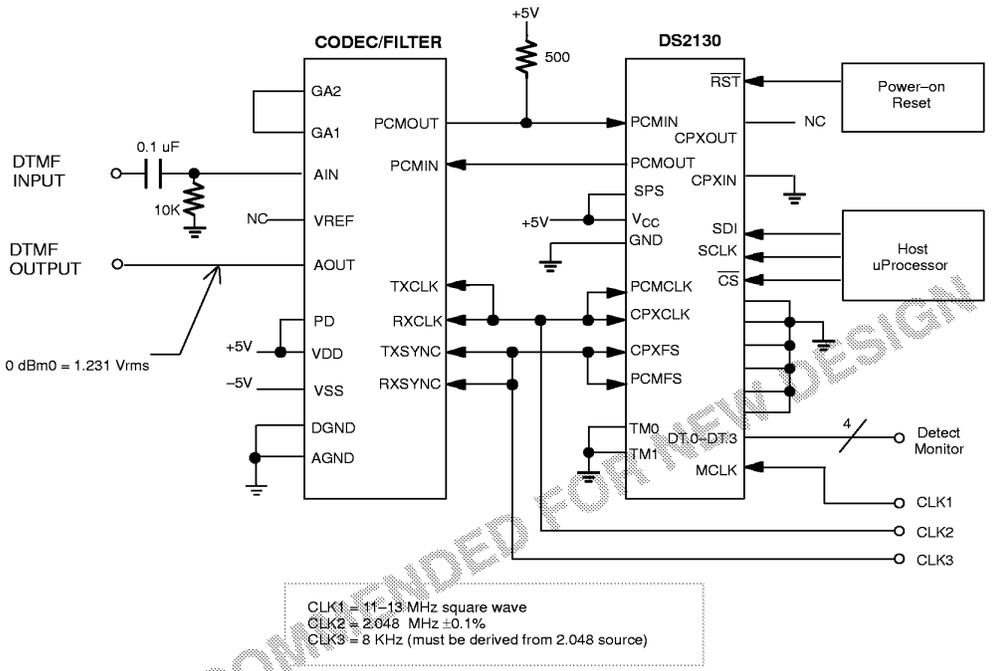
DTMF RECEIVER/GENERATOR TEST CIRCUIT Figure 12



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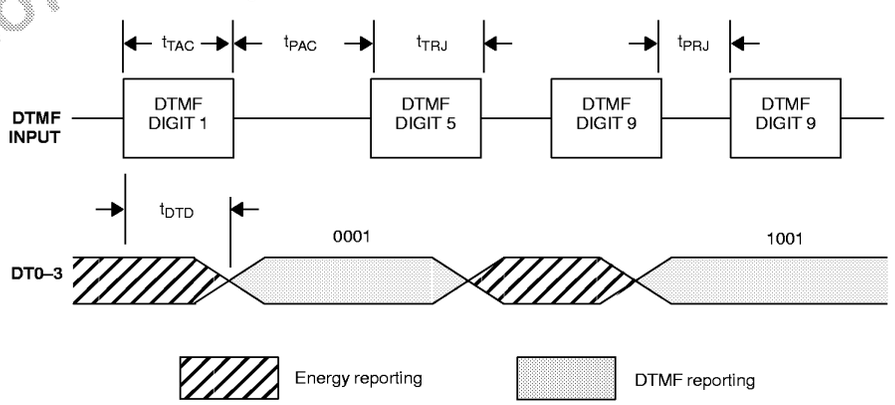
DTMF RECEIVER TIMING Figure 13



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PCM INTERFACE
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PCMCLK, CPXCLK Clock Period	t_P	244		5208	ns	1
PCMCLK, CPXCLK Pulse Width High	t_{WH}	100			ns	
PCMCLK, CPXCLK Rise, Fall Times	t_R t_F	10	20		ns	
Hold Time from PCMCLK, CPXCLK to PCMFS, CPXFS	t_{HOLD}	0			ns	2
Setup Time from PCMFS, CPXFS high to PCMCLK, CPXCLK low	t_{SF}	50			ns	2
Hold Time from PCMCLK, CPXCLK Low to PCMFS, CPXFS Low	t_{HF}	100			ns	2
Setup Time for PCMIN, CPXIN to PCMCLK, CPXCLK Low	t_{SD}	50			ns	2
Hold Time for PCMIN, CPXIN to PCMCLK, CPXCLK Low	t_{HD}	50			ns	2
Delay Time from PCMCLK, CPXCLK to Valid PCMOUT, CPXOUT	t_{DO}	10		150	ns	3
Delay Time from PCMCLK, CPXCLK to PCMOUT, CPXOUT 3-stated	t_{DZ}	20		150	ns	2, 3, 4

NOT RECOMMENDED FOR NEW DESIGN

NOTES:

1. At least nine CPXCLK(or PCMCLK) clocks must be received within 1/3 of the CPXFS (or PCMFS) period.
2. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.
3. Load = 150 pF + 2 LSTTL loads.
4. For LSB of PCM or CPX word.

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MASTER CLOCK/RESET
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
MCLK Period	t_{PM}	75		95	ns	1
MCLK Duty Cycle (t_{WMH} / t_{WML}+ t_{WMH})		45		55	%	
MCLK Rise/Fall Times	t_{RM} t_{FM}			10	ns	
RST Pulse Width	t_{RST}	1			ms	

NOTE:
1. MCLK = 10.5 to 12.5 MHz typically.

SERIAL PORT
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
SDI to SCLK Setup	t_{DC}	55			ns	1
SCLK to SDI Hold	t_{CDH}	55			ns	1
SCLK Low Time	t_{CL}	250			ns	1
SCLK High Time	t_{CH}	250			ns	1
SCLK Rise and Fall Time	t_R, t_F			100	ns	1
CS to SCLK Setup	t_{CC}	50			ns	1
SCLK to $\overline{CS}$ Hold	t_{CCH}	250			ns	1
CS Inactive Time	t_{CWH}	250			ns	1
SCLK Setup to $\overline{CS}$ Falling	t_{SCC}	50			ns	1

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NOTE:
1. Measured at V_{IH} = 2.0V, V_{IL} = 0.8V, and 10 ns maximum rise and fall times.

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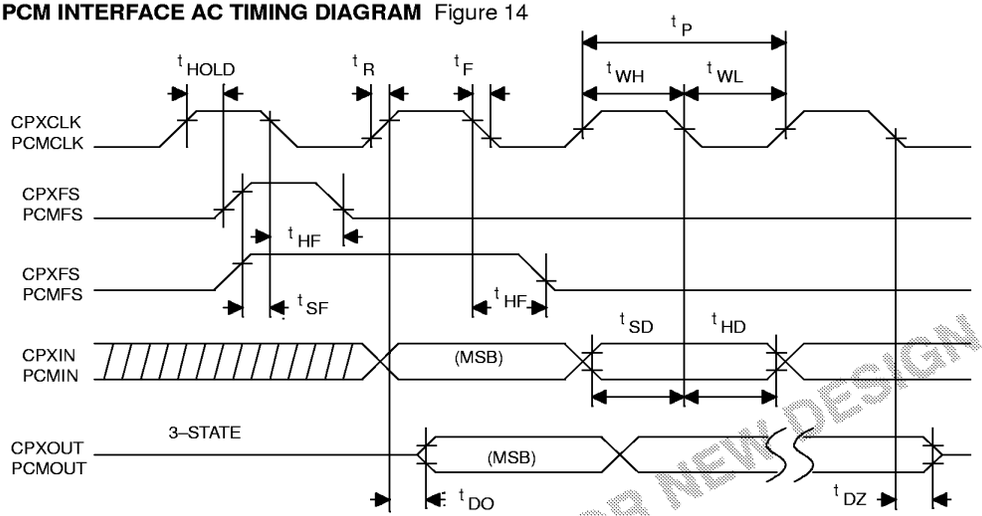
PCM INTERFACE AC TIMING DIAGRAM Figure 14



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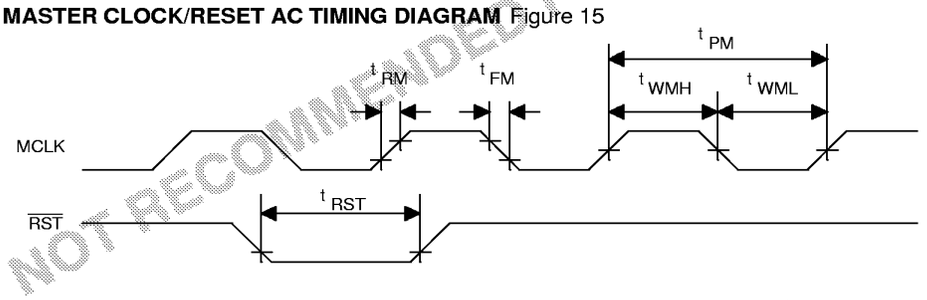
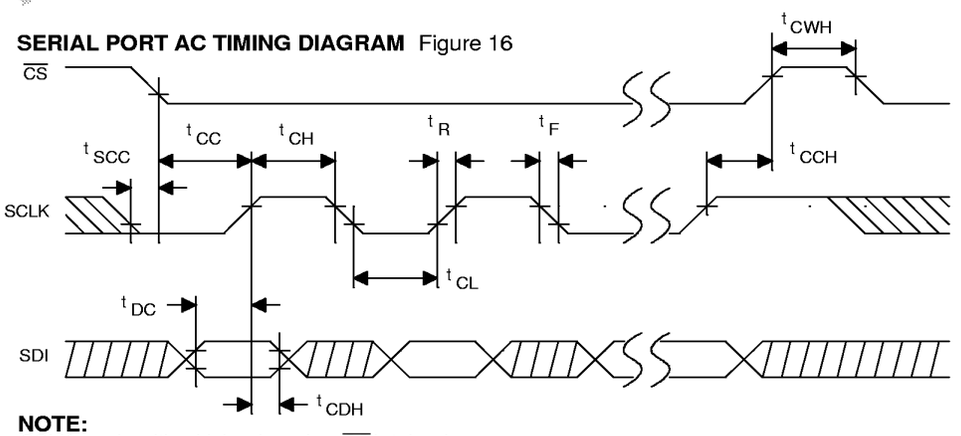
MASTER CLOCK/RESET AC TIMING DIAGRAM Figure 15



SERIAL PORT AC TIMING DIAGRAM Figure 16



NOTE:
SCLK may be either high or low when $\overline{CS}$ is taken low.

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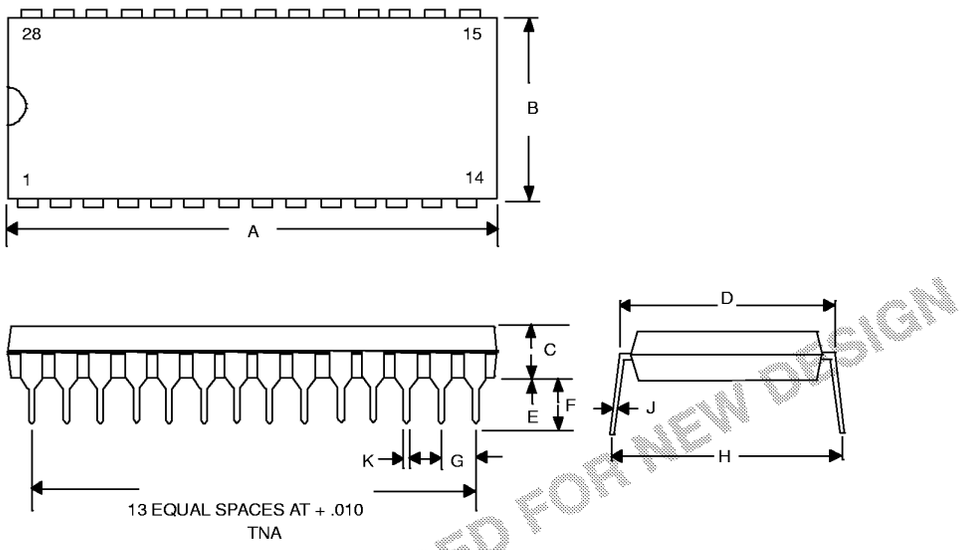
DS2130 VOICE MESSAGING PROCESSOR 28–PIN DIP



DIM	INCHES	
	MIN	MAX
A	1.240	1.280
B	0.540	0.560
C	0.140	0.160
D	0.590	0.610
E	0.020	0.040
F	0.110	0.130
G	0.090	0.110
H	0.600	0.680
J	0.008	0.012
K	0.015	0.021

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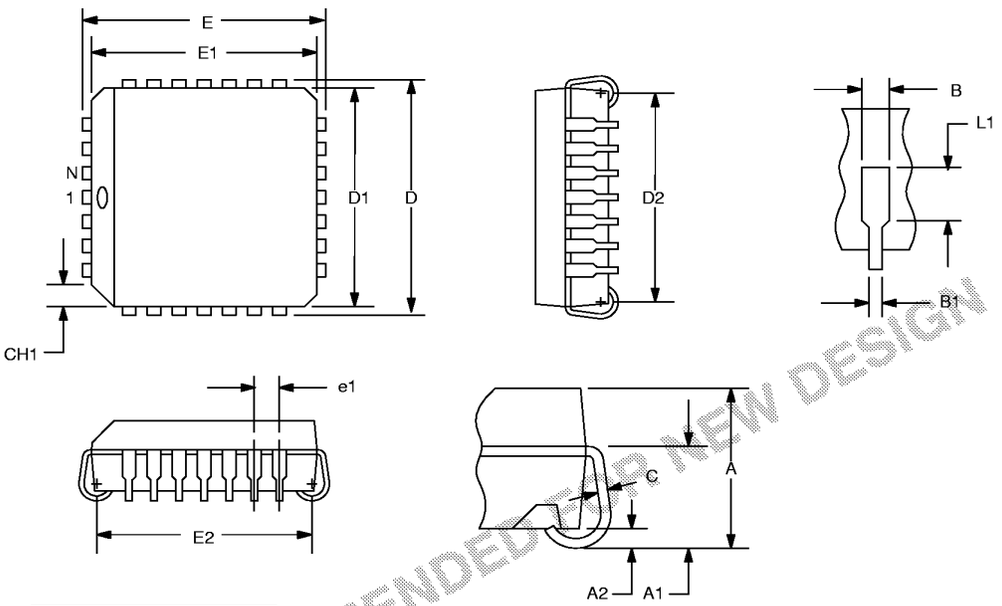
DS2130Q VOICE MESSAGING PROCESSOR 28–PIN PLCC



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DIM	INCHES	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A2	0.020	–
B	0.026	0.033
B1	0.013	0.021
C	0.009	0.012
D	0.485	0.495
D1	0.450	0.456
D2	0.390	0.430
E	0.485	0.495
E1	0.450	0.456
E2	0.390	0.430
L1	0.060	–
N	28	–
e1	0.050 BSC	
CH1	0.042	0.048

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