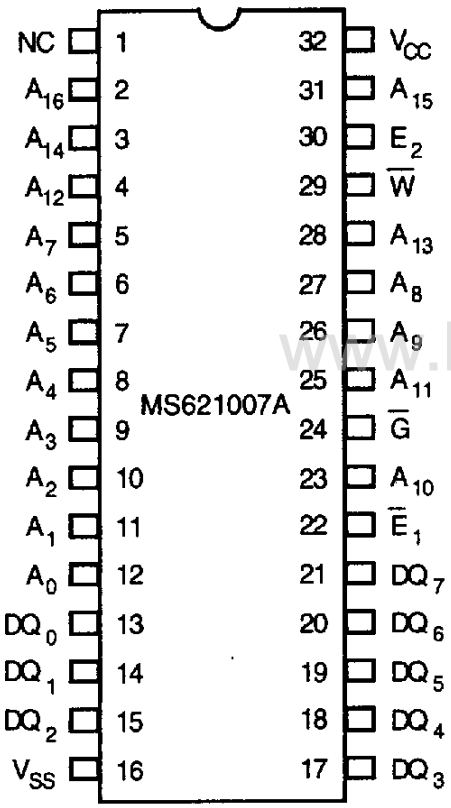
MOSEL VITELIC

MS621007A
128K x 8 CMOS STATIC RAM

Features

- Fast Access Times: 20/25/35 ns
- Two Chip Enable Controls
- Low-Power Standby When Deselected
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention
- Package: 32-Pin, 400-mil SOJ

Pin Configuration



Description

The MS621007A is a high speed 1,048,576-bit static RAM organized as 128K x 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

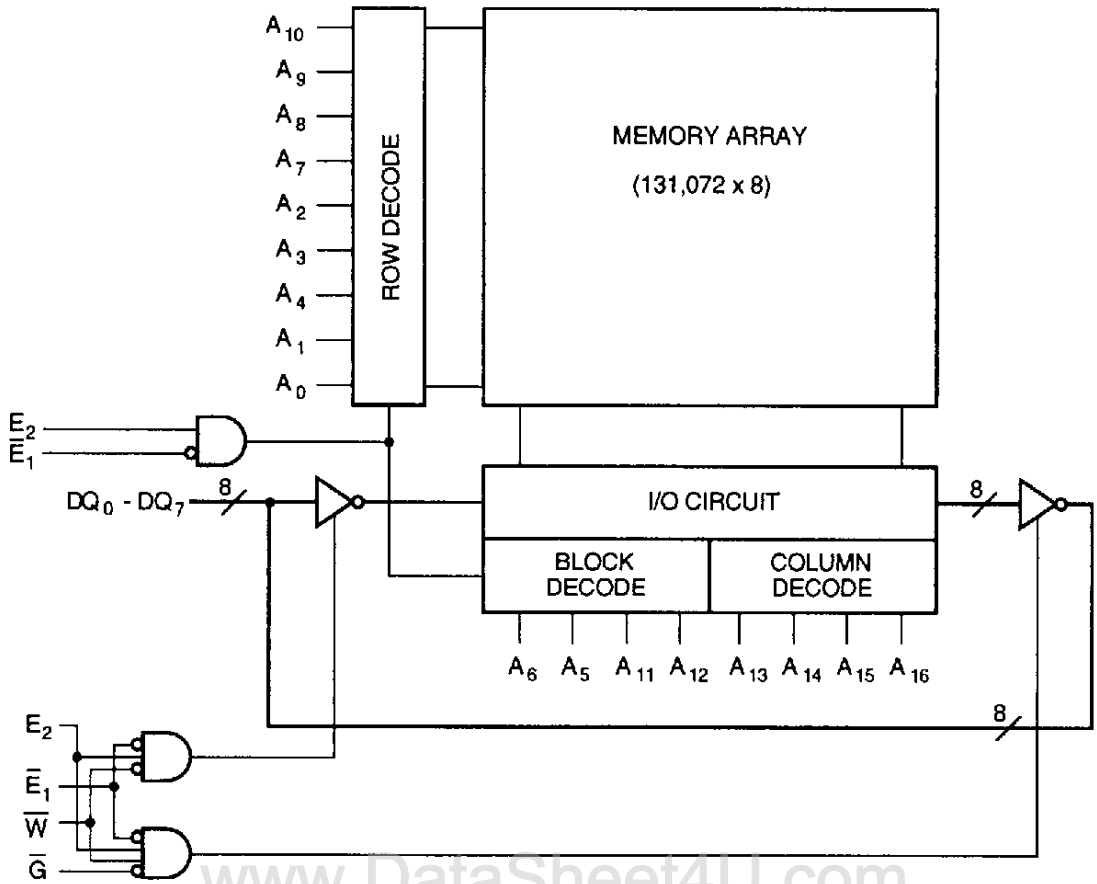
This RAM is fully static in operation. The Chip Enables ($\overline{E}_1$, E_2) permit Read and Write operations when active ($\overline{E}_1$ = LOW and E_2 = HIGH) or place the RAM in a low-power standby mode when inactive ($\overline{E}_1$ = HIGH or E_2 = LOW). Standby power drops to its lowest level when all inputs are stable and are at CMOS levels, while the chip is in standby mode.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable Control ($\overline{G}$) can prevent bus contention.

When both Chip Enables are active and $\overline{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

Functional Block Diagram



Pin Descriptions

A_0–A_{16} Address Inputs
These 17 address inputs select one of the 128K x 8 bit segments in the RAM.

DQ_0–DQ_7 Data Input and Data Output Ports
These 8 bidirectional ports are used to read data from and write data into the RAM.

$\overline{E}1$, E_2 Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory locations.

V_{CC} Power Supply

V_{SS} Ground

Truth Table

E_1	$\overline{E}_2$	$\overline{G}$	$\overline{W}$	Mode	DQ	I_{CC}
H	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

Absolute Maximum Ratings (1)

Parameter	Rating
V_{CC} to V_{SS} Potential	-0.5V to 7 V
Input Voltage Range	-0.5 V to V_{CC} + 0.5V
DC Output Current[2]	± 40 mA
Storage Temperature Range	-65°C to +150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

Operation Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage[1]	–0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTES:
1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC Electrical Characteristics

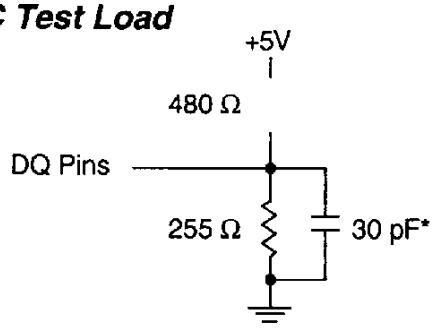
Symbol	Parameter	Test Conditions	Min.	Typ.[1]	Max.	Unit
I_{CC1}	Operating Current (2)	t_{CYCLE} = 20ns		115	180	mA
I_{CC1}	Operating Current (2)	t_{CYCLE} = 25ns		105	175	mA
I_{CC1}	Operating Current (2)	t_{CYCLE} = 35ns		95	165	mA
I_{SB1}	Standby Current	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IH}$ t_{CYC} = min, I_{OUT} = 0		12	25	mA
I_{SB2}	Standby Current	$\overline{E}_1 \geq V_{CC}$ – 0.2V or $E_2 \leq 0.2V$ t_{CYC} = min,		0.5	2	mA
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0V to V_{CC}	-2		2	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V
V_{DR}	Data Retention Voltage	$E_1 \geq V_{CC}$ – 0.2V and $E_2 \leq 0.2V$	2		5.5	V
I_{DR}	Data Retention Voltage	V_{CC} = 3V, $\overline{E}_1 \geq V_{CC}$ – 0.2V and $E_2 \leq 0.2V$			500	µA

NOTES:
1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC Test Conditions

Parameter	Rating
Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5V
Output Load, Timing Tests	Figure 3

AC Test Load



* Includes scope and jig capacitance

Capacitance (1,2)

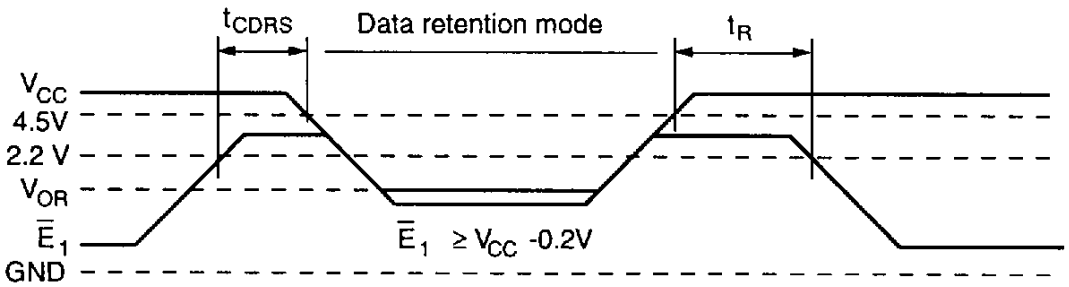
Parameter	Rating
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:
1. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Samples tested only.

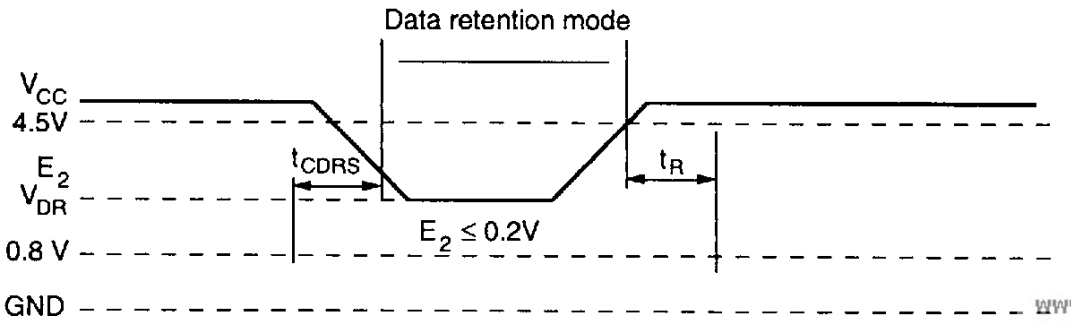
Data Retention Timing

For data retention mode, either $E_1 \geq V_{CC} - 0.2V$ or $E_2 \leq 0.2V$. The other control signals must be at valid CMOS levels ($V_{CC} - 0.2V \leq V_{IN} \leq 0.2V$). The address and data buses are 'Don't Care.'

Low Supply Voltage Data Retention Waveform (1) ($\overline{E}_1$ Control)



Low Supply Voltage Data Retention Waveform (2) (E_2 Control)



AC Electrical Characteristics (Over Operating Range) [1]

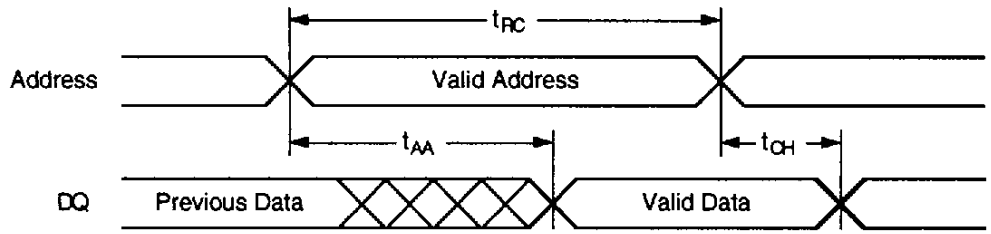
Parameter Name	Parameter	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Units
Read Cycle								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	Chip Enable to Valid Data		20		25		35	ns
t_{ELZ}	Chip Enable to Output Active [2, 3]	5		5		5		ns
t_{EHZ}	Chip Disable to Output High-Z [2, 3]		8		10		15	ns
t_{GA}	$\overline{G}$ Low to Valid Data		7		8		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2, 3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2, 3]		8		10		20	ns
t_{PU}	Chip Enable to Power Up Time [4]	0		0		0		ns
t_{PD}	Chip Disable to Power Down Time [4]		20		25		35	ns
Write Cycle								
t_{WC}	Write Cycle Timing	20		25		35		ns
t_{EW}	Chip Enable to End of Write	13		15		20		ns
t_{AW}	Address Valid to End of Write	13		15		20		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	13		15		20		ns
t_{DW}	Input Data Setup Time	9		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2, 3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2, 3]	5		5		5		ns

NOTES:
1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to active output tests specified for a ±500mV transition from steady levels into the test load. C_{LOAD} = 5 pF.
3. Sample tested only.
4. Guaranteed but not tested.

Switching Waveforms—Read Cycle

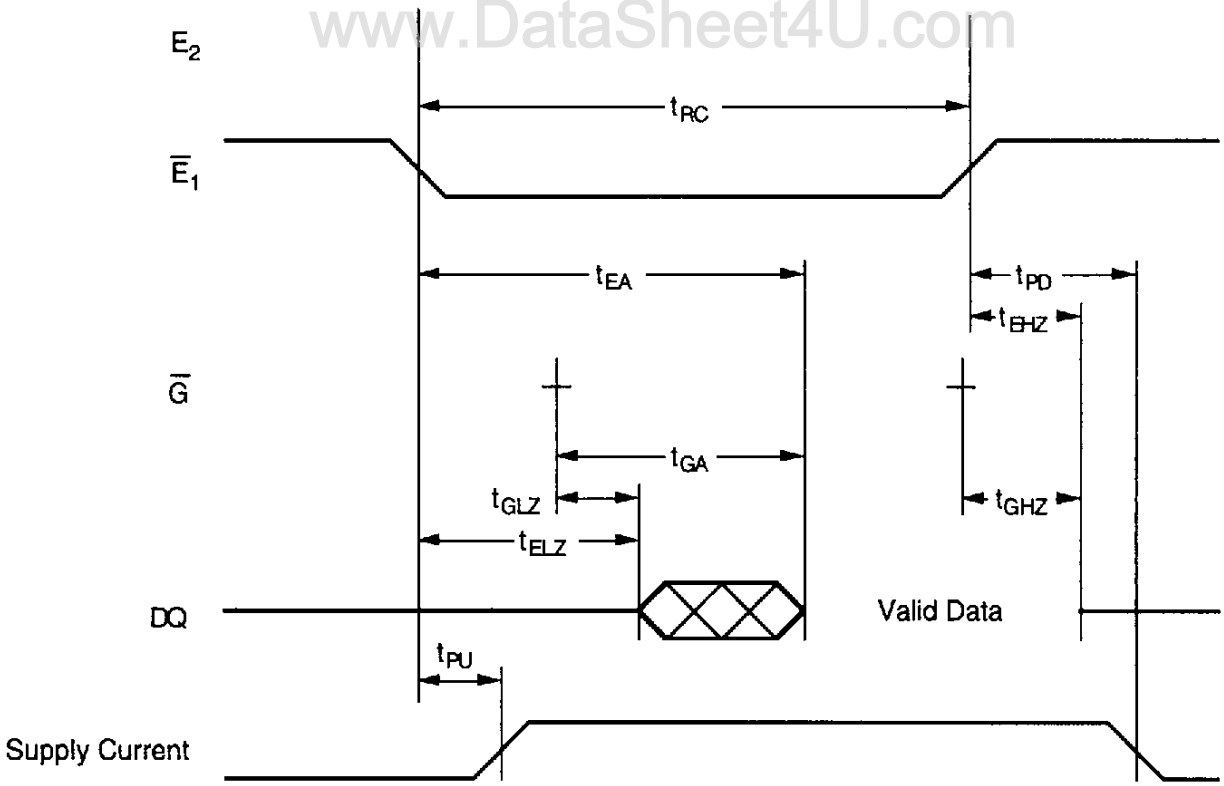
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, and $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data-out implies that data lines are in Low-Z state but the data is not guaranteed to be valid until t_{AA}.



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

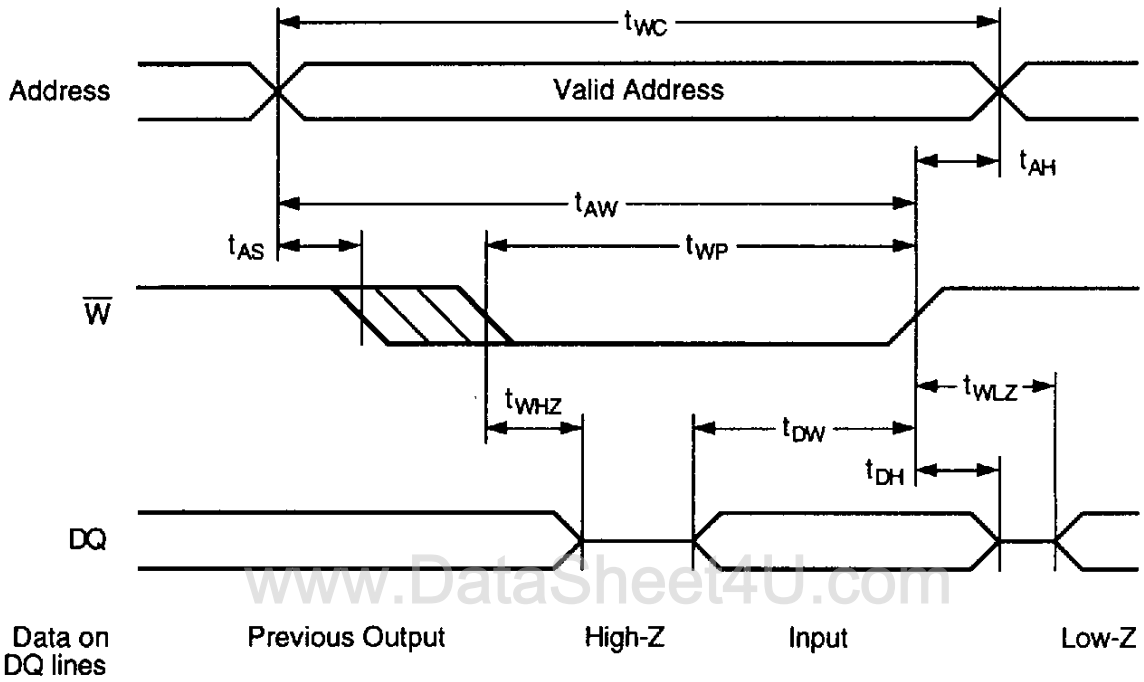


Switching Waveforms—Write Cycle

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, The outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Writes cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

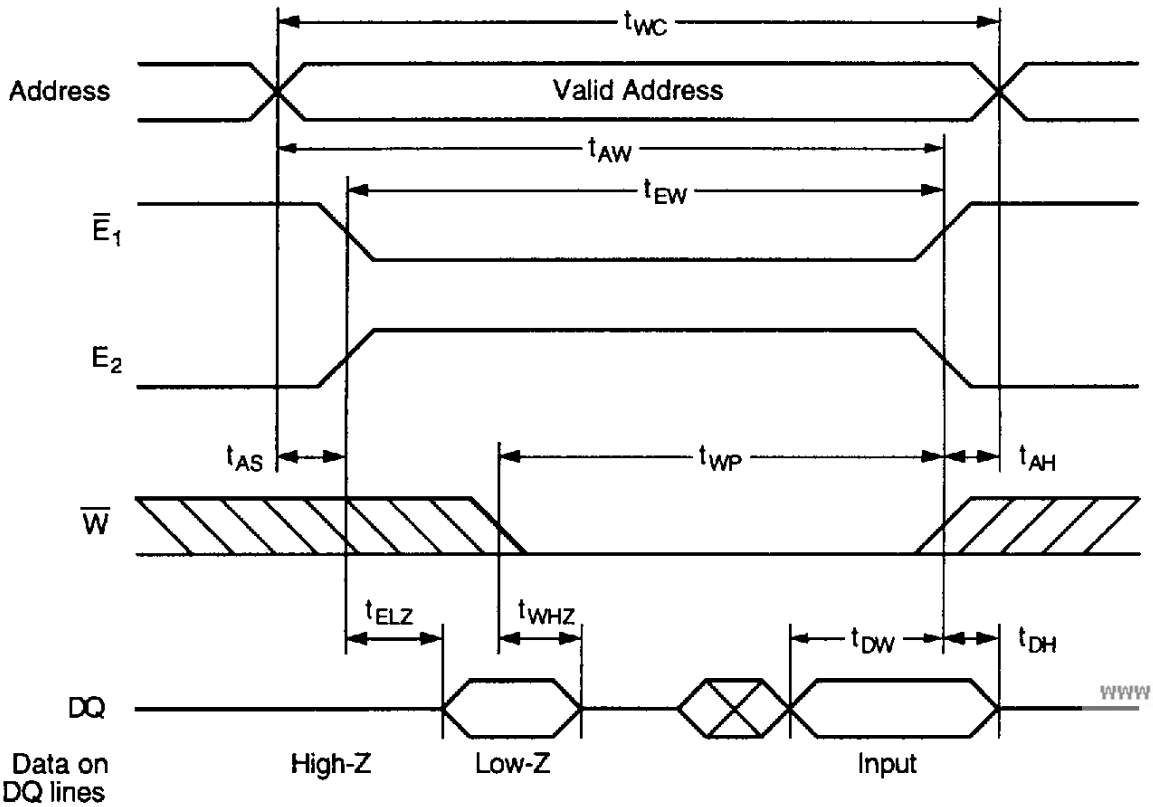
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles may not offer the best performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



Ordering Information

Speed (ns)	Ordering Part Number	Package	Temperature Range
20	MS621007A-20K	32 Pin 400 mil SOJ	0°C to +70°C
25	MS621007A-25K	32 Pin 400 mil SOJ	0°C to +70°C
35	MS621007A-35K	32 Pin 400 mil SOJ	0°C to +70°C