LSI LOGIC

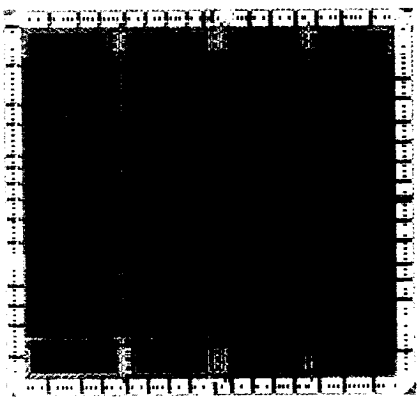
L64245
Versatile FIR Filter
Preliminary

Description

The L64245 FIR (Finite Impulse Response) filter processor performs filtering in many different forms for applications ranging from broadcast-quality video transmission and HDTV to disk drives and digital microwave. To support these applications, the L64245 can implement a wide variety of filter structures, ranging from decimators and interpolators to interleaved and complex filters.

The processor accommodates both real and complex (I and Q) data types, and it is ideally suited for applications with up to 10 bits of data precision and data rates from 5 to 40 MHz. The L64245 can implement 1-D (one-dimensional) filters over a wide range of data sample rates and filter lengths, as well as some 2-D (two-dimensional) filters. In all cases, the device operates from a single clock.

Each L64245 contains 26 *tap cells*. Each tap cell includes a 40 MHz, 10 x 10 multiplier-accumulator (MAC) and eight coefficient registers. These resources make it possible to implement real data filters ranging from 208 taps at 5 MHz to 26 taps at 40 MHz. In each case, as either the input or output data rate drops below the clock rate, the number of filter taps increases.



L64245 Die

The L64245 may be controlled with a simple external state machine. Note that any coefficient that is not being accessed by a multiplier can be updated without affecting the operation of the filter processor.

Features

- Twenty-six 10 x 10 MACs (multiplier-accumulators)
- Flexible architecture with 208 coefficient latches
- Supports real and complex filters
- Performs interpolation and decimation
- Processes up to eight independent interleaved data streams
- Implements 1-D- or 2-D filters
- Provides a simple system interface and control
- Operates at 30/40 MHz data rates
- Fully static operation
- Supplied in a 68-pin CPGA or PPGA (Ceramic or Plastic Pin Grid Array) package

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Order Number H15013

Processor Architecture

The L64245 computes a 26-point inner product during each clock cycle. The inner product is computed between 26 data input values and 26 coefficients. This capability makes the L64245 able to compute a wide range of FIR filters of the type:

$$y(n) = \sum h_i x(n-i)$$

where the number of filter taps is a function of the input and output data rates and the data type (real or complex).

Figure 1 shows a high-level block diagram of the L64245. The processor is organized as a cascade of 26 basic filter tap cells, where each tap cell computes one point of the inner product per cycle. Products are accumulated when RESET is LOW, and the 28-bit accumulator output is latched for output when RESET is HIGH. From the 28 bits available at the accumulator output, the internal control bits BSEL.3:0 select 16 bits for output from the processor. The bit-select and round logic provides the user with these 16 bits, rounded, at the processor output.

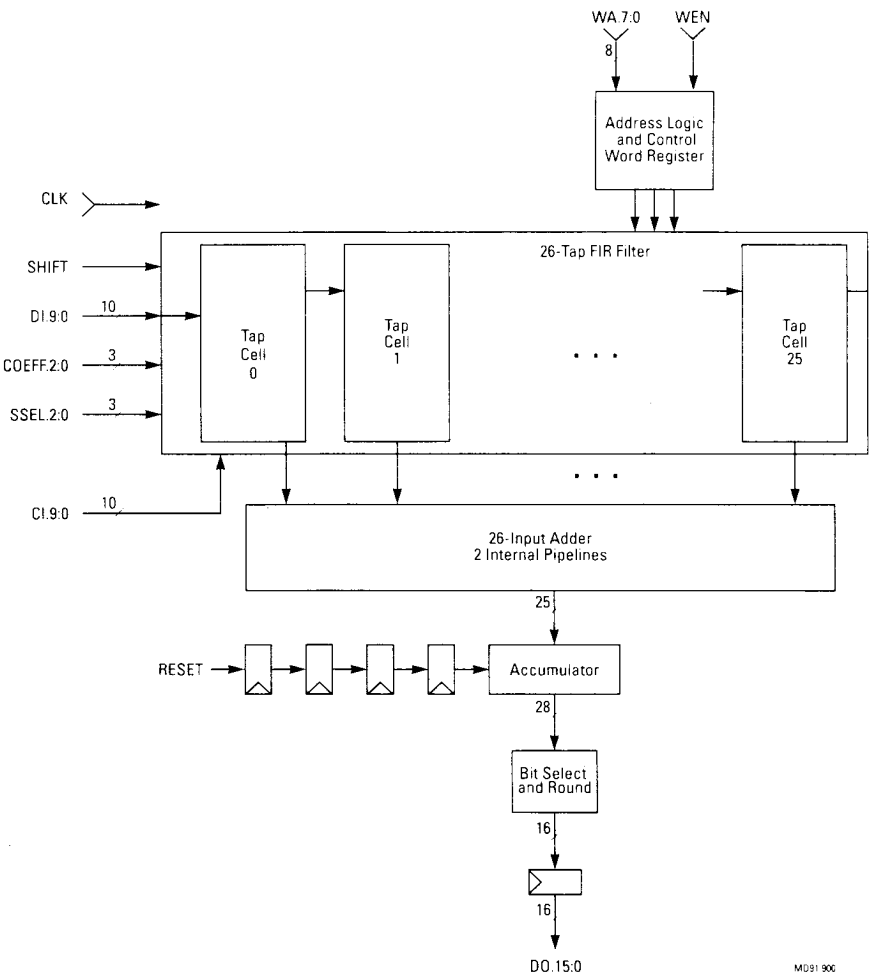


Figure 1. L64245 Block Diagram

Processor Architecture (Continued)

Note that the L64245 utilizes two types of flip flops. One is a standard positive-edge triggered flip flop with clock, while the other is a load/hold flip flop. The load/hold flip flop loads a new value at the rising edge of the clock when the enable signal is HIGH: otherwise, it holds its previous value. Figure 2 shows the flip flop symbols as used in the L64245 block diagrams and the equivalent circuit for each symbol.

The Tap Cell

Figure 3 shows a more detailed diagram of a single tap cell. Each tap cell consists of a 10 x 10 multiplier-accumulator (MAC) and eight coefficient registers. The COEFF.2:0 signals select the current multiplier coefficient. For applications requiring 104 or fewer real coefficients, the coefficient registers can be divided into two sets to effectively double-buffer the coefficients. The active set is used to generate the output data, while the loading set can be updated without disturbing the operation of the filter processor. After a new set of coefficients is loaded, the two sets can be swapped and the procedure repeated. Both sets of coefficients remain available in the processor, and either set can be selected at any time.

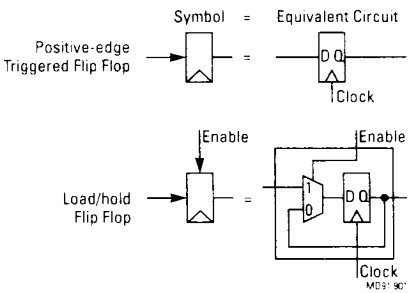


Figure 2. Flip Flops

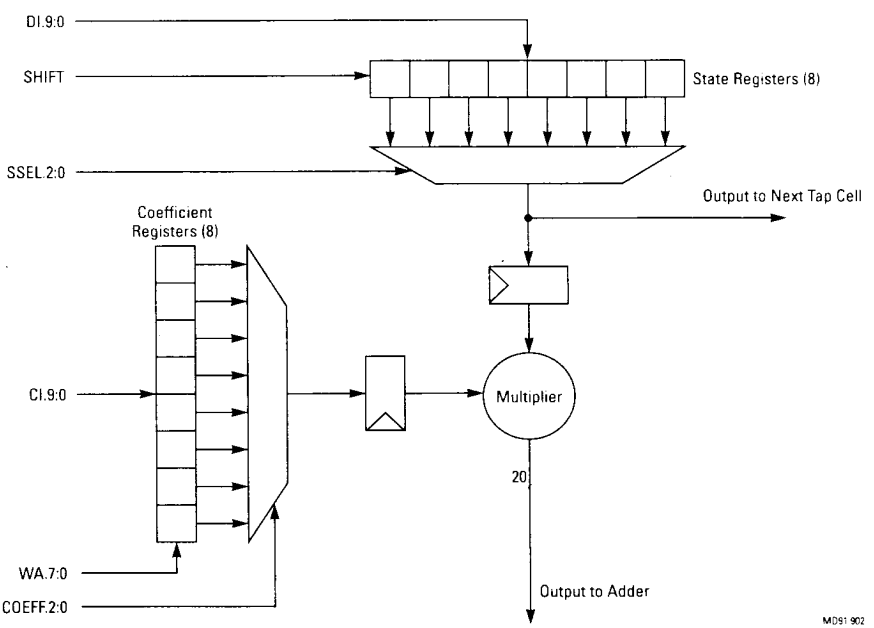


Figure 3. Tap Cell Block Diagram

Processor Architecture (Continued)

Figure 4 presents a more detailed diagram of three adjacent tap cells, illustrating the interconnect.

It is important to note that Figures 3 and 4 are valid only when the following condition is met:

$$SSEL = 2^{STATES} - 1 \text{ whenever SHIFT is HIGH}$$

where $STATES_{10}$, which represents the number of states accessed by each multiplier (see Table 4 on page 6), equals 0, 1, 2 or 3. With this constraint, the SSEL sequences are the simple sequences, as discussed and illustrated in the Application Examples section on pages 8-12 (see in particular Tables 8, 11 and 12). The L64245 can also be used in applications where the number of states accessed is not a power of two, that is 3, 5, 6 or 7. The SSEL sequencing becomes more complex, but the L64245 can operate at higher data rates than if the user simply increased the number of states to the next power of two. Refer to the Advanced Application Example section (pages 13-14) in this datasheet for more information on this topic.

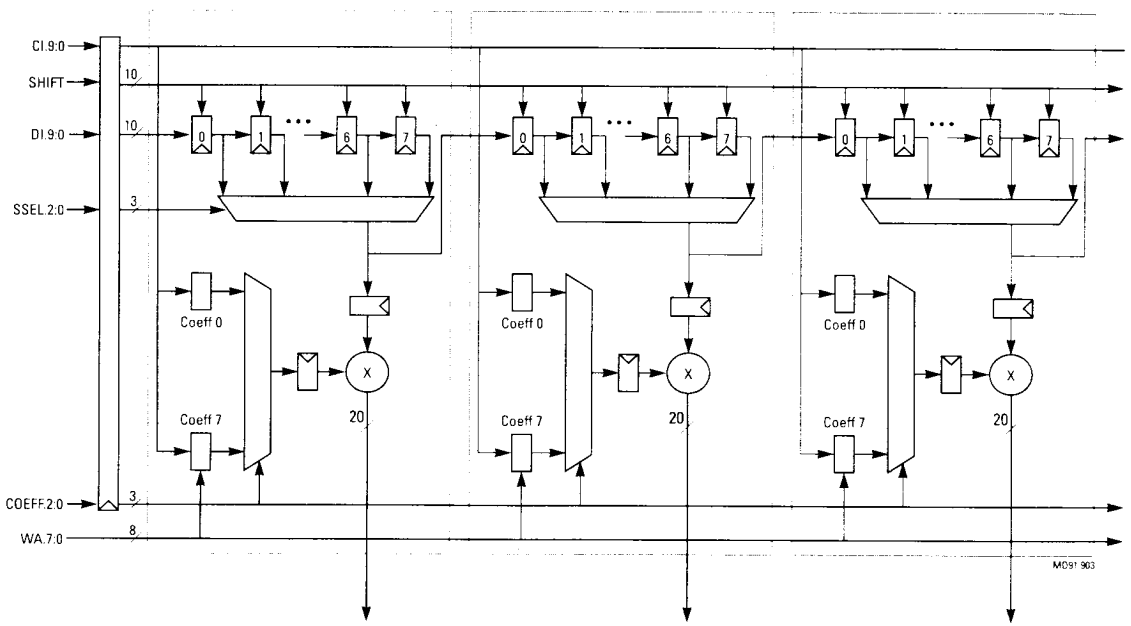


Figure 4. Three-Tap Block Diagram

Pin Listing and Description

This section describes the signals that comprise the I/O interface to the L64245. Note that zero is always the least significant bit (LSB). Figure 5 shows the L64245 logic symbol, and signal descriptions follow the figure. Table 1 then provides a pin description summary.

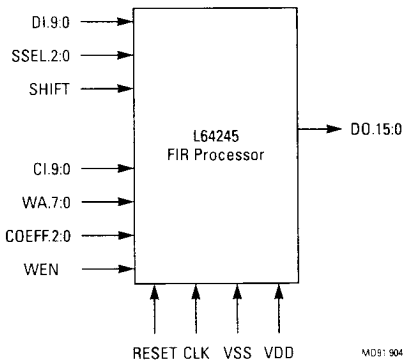


Figure 5. L64245 Logic Symbol

CI.9:0
Coefficient Input Bus (Input) – When WEN goes LOW, the values on this 10-bit signed integer bus are loaded into the coefficient register specified by WA.7:0.

CLK
System Clock (Input) – This signal is the system clock. Note that registers in the L64245 are clocked by the rising edge of CLK.

COEFF.2:0
Coefficient Select Inputs (Input) – All tap cells use, as the multiplier input, the coefficient in the register specified by COEFF.2:0.

DI.9:0
Data Input Bus (Input) – The 10-bit Data Input Bus presents the input data in a format determined by the DMODE bit in the internal control word. When DMODE is HIGH, the format is two's complement. When DMODE is LOW, the format is unsigned. Refer to the Control Word Format discussion in the Operation section, below, for more information.

DO.15:0
Data Output Bus (Output) – The 16-bit output data is selected and rounded from the full-precision, 28-bit result at the accumulator.

RESET
Reset (Input) – When RESET goes HIGH, the accumulator result is latched and reset for a new sum of products. When RESET goes LOW, the products are accumulated.

SHIFT
State Shift Register Shift Enable (Input) – When SHIFT is HIGH, the rising edge of CLK shifts the data in the state shift register. When SHIFT is LOW, the data are held instead of shifted by the rising edge of CLK.

SSEL.2:0
State Select Inputs (Input) – These three bits specify which state in each tap is being accessed both as input to the multiplier and as input to the state shift register in the next tap.

WA.7:0
Write Address Bus (Input) – From this eight-bit Write Address Bus, the 5 MSBs select the tap cell and the 3 LSBs select the coefficient register for the write. When WA.7:0 = 255, the control word is written instead of a coefficient. Note that the coefficient or control word is written when WEN goes LOW.

WEN
Write Enable (Input, Active-LOW) – When WEN goes active (LOW), data on CI.9:0 are written either into the appropriate coefficient register or, if WA.7:0 = 255, into the control word.

Table 1. Pin Description Summary

Pin	No. of Pins	I/O	Description	Pin	No. of Pins	I/O	Description
CI.9:0	10	Input	Coefficient input bus	RESET	1	Input	Accumulator reset control
CLK	1	Input	System clock	SHIFT	1	Input	State register shift enable
COEFF.2:0	3	Input	Coefficient select inputs	SSEL.2:0	3	Input	State shift register input select
DI.9:0	10	Input	Data input bus	WA.7:0	8	Input	Write address bus
DO.15:0	16	Output	Data output bus	WEN	1	Input	Write enable

Operation

This section discusses various aspects of L64245 operation, including loading of coefficients and the control word, data formats and internal precision, and controlling the processor timing.

Loading the Coefficients and the Control Word

Before normal filter operation can commence, the filter coefficients that the multipliers will access must be loaded into the processor. All the parameters are implemented in a memory-mapped fashion, as shown in Table 2, where WA.7:3 identify the tap cell (1 of 26), and WA.2:0 identify the coefficient register for the write (1 of 8). The data on CI.9:0 are latched into the internal register specified by WA.7:0 when WEN is LOW.

Table 2. Addressing for Coefficient Latches

Tap Cell WA.7:3	Coefficient Latch WA.2:0	Destination of CI.9:0
00000	000	TAP 0, Coefficient 7
	...	
00000	111	TAP 0, Coefficient 7
	...	
11001	000	TAP 25, Coefficient 0
	...	
11001	111	TAP 25, Coefficient 7
11111	111	Control Word Register

Note that WA.7:3 = 11010_2 through 11110_2 are reserved and should not be used.

Because the L64245 provides separate read address (COEFF.2:0) and write address (WA.7:0) buses as inputs, the user achieves full flexibility in coefficient loading. For example, while coefficient register 7 is being read in every tap cell (COEFF.2:0 = 111_2), a new coefficient can be written into any one of the other registers, that is, into any one of registers 0 through 6 of any tap cell, without corrupting the computation in progress.

When WA.7:0 equals 255 (11111111_2), the control word is written from the coefficient bus, as described next.

Control Word Format

The control word, shown in Figure 6, consists of the bits that identify the 16 output bits within the 28-bit accumulator result (BSEL.3:0), set the number of state registers accessed per tap (STATES.1:0), and control the data format for the data input bus (DMODE).

CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
BSEL.3:0				STATES.1:0		DMODE

MD91 905

Figure 6. Control Word Format

The BSEL bits control the selection and rounding of the required output bits from the internal 28-bit result, as detailed in Table 3. For example, if BSEL.3:0 = 0, then bits 3 to 18 from the accumulator are passed to the output. If BSEL.3:0 = 15 (1111_2), then only the 10 most significant bits (MSBs) are passed to DO.9:0. Note that if the BSEL bits select fewer than 16 bits for output, the L64245 sign-extends the data to 16 bits.

Table 3. BSEL.3:0 Accumulator Output Selection

BSEL.3:0	Selected Accumulator Output	BSEL.3:0	Selected Accumulator Output
0000	18:3	1000	26:11
0001	19:4	1001	27:12
0010	20:5	1010	27:13
0011	21:6	1011	27:14
0100	22:7	1100	27:15
0101	23:8	1101	27:16
0110	24:9	1110	27:17
0111	25:10	1111	27:18

The internal control bits STATES.1:0 indicate the number of available state registers per tap as defined in Table 4. The multiplier can access one of the available state registers in each cycle via SSEL.2:0. The data in the state registers are shifted whenever SHIFT is HIGH. Note that the SSEL.2:0 signals typically should specify the highest-numbered state being used when SHIFT is HIGH.

Table 4. Use of STATES.1:0

STATES.1:0	No. of State Registers	Highest State
11	8	7
10	4	3
01	2	1
00	1	0

Operation
(Continued)

The DMODE signal specifies two's-complement data when HIGH and unsigned data when LOW.

Data Formats and Internal Precision

The MAC inputs consist of 10-bit, two's-complement or unsigned integer data and 10-bit, two's-complement integer coefficients. The internal control signal DMODE, as mentioned above, specifies the data format for the MACs. The output data are always in two's-complement integer format.

Table 5 and Table 6 illustrate the processor internal precision for both signed and unsigned input data. The figures illustrate the internal formats for fractional numbers, where the magnitude of the numbers is strictly less than one; for integer data formats, move the binary point to the rightmost position of each word. In the figures, the *s* is a sign bit. Note that the processor performs all internal computations to full precision.

Controlling the Device and Internal Delays

For operation when either the input or output sample rate is less than the clock rate, the system must control the processor via the RESET, SHIFT, COEFF and SSEL pins. In general, each signal has been delayed internally to compensate for pipeline delays in the data path; note that all internal delays in the processor are accurately represented in the block diagrams above. As shown in Figure 3 (see page 3), the delay from the COEFF inputs to the multipliers is two clock cycles. The delay from the DI inputs to the multiplier input depends both on the shift time, which is the time between successive HIGH pulses on SHIFT, and on the order in which states are selected. In general, the data on the DI inputs when both SHIFT and RESET are HIGH is delayed to the DO outputs by N + 6 cycles, where N is the number of products accumulated for each output. The exact control signal sequences for most common applications are given in the following section.

Table 5. L64245 Internal Precision: Signed Data, Signed Coefficient

Bit Number:	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Input:																				s	.	b	b	b	b	b	b	b
Coefficient Input:																				s	.	b	b	b	b	b	b	b
Multiplier Input:	s	s	s	s	s	s	s	s	s	b	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b
Accumulator Input:	s	s	s	s	b	b	b	b	b	b	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b
Accumulator Output:	s	b	b	b	b	b	b	b	b	b	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b

Table 6. L64245 Internal Precision: Unsigned Data, Signed Coefficient

Bit Number:	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Input:																		0	.	b	b	b	b	b	b	b	b	b
Coefficient Input:																			s	.	b	b	b	b	b	b	b	b
Multiplier Input:	s	s	s	s	s	s	s	s	s	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b
Accumulator Input:	s	s	s	s	b	b	b	b	b	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b
Accumulator Output:	s	b	b	b	b	b	b	b	b	.	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b	b

Application Examples

This section provides several application examples to illustrate the versatility and power of the filter processor. Figure 7 shows a typical circuit that interfaces an L64245 to an eight-bit microprocessor; the circuit operation is explained below. The tables that follow the figure summarize various filter operations that can be performed with one or more L64245 processors, and detail the control signal and coefficient sequences for typical operations. Note that all of the table entries assume a 40 MHz clock rate.

Writing to the coefficient inputs, CI.9:0, initializes the L64245. The WA.7:0 inputs, connected to the microprocessor address bus, control the address logic for the coefficients and the control word register.

Address bit 0 (Address.0) selects between the high and low bytes written to the L64245. When Address0 selects the high byte, the PAL enables the 74LS373 transparent latch. When Address0 selects the low byte, the PAL asserts WEN (LOW) and the L64245 latches the coefficient data (or the control word) from the Data Bus (CI.7:0) and the 74LS373 (CI.9:8). The microprocessor must make available the high byte first, followed by the low byte, to make both parts of the coefficient available to the L64245 at the same time.

The 74LS373 provides six bits to the PAL to select among the L64245 operating modes stored in the PAL. The PAL then provides the control signals to the L64245.

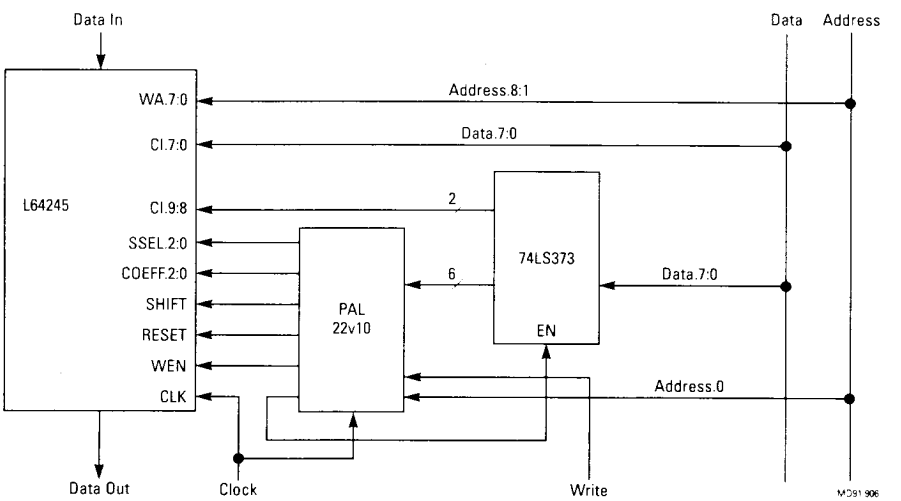


Figure 7. Interfacing an L64245 to an 8-bit Microprocessor

Table 7. Typical Filter Operations – 40 MHz Clock Rate

Filter Type	F_{input} (MHz)	F_{output} (MHz)	No. of Taps	$STATES_{10}$	Equation
Real	40	40	26	0	$y(n) = \sum_{i=0}^{25} h_i x(n-i)$
	20	20	52	1	$y(n) = \sum_{i=0}^{51} h_i x(n-i)$
	10	10	104	2	$y(n) = \sum_{i=0}^{103} h_i x(n-i)$
	5	5	208	3	$y(n) = \sum_{i=0}^{207} h_i x(n-i)$

Application Examples (Continued)

Table 7. Typical Filter Operations – 40 MHz Clock Rate (Continued)

Filter Type	F_{input} (MHz)	F_{output} (MHz)	No. of Taps	$STATES_{10}$	Equation
Decimation (real)	40	20	52	1	$y(n) = \sum_{i=0}^{51} h_i x(2n-i)$
	40	10	104	2	$y(n) = \sum_{i=0}^{103} h_i x(4n-i)$
	20	10	104	2	$y(n) = \sum_{i=0}^{103} h_i x(2n-i)$
	40	5	208	3	$y(n) = \sum_{i=0}^{207} h_i x(8n-i)$
	20	5	208	3	$y(n) = \sum_{i=0}^{207} h_i x(4n-i)$
	10	5	208	3	$y(n) = \sum_{i=0}^{207} h_i x(2n-i)$
Interpolation (real)	20	40	52	0	$y(2n+k) = \sum_{i=0}^{25} h_{i,k} x(n-i)$ k = 0,1
	10	40	104	0	$y(4n+k) = \sum_{i=0}^{25} h_{i,k} x(n-i)$ k = 0,1,2,3
	10	20	104	1	$y(2n+k) = \sum_{i=0}^{51} h_{i,k} x(n-i)$ k = 0,1
	5	40	208	0	$y(8n+k) = \sum_{i=0}^{25} h_{i,k} x(n-i)$ k = 0,....,7
	5	20	208	1	$y(4n+k) = \sum_{i=0}^{51} h_{i,k} x(n-i)$ k = 0,1,2,3
	5	10	208	2	$y(2n+k) = \sum_{i=0}^{103} h_{i,k} x(n-i)$ k = 0,1
Complex	20	20	12	0	$y(n) = \sum_{i=0}^{11} h_i x(n-i)$ y,x,h complex
	20	10	25	1	$y(n) = \sum_{i=0}^{24} h_i x(2n-i)$ y,x,h complex
	10	10	25	1	$y(n) = \sum_{i=0}^{24} h_i x(n-i)$ y,x,h complex
	20	5	50	2	$y(n) = \sum_{i=0}^{49} h_i x(4n-i)$ y,x,h complex
	10	5	51	2	$y(n) = \sum_{i=0}^{50} h_i x(2n-i)$ y,x,h complex
	5	5	51	2	$y(n) = \sum_{i=0}^{50} h_i x(n-i)$ y,x,h complex
k-interleaved filters (real)	40/k	40/k	26	m[1]	$y_k(n) = \sum_{i=0}^{25} h_{i,k} x_k(n-i)$
2D filters (real)	20	20	2 x 26	1	$y(n) = \sum_{k=0}^{1} \sum_{i=0}^{25} h_{i,k} x_k(n-i)$
	10	10	4 x 26	2	$y(n) = \sum_{k=0}^{3} \sum_{i=0}^{25} h_{i,k} x_k(n-i)$
	5	5	8 x 26	3	$y(n) = \sum_{k=0}^{7} \sum_{i=0}^{25} h_{i,k} x_k(n-i)$

Notes:
1. m = 1, 2, 3 for k = 2, 4, 8, respectively.

Application Examples (Continued)

When the filter coefficients contain periodic zeros, the computation rate of the device may be increased. For example, consider a filter with zero values for all even-numbered coefficients (except for the center value), where the filter is processing a 5 MHz data stream. In this case, three of the eight computation cycles (those in which all active coefficients are zero) can be skipped. Not performing computations based on these zero coefficients allows the output data rate to increase from 5 MHz to 8 MHz. Similarly, a 10 MHz output rate could increase to 13.3 MHz, because one cycle of every four is not needed. Note that the filter processor can also implement decimating interleaved real filters. However, it only processes each signal in groups of D input samples, where D is the decimation ratio.

When operating as a 2-D filter, the filter processor is configured as a decimator and the data in the secondary dimension are interleaved before processing. For example, in a video application, up to eight lines of data output from the video-line delays could be interleaved and filtered.

Tables 8, 11 and 12 specify the sequencing of the SSEL, COEFF, SHIFT and RESET signals for a variety of filter types.

Table 8. Real Non-Interleaved Filters

F_{in}/F_{out}	Sequence Period	SSEL Sequence	COEFF Sequence	SHIFT Sequence	RESET Sequence	N
40/40	1	0, ...	0, ...	1, ...	1, ...	1
20/20	2	0,1, ...	0,1, ...	0,1, ...	0,1, ...	2
10/10	4	0,1,2,3, ...	0,1,2,3, ...	0,0,0,1, ...	0,0,0,1, ...	4
5/5	8	0,1,2,3,4,5,6,7, ...	0,1,2,3,4,5,6,7, ...	0,0,0,0,0,0,0,1, ...	0,0,0,0,0,0,0,1, ...	8
40/20	2	1,1, ...	1,0, ...	1,1, ...	0,1, ...	2
40/10	4	3,3,3,3, ...	3,2,1,0, ...	1,1,1,1, ...	0,0,0,1, ...	4
40/5	8	7,7,7,7,7,7,7,7, ...	7,6,5,4,3,2,1,0, ...	1,1,1,1,1,1,1,1, ...	0,0,0,0,0,0,0,1, ...	8
20/10	4	1,3,1,3, ...	1,3,0,2, ...	0,1,0,1, ...	0,0,0,1, ...	4
20/5	8	3,7,3,7,3,7,3,7, ...	3,7,2,6,1,5,0,4, ...	0,1,0,1,0,1,0,1, ...	0,0,0,0,0,0,0,1, ...	8
10/5	8	1,3,5,7,1,3,5,7, ...	1,3,5,7,0,2,4,6, ...	0,0,0,1,0,0,0,1, ...	0,0,0,0,0,0,0,1, ...	8
20/40	2	0,0, ...	0,1, ...	0,1, ...	1,1, ...	1
10/40	4	0,0,0,0, ...	0,1,2,3, ...	0,0,0,1, ...	1,1,1,1, ...	1
5/40	8	0,0,0,0,0,0,0,0, ...	0,1,2,3,4,5,6,7, ...	0,0,0,0,0,0,0,1, ...	1,1,1,1,1,1,1,1, ...	1
10/20	4	0,1,0,1, ...	0,1,2,3, ...	0,0,0,1, ...	0,1,0,1, ...	2
5/20	8	0,1,0,1,0,1,0,1, ...	0,1,2,3,4,5,6,7, ...	0,0,0,0,0,0,0,1, ...	0,1,0,1,0,1,0,1, ...	2
5/10	8	0,1,2,3,0,1,2,3, ...	0,1,2,3,4,5,6,7, ...	0,0,0,0,0,0,0,1, ...	0,0,0,1,0,0,0,1, ...	4

The ordering of the coefficients shown under COEFF Sequence in Table 8 illustrates the case where the coefficients are loaded and stored in sequential order, and read out according to the specified COEFF Sequence. The coefficients can also be loaded and stored in the order specified by the COEFF Sequence, and then read out sequentially. Tables 9 and 10 illustrate the difference in the order of coefficient storage for these two approaches, using the 20/10 F_{in}/F_{out} filter example from Table 8.

For each of the filters in Table 8, each interleaved stream is processed with a 26-tap filter. The filter coefficients for the kth stream are stored in the kth coefficient latch of each tap.

Table 9. Coefficients Stored in Sequential Order (Read Out in COEFF Sequence Order 1,3,0,2)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	h_0	h_4	h_8	h_{12}	h_{16}	...	h_{96}	h_{100}
1	h_1	h_5	h_9	h_{13}	h_{17}	...	h_{97}	h_{101}
2	h_2	h_6	h_{10}	h_{14}	h_{18}	...	h_{98}	h_{102}
3	h_3	h_7	h_{11}	h_{15}	h_{19}	...	h_{99}	h_{103}

Application Examples (Continued)

Table 10. Coefficients Stored in COEFF Sequence Order 1,3,0,2 (Read Out Sequentially)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	h_1	h_5	h_9	h_{13}	h_{17}	...	h_{97}	h_{101}
1	h_3	h_7	h_{11}	h_{15}	h_{19}	...	h_{99}	h_{103}
2	h_0	h_4	h_8	h_{12}	h_{16}	...	h_{96}	h_{100}
3	h_2	h_6	h_{10}	h_{14}	h_{18}	...	h_{98}	h_{102}

For the complex filters, the input and output data are interleaved, with the real parts followed by the imaginary parts. For each sequence in Table 8, the real and imaginary parts are input during the first and second cycles that SHIFT is HIGH, respectively. The filter coefficients, $h_n = h_{r,n} + jh_{i,n}$, are loaded as shown in Tables 13 through 18.

Table 11. Real Interleaved Filters

F_{in} /F_{out}	Sequence Period	SSEL Sequence	COEFF Sequence	SHIFT Sequence	RESET Sequence	N
20/20	2	1,1, ...	0,1, ...	1,1, ...	1,1, ...	1
10/10	4	3,3,3,3, ...	0,1,2,3, ...	1,1,1,1, ...	1,1,1,1, ...	1
5/5	8	7,7,7,7,7,7,7,7 ...	0,1,2,3,4,5,6,7 ...	1,1,1,1,1,1,1,1, ...	1,1,1,1,1,1,1,1, ...	1

Table 12. Complex Non-Interleaved Filters

F_{in} /F_{out}	Sequence Period	SSEL Sequence	COEFF Sequence	SHIFT Sequence	RESET Sequence	N
20/20	2	0,0, ...	0,1, ...	1,1, ...	1,1, ...	1
20/10	4	1,1,1,1, ...	0,1,2,3, ...	1,1,1,1, ...	0,1,0,1, ...	2
10/10	4	0,1,0,1, ...	0,1,2,3, ...	0,1,0,1, ...	0,1,0,1, ...	2
20/5	8	3,3,3,3,3,3,3,3, ...	0,1,2,3,4,5,6,7, ...	1,1,1,1,1,1,1,1, ...	0,0,0,1,0,0,0,1, ...	4
10/5	8	1,3,1,3,1,3,1,3, ...	0,1,2,3,4,5,6,7, ...	0,1,0,1,0,1,0,1, ...	0,0,0,1,0,0,0,1, ...	4
5/5	8	0,1,2,3,0,1,2,3, ...	0,1,2,3,4,5,6,7, ...	0,0,0,1,0,0,0,1, ...	0,0,0,1,0,0,0,1, ...	4

Table 13. Complex Non-Interleaved Filter Coefficient Storage (20/20, 12 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$-h_{i,0}$	$h_{r,0}$	$-h_{i,1}$	$h_{r,1}$	$-h_{i,2}$	...	0	0
1	0	$h_{r,0}$	$h_{i,0}$	$h_{r,1}$	$-h_{i,1}$	...	$-h_{i,11}$	0

Table 14. Complex Non-Interleaved Filter Coefficient Storage (20/10, 25 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$h_{r,0}$	$h_{r,1}$	$h_{r,2}$	$h_{r,3}$	$h_{r,4}$	...	$h_{r,24}$	0
1	$-h_{i,0}$	$-h_{i,1}$	$-h_{i,2}$	$-h_{i,3}$	$-h_{i,4}$	...	$-h_{i,24}$	0
2	0	$h_{i,0}$	$h_{i,1}$	$h_{i,2}$	$h_{i,3}$	...	$h_{i,23}$	$h_{i,24}$
3	0	$h_{r,0}$	$h_{r,1}$	$h_{r,2}$	$h_{r,3}$	...	$h_{r,23}$	$h_{r,24}$

Application Examples
(Continued)

Table 15. Complex Non-Interleaved Filter Coefficient Storage (10/10, 25 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$-h_{i,0}$	$-h_{i,1}$	$-h_{i,2}$	$-h_{i,3}$	$-h_{i,4}$	...	$-h_{i,24}$	0
1	$h_{r,0}$	$h_{r,1}$	$h_{r,2}$	$h_{r,3}$	$h_{r,4}$	...	$h_{r,24}$	0
2	0	$h_{i,0}$	$h_{i,1}$	$h_{i,2}$	$h_{i,3}$	...	$h_{i,23}$	$h_{i,24}$
3	$h_{r,0}$	$h_{r,1}$	$h_{r,2}$	$h_{r,3}$	$h_{r,4}$	...	$h_{r,24}$	0

Table 16. Complex Non-Interleaved Filter Coefficient Storage (20/5, 50 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	$h_{r,9}$	...	$h_{r,49}$	0
1	$-h_{i,1}$	$-h_{i,3}$	$-h_{i,5}$	$-h_{i,7}$	$-h_{i,9}$	...	$-h_{i,49}$	0
2	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$h_{r,6}$	$h_{r,8}$	...	$h_{r,48}$	0
3	$-h_{i,0}$	$-h_{i,2}$	$-h_{i,4}$	$-h_{i,6}$	$-h_{i,8}$	...	$-h_{i,48}$	0
4	0	$h_{i,1}$	$h_{i,3}$	$h_{i,5}$	$h_{i,7}$	...	$h_{i,47}$	$h_{i,49}$
5	0	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	...	$h_{r,47}$	$h_{r,49}$
6	0	$h_{i,0}$	$h_{i,2}$	$h_{i,4}$	$h_{i,6}$	...	$h_{i,46}$	$h_{i,48}$
7	0	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$h_{r,6}$	...	$h_{r,46}$	$h_{r,48}$

Table 17. Complex Non-Interleaved Filter Coefficient Storage (10/5, 51 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$-h_{r,6}$	$h_{r,8}$	...	$h_{r,48}$	$h_{r,50}$
1	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	$h_{r,9}$	...	$h_{r,49}$	0
2	$-h_{i,0}$	$-h_{i,2}$	$-h_{i,4}$	$-h_{i,6}$	$-h_{i,8}$	...	$-h_{i,48}$	$-h_{i,50}$
3	$-h_{i,1}$	$-h_{i,3}$	$-h_{i,5}$	$-h_{i,7}$	$-h_{i,9}$	...	$-h_{i,49}$	0
4	0	$h_{i,1}$	$h_{i,3}$	$h_{i,5}$	$h_{i,7}$	...	$h_{i,47}$	$h_{i,49}$
5	$h_{i,0}$	$h_{i,2}$	$h_{i,4}$	$h_{i,6}$	$h_{i,8}$	...	$h_{i,48}$	$h_{i,50}$
6	0	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	...	$h_{r,47}$	$h_{r,49}$
7	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$h_{r,6}$	$h_{r,8}$	...	$h_{r,48}$	$h_{r,50}$

Table 18. Complex Non-Interleaved Filter Coefficient Storage (5/5, 51 Taps)

Coefficient	Tap 0	1	2	3	4	...	24	25
0	$-h_{i,0}$	$-h_{i,2}$	$-h_{i,4}$	$-h_{i,6}$	$-h_{i,8}$	...	$-h_{i,48}$	$-h_{i,50}$
1	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$h_{r,6}$	$h_{r,8}$	...	$h_{r,48}$	$h_{r,50}$
2	$-h_{i,1}$	$-h_{i,3}$	$-h_{i,5}$	$-h_{i,7}$	$-h_{i,9}$	...	$-h_{i,49}$	0
3	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	$h_{r,9}$	...	$h_{r,49}$	0
4	0	$h_{i,1}$	$h_{i,3}$	$h_{i,5}$	$h_{i,7}$	...	$h_{i,47}$	$h_{i,49}$
5	$h_{r,0}$	$h_{r,2}$	$h_{r,4}$	$h_{r,6}$	$h_{r,8}$	...	$h_{r,48}$	$h_{r,50}$
6	$h_{i,0}$	$h_{i,2}$	$h_{i,4}$	$h_{i,6}$	$h_{i,8}$	...	$h_{i,48}$	$h_{i,50}$
7	$h_{r,1}$	$h_{r,3}$	$h_{r,5}$	$h_{r,7}$	$h_{r,9}$	...	$h_{r,49}$	0

Advanced Application Examples

The previous section of this datasheet provides examples where the number of states accessed by each multiplier is a power of two, that is 1, 2, 4 or 8. The L64245 can also be used in applications where the number of states accessed is not a power of two, that is 3, 5, 6 or 7. In these cases, the SSEL sequencing is more complex than it would be if the user simply increased the number of states to the next power of two, but the device can operate at a higher data rate. Table 19 summarizes the filter operations for several of these more complicated filters.

Table 20 shows the sequencing for the SSEL, COEFF, SHIFT and RESET signals for these filters. Note that the SSEL sequences listed in the table are not used directly as inputs to the L64245; instead, they must be converted to a more complex sequence first, and then input to the device. Note also that the periods for these sequences are larger than expected. An explanation of how to convert the SSEL* sequences to actual device inputs follows the table.

Table 19. Advanced Filter Types

Filter Type	F_{input} (MHz)	F_{output} (MHz)	No. of Taps	STATES	Equation
Real	13.3	13.3	78	2	$y(n) = \sum_{i=0}^{77} h_i x(n-i)$
	8	8	130	3	$y(n) = \sum_{i=0}^{129} h_i x(n-i)$
	6.7	6.7	156	3	$y(n) = \sum_{i=0}^{155} h_i x(n-i)$
	5.7	5.7	182	3	$y(n) = \sum_{i=0}^{181} h_i x(n-i)$
Decimation (Real)	40	13.3	78	2	$y(n) = \sum_{i=0}^{77} h_i x(3n-i)$
	40	8	130	3	$y(n) = \sum_{i=0}^{129} h_i x(5n-i)$
	40	6.7	156	3	$y(n) = \sum_{i=0}^{155} h_i x(6n-i)$
	40	5.7	182	3	$y(n) = \sum_{i=0}^{181} h_i x(7n-i)$
	13.3	6.7	156	3	$y(n) = \sum_{i=0}^{155} h_i x(2n-i)$

Table 20. Advanced Real Non-Interleaved Filters

F_{in}/F_{out}	Sequence Period	SSEL* Sequence	COEFF Sequence	SHIFT Sequence	RESET Sequence	N	M
13.3/13.3	36	0,1,2 ...	0,1,2 ...	0,0,1 ...	0,0,1 ...	4	3
8/8	200	0,1,2,3,4, ...	0,1,2,3,4, ...	0,0,0,0,1, ...	0,0,0,0,1, ...	8	5
6.7/6.7	144	0,1,2,3,4,5, ...	0,1,2,3,4,5, ...	0,0,0,0,0,1, ...	0,0,0,0,0,1, ...	8	6
5.7/5.7	392	0,1,2,3,4,5,6, ...	0,1,2,3,4,5,6, ...	0,0,0,0,0,0,1, ...	0,0,0,0,0,0,1, ...	8	7
40/13.3	12	2,2,2, ...	2,1,0, ...	1,1,1, ...	0,0,1, ...	4	3
40/8	40	4,4,4,4,4, ...	4,3,2,1,0, ...	1,1,1,1,1, ...	0,0,0,0,1, ...	8	5
40/6.7	24	5,5,5,5,5,5, ...	5,4,3,2,1,0, ...	1,1,1,1,1,1, ...	0,0,0,0,0,1, ...	8	6
40/5.7	56	6,6,6,6,6,6,6, ...	6,5,4,3,2,1,0, ...	1,1,1,1,1,1,1, ...	0,0,0,0,0,0,1, ...	8	7
13.3/6.7	72	1,3,5,1,3,5, ...	1,3,5,0,2,4, ...	0,0,1,0,0,1, ...	0,0,0,0,0,1, ...	8	6

Advanced Application Examples
(Continued)

The actual SSEL input sequence for an application can be computed from the associated SSEL*(i) sequence and two other sequences, COUNT*(i) and COUNT(i), according to these equations:

SSEL(i) = (SSEL*(i) - COUNT*(i) + COUNT(i)) mod N if (SSEL*(i) - COUNT*(i) ≥ 0)
otherwise
SSEL(i) = (SSEL*(i) - COUNT*(i) + COUNT(i) + M) mod N

where COUNT(i) increments modulo N each time that SHIFT is HIGH, and COUNT*(i) increments modulo M when SHIFT is HIGH.

The sequence period is the least common multiple (LCM) of S x M and S x N, that is:

sequence period = S x LCM(N, M)

where S is the period of the SHIFT sequence.

As an example consider the 13.3 MHz, 78-tap filter characterized in Tables 19 and 20. In this case:

SSEL*(i) = 0,1,2, ...

COUNT*(i) = 0,0,0,1,1,1,2,2,2, ...

COUNT(i) = 0,0,0,1,1,1,2,2,2,3,3,3, ...

SSEL(i) = 0,1,2,3,1,2,3,0,2,3,0,1,2,0,1,2,3,1,2,3,0, 1,3,0,1,2,0,1,2,3,0,2,3,0,1,3, ...

Note that the sequence period for this example is:

3 x LCM(3,4) = 36

As a second example, consider the 130-tap, 40 MHz to 8 MHz decimator listed in Tables 19 and 20. For this case:

SSEL*(i) = 4, ...

COUNT*(i) = 0,1,2,3,4, ...

COUNT(i) = 0,1,2,3,4,5,6,7, ...

SSEL(i) = 4,4,4,4,4,1,1,1,1,1,6,6,6,6,6,3,3,3,3,3,0, 0,0,0,0,5,5,5,5,5,2,2,2,2,2,7,7,7,7,7, ...

The sequence period in this case is:

1 x LCM(5,8) = 40

The L64245 can implement many other filter variations in a similar fashion. For example, both interleaved filters with three, five, six or seven interleaved streams and 2-D (3 x n, 5 x n, 6 x n or 7 x n) filters have SSEL sequences that are the same as those of corresponding decimation filters. In general, whenever the number of taps accessed by each multiplier is not a power of two, set STATES.1:0 to allow access to a number of state registers given by the next larger power of two. Then the required SSEL sequence can be determined as described above.

Functional Waveforms

The following information, extracted from Table 8, summarizes the control signal information for a 20 MHz to 10 MHz decimation filter with a 40 MHz clock.

Table 21. Control Signals for a 20 MHz to 10 MHz Decimator

F_{in}/F_{out}	Sequence Period	SSEL Sequence	COEFF Sequence	SHIFT Sequence	RESET Sequence	N
20/10	4	1,3,1,3, ...	1,3,0,2, ...	0,1,0,1, ...	0,0,0,1, ...	4

Figure 8 shows the detailed waveforms for this filter. For a 10-MHz output rate, the processor can perform four filter taps per multiplier, resulting in a maximum filter length of 104 taps. The input data, DI.9:0, are sampled on every other cycle, when SHIFT is HIGH. When SHIFT is LOW, the data on DI.9:0 are ignored. To obtain a regular sequence on the COEFF bus, the coefficients have been stored in the order specified by the COEFF Sequence (1, 3, 0, 2), as discussed previously. In this case, as with the example of Table 8, coefficients h(4n+1), h(4n+3), h(4n) and h(4n+2) are stored in the coefficients registers with addresses 0, 1, 2 and 3 for each tap, respectively. The states are selected in a somewhat irregular order because the data are shifted in the middle of the computation.

The example of Figure 8 assumes that the data on DI.9:0 were always zero before x(0) was input. The first non-zero output, y(1), arrives N + 6 = 10 cycles after x(1) is input.

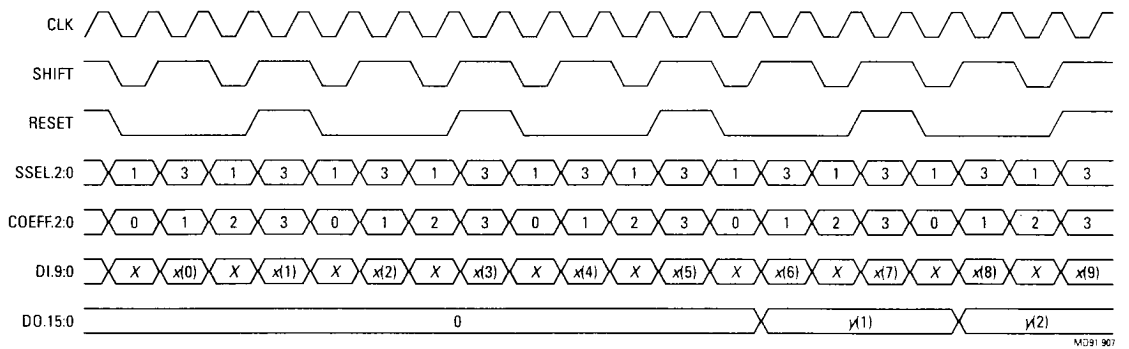


Figure 8. Waveforms for a 20 MHz to 10 MHz Decimator

AC Timing

Figures 9 and 10 illustrate and the table that follows summarizes the L64245 AC timing both during normal operation and during coefficient and control word update.

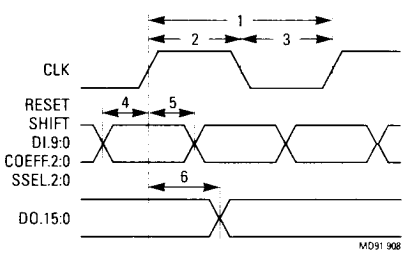


Figure 9. Normal Operation Timing

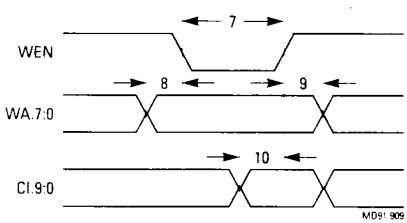


Figure 10. Coefficient and Control Word Update Timing

AC Switching Characteristics: Commercial (TA = °C to 70°C, VDD = 4.75 V to 5.25 V)

Parameter	Symbol	Description	L64245-40[1]		L64245-30[1]		L64245-20[1]	
			Min	Max	Min	Max	Min	Max
1	tCYCLE	CLK cycle time	25		33		50	
2	tPWH	Min CLK pulse width, HIGH	10		15		20	
3	tPWL	Min CLK pulse width, LOW	12		15		20	
4	tS	Input setup time to CLK	7		10		13	
5	tH	Input hold time to CLK	0		1		2	
6	tOD	DO Output Delay from CLK[2]		18		24		30
7	tWEPWL	WEN Pulse Width, LOW	10		15		18	
8	tRS	Setup time to WEN	7		8		10	
9	tRH	Hold time to WEN	7		9		11	
10	tCS	Setup time to WEN	10		12		15	

Notes:
1. All input times are in ns.
2. Output loading = 50 pF.

Operating Characteristics

Absolute Maximum Ratings (referenced to GND)

Parameter	Symbol	Limits	Units
DC supply voltage Input voltage	VDD VIN	-0.3 to +7 -0.3 to VDD + 0.3	V V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range (commercial)	TA	0 to +70	°C

DC Characteristics: Temperature Range 0°C to +70°C, ± 5% Power Supply

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low-level input voltage (commercial)				0.8	V
VIH	High-level input voltage (commercial)		2.0			V
IIN	Input current	VIN = VDD	-370		400	µA
VOH	High-level output voltage (commercial)	IOH = -4 ma	2.4	4.5		V
VOL	Low-level output voltage (commercial)	IOL = 4 ma		0.2	0.4	V
IOS	Output short circuit current[1]	VDD = Max, VO = VDD	30	75	140	mA
		VDD = Max, VO = 0 V	-25	-70	-140	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current[2]	tCYCLE = 25 ns		400		mA
CIN	Input capacitance	Any input		2.5		pF
COUT	Output capacitance	Any output		2.0		pF

Notes:
1. Do not short more than one output at one time. Duration of the short circuit test must not exceed one second.
2. For 40 MHz device.

Pinout, Package and Ordering Information

The L64245 is available in both a 68-pin ceramic and 68-pin plastic pin grid array (CPGA and PPGA) packages. This section contains the package pinouts, organized both by signal name and pin number, as well as the package mechanical drawings and ordering information for the L64245.

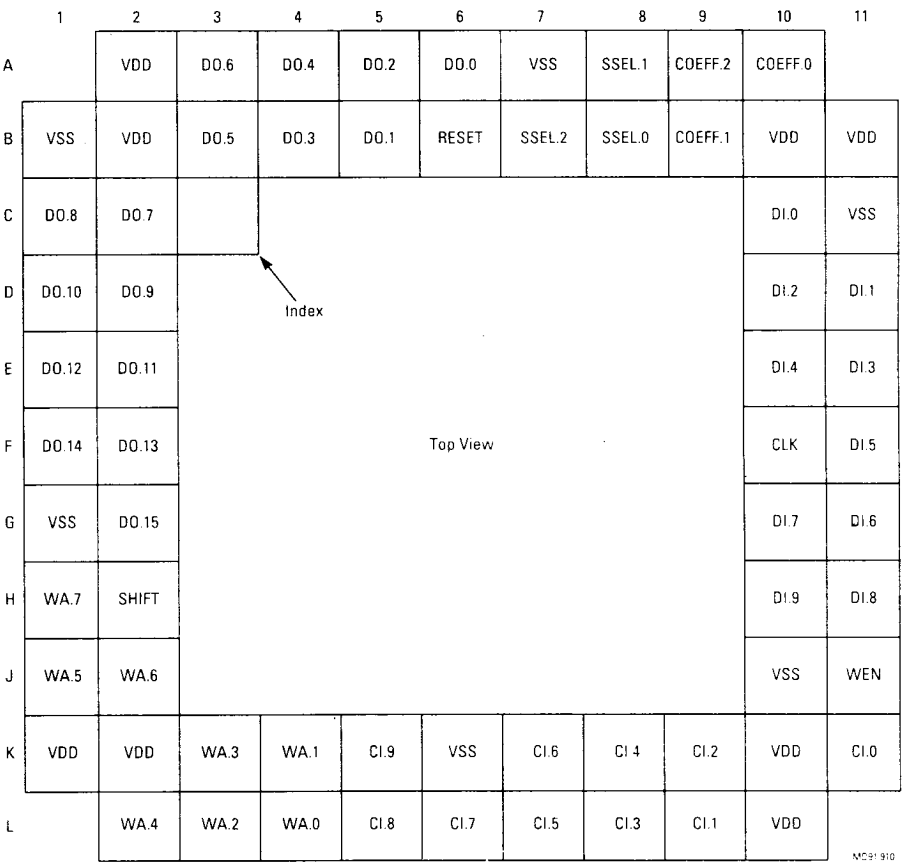
L64245 Package Pin Information (68-Pin CPGA and PPGA, by Signal Name)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
CI.0	K11	DI.3	E11	DO.4	A4	VDD	K2
CI.1	L9	DI.4	E10	DO.5	B3	VDD	L10
CI.2	K9	DI.5	F11	DO.6	A3	VSS	A7
CI.3	L8	DI.6	G11	DO.7	C2	VSS	B1
CI.4	K8	DI.7	G10	DO.8	C1	VSS	C11
CI.5	L7	DI.8	H11	DO.9	D2	VSS	G1
CI.6	K7	DI.9	H10	RESET	B6	VSS	J10
CI.7	L6	DO.0	A6	SHIFT	H2	VSS	K6
CI.8	L5	DO.1	B5	SSEL.0	B8	WA.0	L4
CI.9	K5	DO.10	D1	SSEL.1	A8	WA.1	K4
CLK	F10	DO.11	E2	SSEL.2	B7	WA.2	L3
COEFF.0	A10	DO.12	E1	VDD	A2	WA.3	K3
COEFF.1	B9	DO.13	F2	VDD	B10	WA.4	L2
COEFF.2	A9	DO.14	F1	VDD	B11	WA.5	J1
DI.0	C10	DO.15	G2	VDD	B2	WA.6	J2
DI.1	D11	DO.2	A5	VDD	K1	WA.7	H1
DI.2	D10	DO.3	B4	VDD	K10	WEN	J11

L64245 Package Pin Information (68-Pin CPGA and PPGA, by Pin Number)

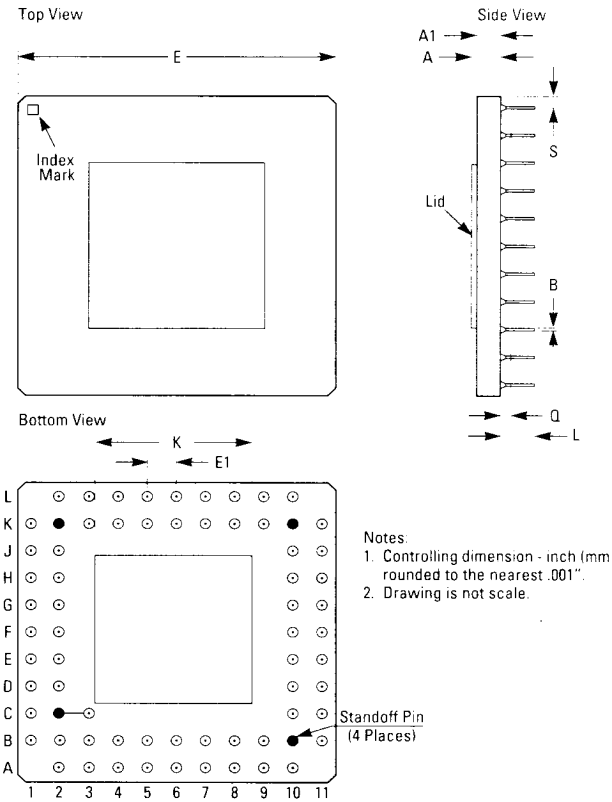
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VDD	B9	COEFF.1	F10	CLK	K4	WA.1
A3	DO.6	B10	VDD	F11	DI.5	K5	CI.9
A4	DO.4	B11	VDD	G1	VSS	K6	VSS
A5	DO.2	C1	DO.8	G2	DO.15	K7	CI.6
A6	DO.0	C2	DO>7	G10	DI.7	K8	CI.4
A7	VSS	C10	DI.0	G11	DI.6	K9	CI.2
A8	SSEL.1	C11	VSS	H1	WA.7	K10	VDD
A9	COEFF.2	D1	DO.10	H2	SHIFT	K11	CI.0
A10	COEFF.0	D2	DO.9	H10	DI.9	L2	WA.4
B1	VSS	D10	DI.2	H11	DI.8	L3	WA.2
B2	VSS	D11	DI.1	J1	WA.5	L4	WA.0
B3	DO.5	E1	DO.12	J2	WA.6	L5	CI.8
B4	DO.3	E2	DO.11	J10	VSS	L6	CI.7
B5	DO.1	E10	DI.4	J11	WEN	L7	CI.5
B6	RESET	E11	DI.3	K1	VDD	L8	CI.3
B7	SSEL.2	F1	DO.14	K2	VDD	L9	CI.1
B8	SSEL.0	F2	DO.13	K3	WA.3	L10	VDD

Pinout, Package and Ordering Information
(Continued)



68-Pin CPGA and PPGA Pin Diagram

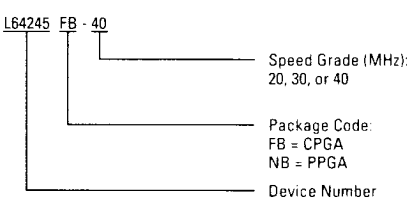
Pinout, Package and Ordering Information (Continued)



Notes:
1. Controlling dimension - inch (mm), rounded to the nearest .001".
2. Drawing is not scale.

Dimension		Inches (mm) PPGA	CPGA
A	Max	0.139 (3.531)	0.117 (2.972)
A1	Ref	0.089 (2.261)	0.080 (2.032)
B	Min	0.016 (0.406	0.016 (0.406)
	Max	0.020 (0.508)	0.020 (0.508)
E	Min	1.137 Sq (28.88)	1.086 Sq (27.58)
	Max	1.157 Sq (29.39)	1.122 Sq (28.50)
E1	Min	0.088 (2.235)	0.095 (2.413)
	Max	0.112 (2.845)	0.105 (2.667)
K	Ref	0.650 Sq (16.51)	0.673 Sq (17.09)
L	Min	0.187 (4.750)	0.175 (4.445)
	Max	0.207 (5.258)	0.185 (4.699)
Q	Ref	0.070 (1.803)	0.050 (1.270)
S	Ref	0.050 (1.270)	0.050 (1.270)

68-Pin CPGA and PPGA Mechanical Drawing



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