microelectronics group

Lucent Technologies
Bell Labs Innovations

DNCM00
10 Mbit/s Ethernet MAC ASIC Macrocell

Features

- 10 Mbit/s Ethernet MAC designed to operate with industry-standard physical layer transceivers

- Operation in half- or full-duplex environment

- Asynchronous reset with no clocks present

- Interconnection with physical layers that do not produce a continuous RXC

- Receiver handles seven dribble bits

- Easy simulation in *Verilog*[*] or *Synopsys*[†] synthesis

- Compatibility with full internal scan test methodology

Description

The DNCM00 is an 802.3 compliant MAC that is designed to interface to industry-standard physical layer transceivers.

The DNCM00 operates in a half- or full-duplex environment. In half duplex, the receiver is not activated if TXE is active to avoid buffering one's own transmitted packet. In full-duplex mode, the COL input from the physical layer is ignored, and the DNCM00 can transmit and receive data simultaneously.

All transmit and receive functions can be asynchronously reset with no clocks present. For interconnection with physical layers that do not produce a continuous RXC, the DNCM00 receiver completes a packet reception with as few as three RX clocks after CRS falls. The receiver will also correctly handle up to seven dribble bits.

The DNCM00 is described in fully synthesizable behavioral *Verilog* with 2-state table format state machines for easy simulation in *Verilog* or *Synopsys* synthesis.

The DNCM00 has been designed to be used with a full internal scan test methodology. There are test inputs for controllability of all RESET signals, and the DNCM00 can be synthesized in the Lucent Technologies libraries with flip-flop types that guarantee scan equivalent types if scan is inserted. The DNCM00 is approximately 10K grids in size without scan, and approximately 12K grids in size with scan.

All control inputs to the DNCM00 are assumed to be stable levels that remain valid for the duration of a transmitted or received packet. They are not registered or resynchronized to a clock in the DNCM00.

[*] *Verilog* is a registered trademark of Cadence Design Systems, Inc.
[†] *Synopsys* is a registered trademark of Synopsys, Inc.

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

Signal Information

Table 1. Input Terminal Descriptions

Input Terminal	Description
TXC	**Transmit Clock.** 10 MHz, 50% duty cycle, continuously running. TXC clocks all transmitter and timer logic.
RST	**Reset (Active-High).** Assumed to be asynchronous. Used to reset state machines and critical logic in the transmitter, and state machines in the receiver.
COL	**Collision Detect (Active-High).** Used to indicate a collision between two stations. Assumed to be active a minimum of two TXC cycles. COL is only sampled when appropriate, during half-duplex transmit operations when TXE is active, and during the first 6.4 μs of intergap time after any (normal or aborted) transmission if ISQE is active.
MFDUP	**MAC Full Duplex (Active-High).** Used to control half- or full-duplex operation. When MFDUP is low, the COL input is monitored and the binary backoff algorithm is employed if collisions occur during transmission. When MFDUP is low if CRS activates while the MAC's own packet is being transmitted, the receiver is not enabled since the received packet is the MAC's own transmitted packet. When MFDUP is high, the COL input is ignored during packet transmission and monitored during intergap delay for the presence of SQE if the ISQE signal is not active. When MFDUP is high, all packets are received regardless of the status of TXE.

RETRY_1_, RETRY_0_	**Retry.** Used to control the total number of attempts (initial + retries after collision) the MAC will make to transmit a packet. The total attempts follow the below table:
	
	RETRY_1_ RETRY_0_ ATTEMPTS
	   0 0 16
	   0 1 8
	   1 0 4
	   1 1 1

BSEL	**Backoff Select (Active-High).** Used to control whether the binary backoff algorithm is used during collision handling. If BSEL is high, the backoff algorithm is not used. The transmitter will jam for 32 TXC cycles and attempt to retransmit after 9.6 μs of intergap time. If low, the transmitter follows the normal binary backoff algorithm following a collision.

PREAM_1_, PREAM_0_	**Preamble Control.** Used to control the length of the preamble sequence preceding packet transmission. The total bit count in the preamble (10101010... + 10101011) follows the below table:
	
	PREAM_1_ PREAM_0_ Length
	   0 0 64 bits
	   0 1 56 bits
	   1 0 48 bits
	   1 1 40 bits

ISQE	**Ignore SQE (Active-High).** Used to ignore the SQE signal from the physical layer transceiver during the first 6.4 μs of interframe gap. If high, the SQE error flag will not set.
DEFER	**Abort After Max Deferral (Active-High).** Used to force the transmitter to abort a transmission attempt if it has deferred for more than 24,288 TXC cycles. Deferring starts when the transmitter is ready to transmit but is prevented from doing so because CRS is active. Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits and collides, backs off, and then has to defer again after completion of backoff, the deferral timer resets to 0 and restarts. If DEFER is low, the transmitter will defer indefinitely.
TXREQ	**Transmit Request (Active-High).** Used to request a packet transmission. TXREQ is a handshake signal; it should be held high until TXACK is activated by the transmitter. TXREQ should then not be reactivated until TXEOP is returned by the transmitter.

Signal Information (continued)

Table 1. Input Terminal Descriptions (continued)

Input Terminal	Description
TXEOD	**Transmit End of Data (Active-High).** Used to end a transmit operation normally. TXEOD should activate one clock after the DMA receives a TXLD from the transmitter. The transmitter will load and transmit that byte, and then transmit (inverted) CRC data according to the status of APND-CRC and INVCRC.
ABORT	**Abort Transmit (Active-High).** Used to stop a transmission ungracefully. The transmitter will immediately terminate a transmission if this input is set. Abort should be held high for two or more TXC cycles. When a packet is aborted during preamble, the preamble is completed and the APNDCRC and INVCRC inputs are followed. If ABORT is activated during transmission, transmission immediately stops, and the APNDCRC and INVCRC inputs are followed.
APNDCRC	**Append CRC (Active-High).** Used to control if a 32-bit CRC polynomial is appended to the end of a transmitted packet. If high, the CRC is appended.
INVCRC	**Invert CRC (Active-High).** Used to invert the polarity of the 32-bit CRC polynomial. The normal CRC is inverted prior to transmission. If INVCRC is high, the normal CRC will be reinverted prior to sending, forcing a CRC error.
TSTMODE	**Test Mode (Active-High).** Used to modify the terminal count of transmit counters to speed up testing. When TSTMODE is high, the counters are modified as follows: Counter Normal Count Modified Count 9.6 µs intergap 96 25 51.2 µs timer 512 8 DEFER timer 24288 242
TXDB_[7:0]_	**Transmit Data Byte.** Transmit data. TXDB is loaded into the transmit shift register in the falling edge of the TXLD input and is transmitted LSB first onto the medium.
RXC	**Receive Clock.** 10 MHz receive clock recovered from the receive data stream. RXC is assumed not to be present when the medium is inactive. It is assumed that RXC will be delayed by up to 5 data bit times after CRS activates. RXC must be generated for 5 bit times after CRS goes low to guarantee proper receiver operation. If RXC is delayed after CRS activates, it will cause inaccuracies in some of the RX statistics (SHORT).
RXD	**Receive Data.** RXD is strobed on the rising edge of RXC when CRS is active to assemble receive data bytes.

Signal Information (continued)

Table 2. Output Terminal Descriptions

Output Terminal	Description
TXACK	**Transmit Acknowledge (Active-High) (posedge TXC).** Used in conjunction with TXREQ as a handshake. When TXACK goes high in response to TXREQ, TXREQ can be deactivated.
TXINPROG	**Transmit in Progress (Active-High) (posedge TXC).** Set high if the MAC is currently transmitting preamble, data, or CRC. It is not active if jamming or during collision backoff.
TXD	**Transmit Data (posedge TXC).** Serial transmit data out.
TXLD	**Transmit Load (Active-High) (posedge TXC).** Used to tell the DMAC that the transmitter requires a byte of data for transmission. TXDB_[7:0]_ will be strobed into the transmit shift register on the falling edge of TXLD.
TXEOP	**Transmit End of Operation (Active-High) (posedge TXC).** Used to indicate the end of a transmit operation. The operation may end because of successful transmission, excessive collisions, excess deferral, or an ABORT command. TXEOP is active for one TXC cycle. Transmit statistics, except for SQE, can be monitored after TXEOP activates. SQE should be latched on the falling edge of TXSOP of the following frame.
LATE	**Late Collision (Active-High) (posedge TXC).** Indicates that a collision occurred more than 512 bit times from the start of a transmission. The start of transmission is defined as the transmission of the first bit of preamble.
EXDEF	**Excess Deferral (Active-High) (posedge TXC).** Indicates transmission ended because of waiting for more than 24,288 bit times for the medium to become unbusy.
DEF	**Deferred (Active-High) (posedge TXC).** Indicates that a transmission deferred for 1 to 24,288 bit times during transmission.
COLDET	**Collision Detected (Active-High) (posedge TXC).** Indicates that a collision has been detected. This signal is active from the time a collision was detected until the completion of the 32-bit jam sequence. The COL signal is monitored only when the transmitter is actively transmitting data.
SCOL	**Single Collision (Active-High) (posedge TXC).** Indicates that there was one collision during transmission of the previous packet.
MCOL	**Multiple Collisions (Active-High) (posedge TXC).** Indicates that there was more than one collision during transmission of the previous packet.
CERR	**Collision Error (Active-High) (posedge TXC).** Indicates that the previous transmission was stopped because of excessive collisions as allowed by the RETRY_[1:0]_ inputs. SCOL or MCOL are also valid if CERR is active.
LCRS	**Loss of CRS (Active-High) (posedge TXC).** Indicates that the CRS input was inactive for one or more bit times while the transmitter was active.
SQE	**Signal Quality Error (Active-High) (posedge TXC).** Indicates that a COL signal was not detected during the first 6.4 μs of interframe gap following a transmit attempt. SQE is inactive if the ISQE input is high.
TXBYTE	**Byte Transmitted (Active-High) (posedge TXC).** Indicates that a complete byte of data or CRC has been transmitted. TXBYTE is valid for 1 TXC bit time immediately after the last bit of a byte was transmitted.
TXSOP	**Transmit Start of Packet (Active-High) (posedge TXC).** Active for 1 bit time at the start of preamble.
TXE	**Transmit Enable (Active-High) (posedge TXC).** Indicates that data on the TXD line is valid.
RXCOUNT_[15:0]_	**Receive Byte Count (posedge RXC).** Indicates the number of full bytes received in the current packet. This counter freezes at FFFF(hex) bytes.

Signal Information (continued)

Table 2. Output Terminal Descriptions (continued)

Output Terminal	Description
RXBYTE_[7:0]_	**Receive Byte (posedge RXC)**. An 8-bit latch which holds a byte of receive data.
RXSOP	**Receive Start of Packet (Active-High) (posedge RXC)**. Indicates that the receiver has detected that CRS is high and that RXC is being generated. Receive statistics are reset on the falling edge of RXSOP.
RXSFD	**Start-of-Frame Detect (Active-High) (posedge RXC)**. Indicates that a start-of-frame delimiter has been detected in a received packet (10101011).
RXEOP	**Receive End of Packet (Active-High) (posedge RXC)**. Indicates that CRS has gone inactive and that receive statistics are valid for reading.
RXBVLD	**RX Byte Valid (Active-High) (posedge RXC)**. Active for 1 bit time after a new receive byte has been loaded into the RXBYTE_[7:0]_ latch.
RXJAB	**Receiver Jabber (Active-High) (posedge RXC)**. Indicates that receive packet length was greater than 1518 bytes and that the packet had a bad CRC or a FAE.
FAE	**Frame Alignment Error (Active-High) (posedge RXC)**. Indicates a packet was received with a bit count with a mod 8 remainder other than 0 and that the packet had an incorrect CRC.
CRC	**CRC Error (Active-High) (posedge RXC)**. Indicates a packet was received with a bit count with a mod 8 remainder equal to 0 and that the packet had an incorrect CRC.
RUNT	**RUNT Packet (Active-High) (posedge RXC)**. Indicates a packet was received with a byte count (including CRC) < 64 and the packet had a good CRC.
FRAG	**Collision Fragment (Active-High) (posedge RXC)**. Indicates a packet was received with a byte count (including CRC) < 64 and the packet had a bad CRC or a FAE.
LONG	**Long Packet (Active-High) (posedge RXC)**. Indicates that receive packet length was greater than 1518 bytes and the packet had a good CRC.
PHYS	**Physical Address (Active-High) (posedge RXC)**. Indicates that the first bit of the received packet was 0 and that at least 6 bytes of data were received.
MULT	**Multicast Address (Active-High) (posedge RXC)**. Indicates that the first bit of the received packet was 1, that all address bits were not 1, and that at least 6 bytes of data were received.
BRD	**Broadcast Address (Active-High) (posedge RXC)**. Indicates that all 36 address bits were 1.
SHORT	**Short Frame (Active-High) (posedge RXC)**. Indicates a frame was received with less than 80 bits of preamble and data.
IFG	**Short Interframe Gap (Active-High) (posedge RXC)**. Indicates that the interframe gap prior to the start of the packet was less than 9.6 µs.
NUL	**Null Packet (Active-High) (posedge RXC)**. Indicates that CRS and RXC were active for some time and that no SFD sequence was detected.

Table 3. Additional Scan Outputs

I/O Terminal	Description
TEST_SEI	**Scan Data Input Control (Input) (Active-High).** Used to control data input to scan flip-flops.
TEST_SI1	**Scan Data Input to TXC Scan Chain (Input).**
TEST_SI2	**Scan Data Input to RXC Scan Chain (Input).**
TEST_SO1	**Scan Data Output for TXC Scan Chain (Output) (posedge TXC).**
TEST_SO2	**Scan Data Output for RRXC scan chain (Output) (posedge TXC).**

Signal Information (continued)

Netlist

Inputs: XC, RST, COL, MFDUP, RETRY_1_,
RETRY_0_, BSEL,PREAM_1_,
PREAM_0_, ISQE, DEFER, TXREQ,
TXEOD, ABORT, APNDCRC, INVCRC,
TSTMODE, TXDB_7_, TXDB_6_,
TXDB_5_, TXDB_4_, TXDB_3_,
TXDB_2_, TXDB_1_, TXDB_0_, RXC,
RXD, CRS

Outputs: TXACK, TXINPROG, TXD, TXLD, TXEOP,
LATE, EXDEF, DEF, COLDET, SCOL,
MCOL, CERR, LCRS, SQE, TXBYTE,
TXSOP, TXE, ABORTED,
RXCOUNT_15_, RXCOUNT_14_,
RXCOUNT_13_, RXCOUNT_12_,
RXCOUNT_11_, RXCOUNT_10_,
RXCOUNT_9_, RXCOUNT_8_,
RXCOUNT_7_, RXCOUNT_6_,
RXCOUNT_5_, RXCOUNT_4_,
RXCOUNT_3_, RXCOUNT_2_,
RXCOUNT_1_, RXCOUNT_0_,
RXBYTE_7_, RXBYTE_6_,
RXBYTE_5_, RXBYTE_4_,
RXBYTE_3_, RXBYTE_2_,
RXBYTE_1_, RXBYTE_0_, RXSOP,
RXEOP, RXBVLD, RXJAB, FAE, CRC,
RUNT, FRAG, LONG, PHYS, RXMULT,
BRD, SHORT, IFG, NUL

Functional Description

The DNCM00 consists of two main blocks, the transmitter and receiver. A brief description of each block follows.

Transmitter

The transmitter in the DNCM00 is made up of a state machine, a preamble-jam counter block, a transmit counters block, a 32-bit CRC generator, a 15-bit deferral time-out counter, and a transmit serializer.

A transmit operation is initiated by the host activating TXREQ. When TXREQ is recognized, the DNCM00 will respond by activating TXACK. The DNCM00 will hold TXACK active until TXREQ is dropped, until the transmitter successfully sends the packet, or until transmit is aborted because of excessive collisions, excessive deferral, or a host initiated abort.

Transmission will begin if the 9.6 μs intergap timer has expired. If the timer has reached 9.6 μs prior to TXREQ packet, transmission will begin immediately. If TXREQ is given before 6.4 μs of intergap and the DNCM00 was the last station transmitting, the new packet will begin transmission at 9.6 μs regardless of CRS. If the timer is greater than 6.4 μs and CRS is high, the transmission will defer until CRS deactivates, at which time the 9.6 μs timer will activate and transmission will start after time-out.

Transmitter operation is controlled by a state machine modelled after the one shown in Appendix B of the 1993 version of *IEEE*[*] 802.3.

Immediately prior to starting preamble, the DNCM00 will send a 1 TXC signal, TXSOP, to the host. Another DNCM00 output TXINPROG is valid while the DNCM00 is actively transmitting.

Preamble is programmable by PREAM[1:0] to be 32, 40, 48 or 56 bits, and an 8-bit SFD (10101011) is appended after preamble. The DNCM00 has no address registers, so source and destination addresses must be included in the byte stream sent by the host. The DNCM00 does not provide automatic frame padding.

---

[*] *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Functional Description (continued)

Transmitter (continued)

At the end of preamble the DNCM00 sends a one TXC signal, TXLD, to the host. The DNCM00 strobes in the byte to be transmitted on the falling edge of TXLD. After the first TXLD, subsequent requests will be sent every eight TXC cycles. After the last byte has been sent by the host, the host will signify end of data by activating TXEOD for one TXC. After transmitting the last byte, the DNCM00 will append the CRC to the data stream if the CRC input to the DNCM00 is high. The CRC can also be sent inverted if desired (to force a bad CRC) by setting the INVCRC input high. After completing transmission, the DNCM00 will send a TXEOP signal to the host. All transmit statistics (SCOL, MCOL, CERR, ABORTED, EXDEF, etc.) except SQE can be latched on the falling edge of TXEOP. During transmission, the DNCM00 will activate TXBYTE for one TXC for each byte it sends. For an N-byte packet, the DNCM00 will send N + 4 TXBYTE signals if CRC was appended.

After successful transmission, the DNCM00 will monitor the COL input for an SQE test signal if the ISQE input is low. COL is monitored for the first 6.4 µs of intergap time. If SQE test is not observed, the SQE output will be set to 1 and held until the next TXSOP signal. A control output SQEVALID will be valid from 6.4 µs until TXSOP of the next packet, and SQE is valid when SQEVALID is high.

If another TXREQ is sent before 6.4 µs of intergap, the DNCM00 will attempt to transmit the new packet regardless of CRS. CRS will normally not activate during this time if all stations are observing proper protocol, so this should be an infrequent event.

The DNCM00 handles collision situations in accordance with 802.3. The RETRY[1:0] inputs select 1, 4, 8, or 16 attempts to transmit, with 00 giving the standard 16 attempts. The standard backoff algorithm is used. The DNCM00 has a 12-bit pseudorandom shift register counter that free runs. The counter can be frozen for periods of time by driving the MODRNDM input high. This signal can be a decoded chip enable or some other unique signal to increase the randomness of a group of ATTMACS. When a collision is sensed, a 32-bit jam pattern (1111) is transmitted. After jam is complete, n bits of the counter (n depends on the collision number) is dumped into a 10-bit counter, which in turn is decremented by the turnover of the 51.2 µs timer. Backoff lasts until the 10-bit counter reaches 0. Transmission is reattempted if the 9.6 µs timer has expired or is deferred until CRS deactivates and the 9.6 µs timer expires. If a deferral lasts longer than

24,288 bit times, the DNCM00 will abort the transmission if the DEFER input is set high. This also applies to a deferral at the start of a regular transmission. Deferral is not cumulative; it restarts from 0 each time a deferral state is entered. If a packet cannot be transmitted after making the selected number of attempts, the transmit is aborted and the CERR output is activated. If a collision occurs during preamble, the preamble-SFD sequence is completed prior to jamming.

The COLDET output indicates the presence of a collision situation to the host. If a late collision (after 512 bit times, including preamble and SFD) occurs, the LATE output will be set high. The MAC does not abort after a late collision is detected. This must be done by the host. If the DNCM00 detects a collision while transmitting, it will always send a jam pattern prior to deactivating TXE regardless of the status of ABORT, TXEOD, or the status of the collision counter. The host should always reset its transmit stack if the COLDET output goes high to ensure complete packet transmission.

The BSEL input can be used to override the backoff timer if desired. If BSEL is 1 and a collision is detected, the DNCM00 will jam and retransmit when the 9.6 µs IGT has expired. If the MFDUP is high (full-duplex mode), the DNCM00 ignores the collision signal.

Functional Description (continued)

Receiver

The DNCM00 receiver consists of a state machine, CRC generator, 64 Kbyte counter, and deserializer.

When the DNCM00 detects a low-to-high transition of CRS and RXC is operating, it will send an RXSOP signal to the host. The first 10 bits of preamble sensed are ignored. After the first 10 bits of preamble, a SFD sequence (10101011) will cause an RXSFD signal to be sent. After RXSFD, the receiver will buffer each byte of received data. After assembling the byte, a 1 RXC RXBVLD signal will be sent to the host. The host has eight RXC times to read the byte from the RXBYTE register. When CRS falls, the receiver monitors the result of CRC calculated on the last full byte. If CRS falls on a byte boundary, the packet is either good or a CRC error. If CRS falls on a nonbyte boundary, but the last full byte received had a good CRC, its a good packet with dribble bits. If CRS falls on a nonbyte boundary and the last full byte CRC was bad, it is a frame alignment error. The receiver will inform the host of the end of packet by activating the RXEOP output for one RXC.

Other receive statistics include RXJAB (packet with >1518 bytes and a CRC or FAE), LONG (>1518 bytes with good CRC), NUL (CRS high for indefinite time with no SFD), and others that are described in the terminal descriptions list. Receive statistics are valid from RXEOP to the next RXSOP.

If the MFDUP input is low (half duplex), the receiver will ignore any packets that start while TXE is high to avoid buffering ones own transmitted packet. In order to prevent glitches on CRS during a collision situation from affecting the receiver, the receiver will ignore high-to-low transitions of CRS if a packet reception is in progress and the COL signal is present. If MFDUP is high (full duplex), the receiver will ignore the COL signal.

The DNCM00 does not have any physical address registers or multicast address registers, nor does it have any multicast address group detection logic. It does have three outputs, PHYS, RXMULT and BRD, one of which will activate after 6 bytes of data have been received. PHYS means the first bit of data in the packet was 0; RXMULT means the first bit was 1, and at least 1 of the next 47 was 0; and BRD is a 48-bit address of all 1s.

General Information

The DNCM00 is approximately 4100 gates without scan logic. It exists as a fully synthesizable *Verilog* HDL behavioral/state table description and can be easily modified for specific customer requirements.

microelectronics group

Lucent Technologies
Bell Labs Innovations