								F	REVISI	ONS										
LTR						DESCF	RIPTIO	N						DA	ΛTE		APPROVED			
A	lette	Removed vendor CAGE 61772 as source of supply for case outline letter Z, the F-11A package. Added case outline letters U and T, F-11 and D-15 to the drawing. Editorial changes throughout.						1990 OCT 04		M. A. Frye										
В	Cha	nges i	n acco	ordanc	dance with NOR 5962-R042-95.					94-12-15			M. A	. Frye						
С							n													
THE ORIG	JINA	L FIF	STI	PAG	ΕO	FTH	IS DI	RAW	'ING	HAS	BEI	EN R	EPL	ACE	D.					
REV																				
SHEET																				
REV	С	С																		
SHEET	15	16																		
REV STATUS				REV	/		С	С	С	С	С	С	С	С	С	С	С	С	С	С
OF SHEETS				SHE	ET		1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A					PAREI neth Ri						D	EFEN	SE SI	UPPL	Y CE	NTER	COL	UMB	US	
MICRO	NDAR DCIRC AWIN(UIT			CKED Monnir								COL	UMB	US, O	HIO	43216	5		
THIS DRAWIN FOR USE BY A					ROVEI ael. A.					CM	IOS,		ALL	EL 5	EMC 12 X DN			TAL	,	
AND AGEN DEPARTMEN	NT OF E	DEFEN				23 Ma	OVAL E ay 1988													
AM	SC N/A			REV	ISION	LEVEL	C				ZE 4 ET		GE CC 67268			Ę	5962-	8753	1	
	1 OF 16																			

1. SCOP	Έ
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1.1 <u>Scope</u>. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

<u>5962-87531</u>	<u>01</u>	<u>x</u> 	<u></u>	ine renering enampier	
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finis (see 1.2.		
1.2.1 Device type(s).	The device type(s) sha	II identify the cir	cuit function as fo	llows:	
Device type	Generic number		<u>Circuit</u>	Access tim	<u>e</u>
01 02 03	7201 7201 7201 7201	512 X 512 X	9-bit parallel FIF(9-bit parallel FIF(9-bit parallel FIF(D 50 ns D 80 ns	
Outline letter	The case outline(s) sh	-	Terminal		age style
X Y Z U T	GDIP1-T28 or CQCC1-I CDFP3-I GDFP2-F GDIP4-T28 or	CDIP2-T28 N32 F28 F28	28 32 28 28 28 28	dual-in-l rectangula flat p flat p	ine package ir chip carrier ackage ackage ine package
1.2.3 Lead finish. The	e lead finish is as speci	fied in MIL-PRF	-38535, appendix	Α.	
1.3 Absolute maximur	<u>n ratings</u> . <u>1</u> /				
DC output current (Ic Ambient storage temp Temperature under b Thermal resistance, j	(V _{CC}) poerature ias unction-to-case (Θ _{JC}) ipation (P _D):		50 mA -65°C to +150°C -55°C to +125°C See MIL-STD-18		
1.4 Recommended op	perating conditions. 1/				
Ground voltage (V _{SS}) Minimum high level ir Maximum low level in Case operating tempo Rise time	(V_{CC}) nput voltage (V_{IH}) put voltage (V_{IL}) erature range (T_C)		0 V dc 2.0 V dc 0.8 V dc -55°C to +125°C 5 ns		
1/ All voltages reference $2/$ Must withstand the ac		cuit test; e.g., lo	DS.		
	TANDARD IRCUIT DRAWING		SIZE A		5962-87531
	LY CENTER COL S, OHIO 43216-50			REVISION LEVEL C	SHEET 2
DSCC FORM 2234					

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits. MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's). MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 <u>Item requirements</u> The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 <u>Truth table</u>. The truth table shall be as specified on figure 2.

3.2.4 <u>Die overcoat</u>. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection provided that each coated microcircuit inspection lot (see MIL-PRF-38535, appendix A) shall be subjected to and pass the Internal Water-Vapor Content test (test method 1018 of MIL-STD-883). The frequency of the internal water vapor testing may not be decreased unless approved by the preparing activity.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87531
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 3

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 - (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}C$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after any design or process changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.
- d. Subgroups 7 and 8 tests shall include verification of the truth table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87531
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 4

		TABLE I. Electrical performance	characteristi	<u>cs</u> .			
Test	 Symbol 	Conditions $-55^{\circ}C \leq T_{C} \leq +125^{\circ}C$ $V_{SS} = 0 V$ $4.5 V \leq V_{CC} \leq 5.5 V$	 Group A subgroups	 Device types 		mits	 Unit
Input leakage current	 I _{LI}	unless otherwise specified 0.4 V ≤ V _{IN} ≤ V _{CC}	1, 2, 3	 All	<u>Min</u> -10	<u>Max</u> 10	 μΑ
Output leakage current	 I _{LO}	$0.4 \text{ V} \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{CC}}, \overline{\text{R}} \geq \text{V}_{\text{IH}}$	 1, 2, 3	 All	-10	10	 μΑ
Output low voltage	V _{OL}	$V_{CC} = 4.5 \text{ V}, I_{OL} = 8.0 \text{ mA}$ $V_{IL} = 0.8 \text{ V}, V_{IH} = 2.2 \text{ V}$	1, 2, 3	 All		0.4	V
Output high voltage	 V _{он}	$ V_{CC} = 4.5 \text{ V}, I_{OH} = -2.0 \text{ mA} $ $ V_{IL} = 0.8 \text{ V}, V_{IH} = 2.2 \text{ V} $	 1, 2, 3	 All	2.4	 	V
Operating supply current	 I _{CC1} 	│ │ f = maximum, outputs open, │ V _{CC} = maximum	 1, 2, 3 	 All 		 100 	 mA
Standby power supply current	 I _{CC2} 	│ = = = T = V _{IH} , │ outputs open	1, 2, 3	 All		 15 	 mA
Power down current	 CC3	All inputs = V _{CC} - 0.2 V, outputs open	 1, 2, 3 	 All		 900 	 μΑ
Input capacitance <u>1</u> /	C	V₁ = 5.0 V or GND, f = 1 MHz T _C = +25°C, See 4.3.1c	4	 All 		 5 	 pF
Output capacitance <u>1</u> /	C _o	V ₀ = 5.0 V or GND, f = 1 MHz T _C = +25°C, See 4.3.1c	4	 All		 7 	 pF
Functional tests		See 4.3.1d.	 7, 8A, 8B	 All		 	

See footnotes at end of table.

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DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
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		TABLE I. Electrical per	formance charac	cteristic	<u>cs</u> .			
Test	Symbol 	Conditions <u>2/</u> -55°C <u>≤</u> T _C <u>≤</u> +125°C V _{SS} = 0 V 4.5 V <u>≤</u> V _{CC} <u>≤</u> 5.5 V	C Group subgr		Device types	 L	imits	 _ Unit
		unless otherwise speci				Min	Max	
					01	40	ļ	<u> </u>
Read cycle time	t _{RC}		9, 10,	11	02	65		ns
			<u> </u>		03 01	100	30	
Access time	t _A		9, 10,	11	02		50	 ns
			-,,		03		80	+
			<u> </u>		01	10		
Read recovery time	t _{RR}		9, 10,	11	02	15		ns
			<u> </u>		03	20		-
Read pulse width			9, 10,	11	01 02	30 50		
Read puise width	t _{RPW}		9, 10,		02	80		ns
			+		05	00	1	
Read pulse low to data bus at low-Z	t _{RLZ} <u>4</u> /		9, 10,	11	All	5		ns
Write pulse low to data bus at low-Z	t _{WLZ} <u>4</u> /		9, 10,	11	All	5		ns
Data valid from read pulse high	t _{DV}		9, 10,	11	All	5		ns
Read pulse high to data bus at high-Z	t _{RHZ} <u>4</u> /		9, 10,	11	<u>01</u> 02,03		20 30	ns
					01	40		<u> </u>
Write cycle time	t _{wc}		9, 10,	11	02	65		ns
			<u> </u>		03	<u>100</u> 30		
Write pulse width	t _{wew}		9, 10,	11	01 02	50	1	ns
			0, 10,		03	80		113
			1		01	10		
Write recovery time	t _{WR}		9, 10,	11	02	15	Ì	ns
			<u> </u>		03	20		
					01	18		+
Data setup time	t _{DS}		9, 10,	11	02 03	30 40		ns
			<u> </u>		03	0		
Data hold time	t _{DH}		9, 10,	11	02	5		 ns
			0, 10,		03	10	1	1 110
			1	i	01	40	1	
Reset cycle time	t _{RSC}		9, 10,	11	02	65		ns
	-		1	[03	100	ļ	
Department 111				4.4	01	30	<u> </u>	<u> </u>
Reset pulse width	t _{RS}		9, 10,	11	02	50		ns
			<u> </u>		03 01	80		
Reset recovery time	t _{RSR}		 9, 10,	11	01	10		 ns
	×ror		3, 10,		03	20	1	
See footnotes at end of ta	ible.							
ST MICROCI	FANDARD RCUIT DR		SIZE A				59	62-87531
DEFENSE SUPP COLUMBUS				RE'	VISION LE C	EVEL	SHE	ET 6

		TABLE I. Electrical performanc	e characterist	CS.			
Test	 Symbol	Conditions $2/3/$ -55°C \leq T _C \leq +125°C V _{SS} = 0 V	Group A subgroups	 Device types	 L	imits	Unit
		4.5 V <u><</u> V _{CC} <u><</u> 5.5 V unless otherwise specified			Min	 Max	
	i i			01	30		Ĺ
Reset setup time	t _{RSS}		9, 10, 11	02	50		ns
				03	80		
				01	40		\perp
Retransmit cycle time	t _{RTC}		9, 10, 11	02	65		ns
				03	80		
				01	30		\perp
Retransmit pulse width	t _{RT}		9, 10, 11	02	50		ns
				03	80		
				01	10		\perp
Retransmit recovery	t _{RTR}		9, 10, 11	02	15		ns
time		<u> </u>		03	20		
				01		40	<u> </u>
Reset to empty flag low	tefl		9, 10, 11	02		65	ns
				03		100	
				01		30	ns
Read low to empty flag	t _{REF}		9, 10, 11	02		45	1
low				03		60	
	j j		 9, 10, 11	01		30	ns
Read high to full flag	t _{RFF}			02		45	1
high			ĺ	03		60	<u> </u>
	1			01		30	ns
Write high to empty	twer		9, 10, 11	02	İ	45	Ĺ
flag high	j		j	03		60	
				01		30	ns
Write low to full flag	t _{WFF}		9, 10, 11	02		45	Ī
low			ĺ	03	ĺ	60	<u> </u>
	t _{HFH}			01		40	
Reset to half-full and	t _{FFH}		9, 10, 11	02		65	ns
full flag high				03		100	
	j j			01		30	ĺ
Read/write to \overline{XO} low	t _{XOL}		9, 10, 11	02		50	ns
				03		80	
	j j			01		30	ĺ
Read/write to \overline{XO} high	t _{XOH}		9, 10, 11	02		50	ns
		<u> </u>		03		80	
				01	30		1
XI pulse width	t _{XI}		9, 10, 11	02	50		ns
	j j			03	80		
XI recovery time	t _{XIR}		 9, 10, 11 	All	 10		 ns
XI setup time	t _{xis}		9, 10, 11	 All	15		 ns

1/ This parameter tested initially and after any design or process change which could affect this parameter, and is therefore <u>1</u>/ This parameter tested mining and after any design of process change which guaranteed to the limits specified in table I.
<u>2</u>/ For output load circuit and ac test conditions, see figure 3.
<u>3</u>/ For timing waveforms, see figure 4.
<u>4</u>/ May not be tested, but shall be guaranteed to the limits specified in table I.

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Device types	All			
Case outlines	X, Z, U, T	Y		
Terminal number	Terminal symbol			
1	 W	 NC		
2 3 4 5 6	D ₈ D ₃ D ₂ D ₁ D ₀	W D ₈ D ₃ D ₂ D ₁		
7		D ₀		
8	' FF	<u>x</u>		
9 10 11	Q ₀ Q ₁ Q ₂	FF Q ₀ Q ₁		
12 13 14	Q ₃ Q ₈ GND	NC Q ₂ Q ₃		
15 16 17	R Q4 Q5	Q ₈ GND NC		
18 19	Q ₆ Q ₇	R Q4		
20	<u> </u>	Q ₅		
21	EF	Q ₆		
22	RS	Q7		
23	' FL/RT	<u></u> XO/HF		
24	D ₇	EF		
25	D ₆	RS		
26 27 28 29 30 31 32	D5 D4 V _{CC} 			

FIGURE 1. Terminal connections.

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Reset and retransmit Single device configuration/width expansion mode

Mode		Inputs		Internal status		C	Outputs	
	 RS	 RT 	 _XI	 Read pointer 	 Write pointer 	 EF 	 FF 	 HF
Reset Retransmit	0	X 0	0	Location zero	Location zero	0 X	 1 X	 1 X
Read/write	1	1 	0	Increment <u>1</u>	Increment <u>1</u> /	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load Depth expansion/compound expansion mode

		Input	3	 Internal	status	 Outp	outs
 Mode 	 RS	 FL 	 _XI	 Read pointer 	 Write pointer 	 EF 	 FF
Reset first device Reset all other devices Read/write	001	0 1 X	<u>1</u> / <u>1</u> / <u>1</u> /	Location zero	Location zero Location zero X	0 0 X	1 1 X

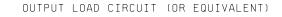
1/ XI is connected to XO of previous device.

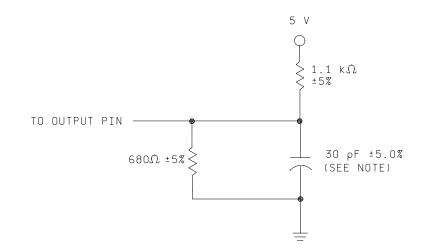
NOTES: \overrightarrow{RS} = Reset input, $\overrightarrow{FL/RT}$ = First load/retransmit, \overrightarrow{EF} = Empty flag output,

 \overline{FF} = Full flag output, \overline{XI} = Expansion input, and \overline{HF} = Half-full flag output 0 = Low level voltage 1 = High level voltage X = Don't care

FIGURE 2. Truth tables.

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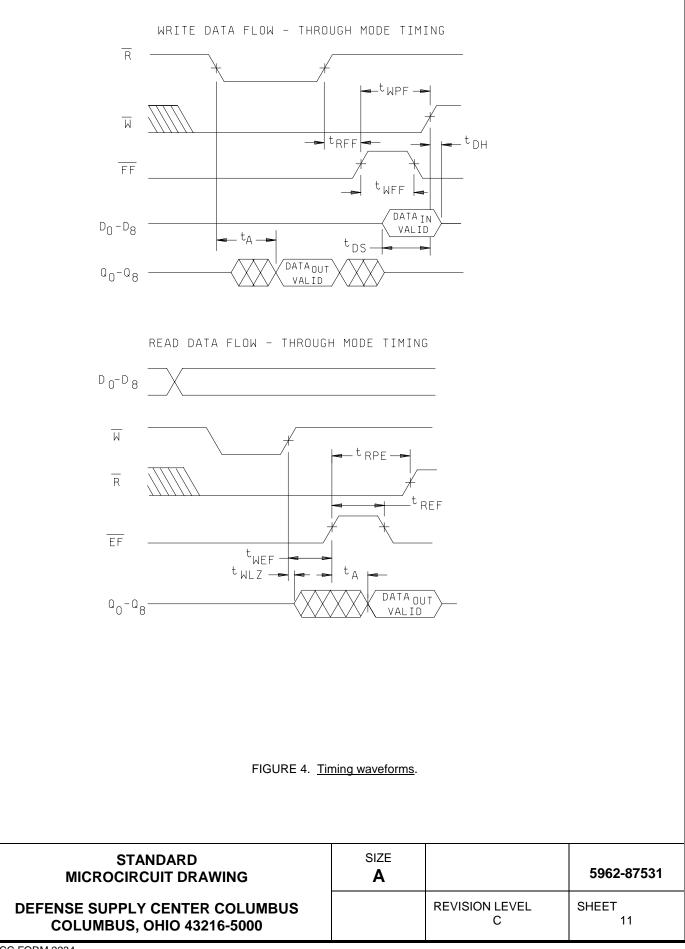
NOTE: C_L includes scope and jig capacitance.

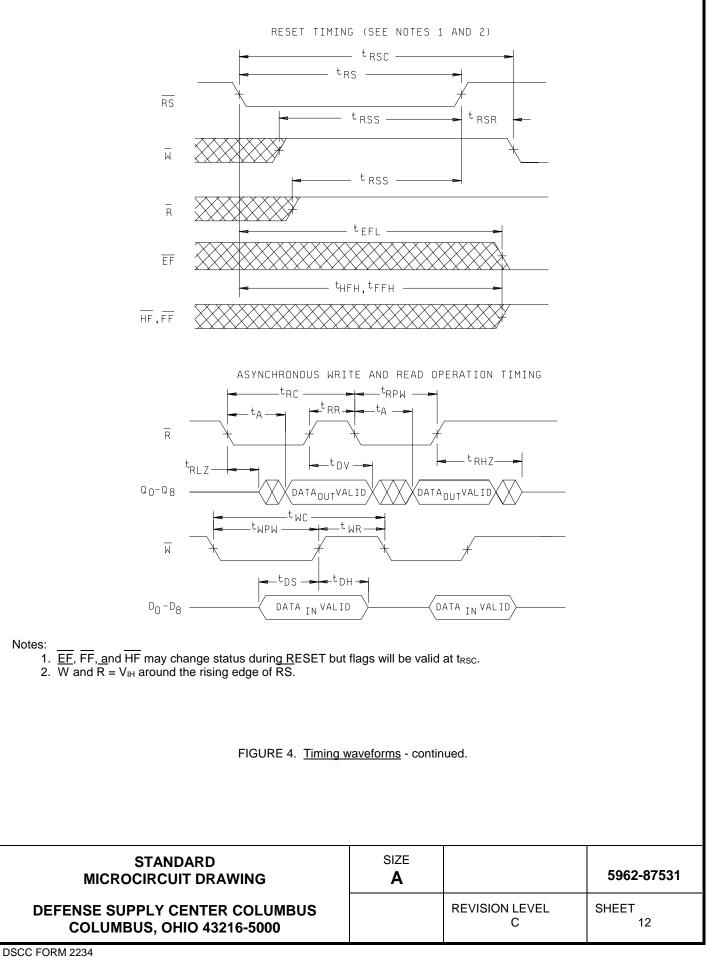
AC test conditions

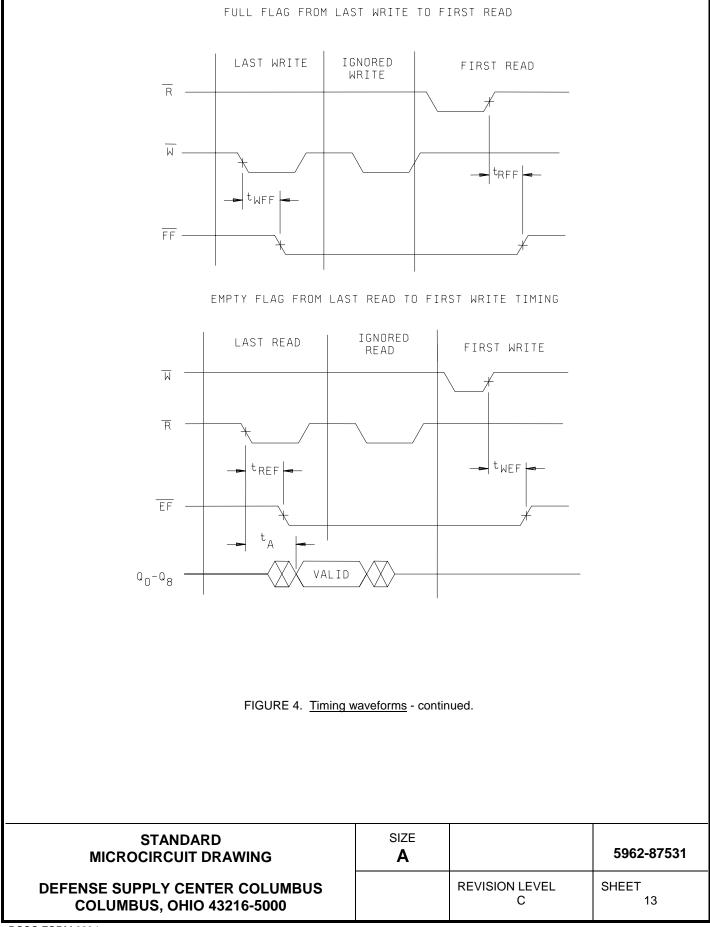
Input pulse levels	GND to 3.0 V	İ
Input rise and fall times	5 ns	İ
Input timing reference levels	1.5 V	İ
Output reference levels	1.5 V	İ
		İ

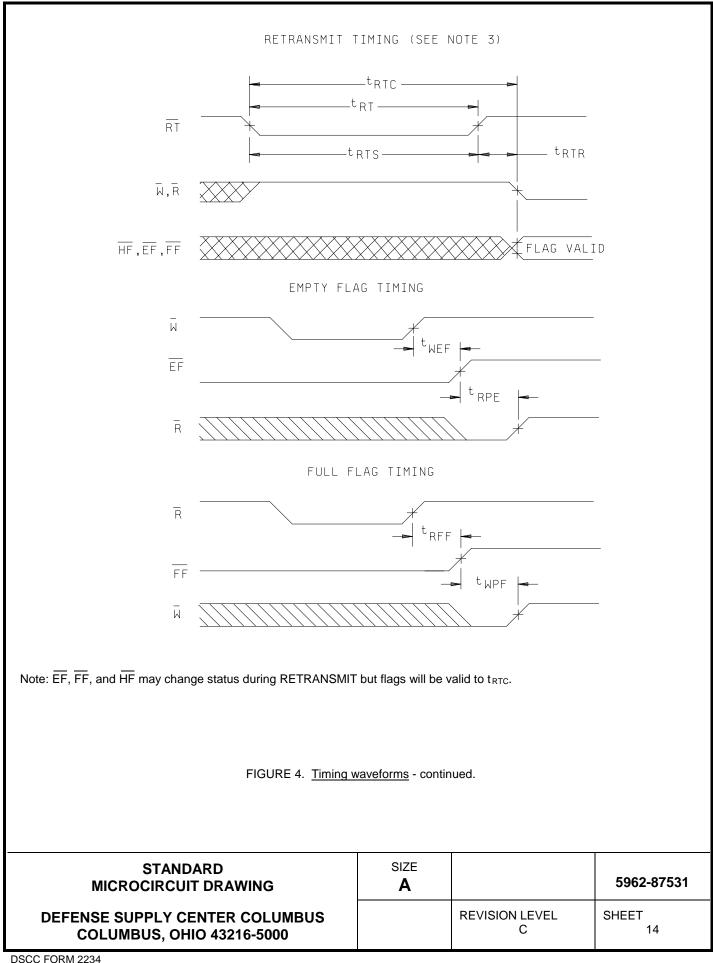
FIGURE 3. Output load circuit and ac test conditions.

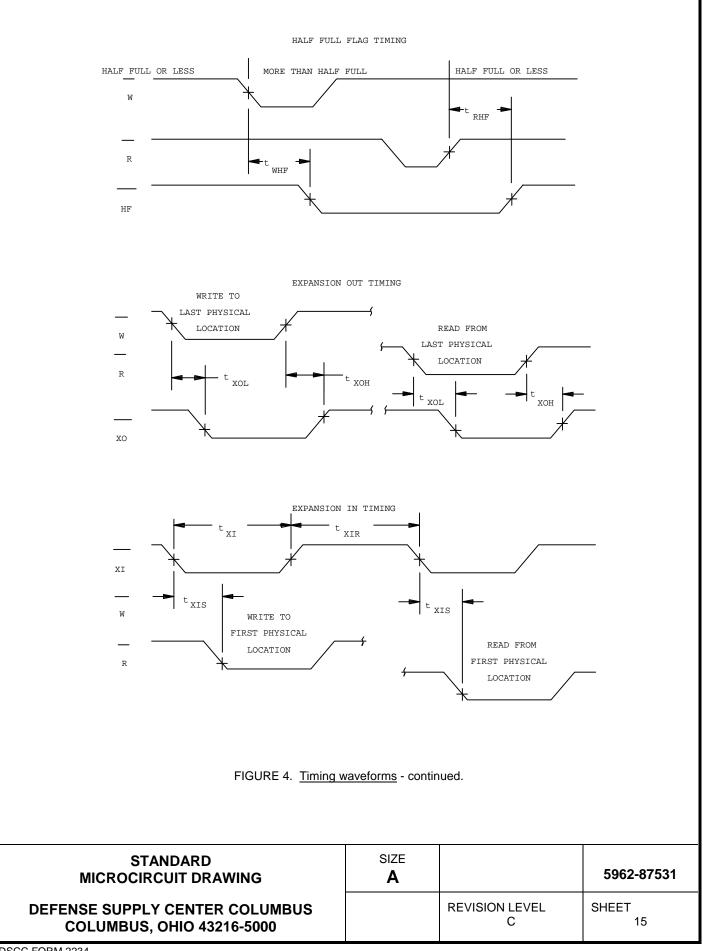
STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87531
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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
- (1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- (2) $T_A = +125^{\circ}C$, minimum.
- (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8A, 8B

TABLE II. Electrical test requirements. *

* Indicates PDA applies to subgroups 1 and 7.

** See 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractorprepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone 614-692-0674.

6.6 <u>Approved source of supply</u>. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-01-17

Approved sources of supply for SMD 5962-87531 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit <u>1</u> / drawing PIN	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8753101XA	61772	IDT7201LA30DB
5962-8753101YA	61772	IDT7201LA30XB
5962-8753101ZA	<u>3</u> /	IDT7201LA30XB
5962-8753101UA	61772	IDT7201LA30XEB
5962-8753101TA	61772	IDT7201LA30TCB
5962-8753102XA	61772	IDT7201LA50DB
5962-8753102YA	61772	IDT7201LA50XB
5962-8753102ZA	<u>3</u> /	IDT7201LA50XB
5962-8753102UA	61772	IDT7201LA50XEB
5962-8753102TA	61772	IDT7201LA50TCB
5962-8753103XA	61772	IDT7201LA80DB
5962-8753103YA	61772	IDT7201LA80XB
5962-8753103ZA	<u>3</u> /	IDT7201LA80XB
5962-8753103UA	61772	IDT7201LA80XEB
5962-8753103TA	61772	IDT7201LA80TCB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- $\underline{3}$ / No longer available from an approved source.

Vendor CAGE Vendor name number and address 61772 Integrated Device Technology, Incorporated 2975 Stender Way Santa Clara, CA 95054

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.