



BIPOLAR ANALOG INTEGRATED CIRCUIT μ PC1486, μ PC1487C

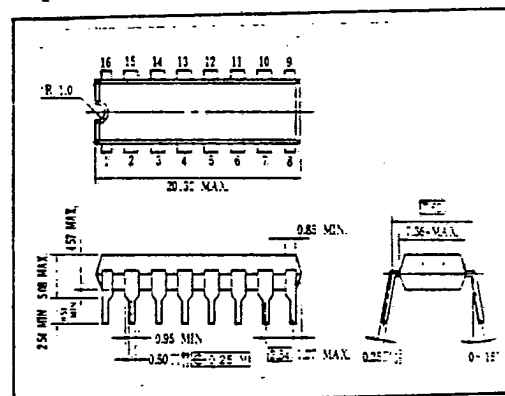
DTS INTERFACE FOR TV

The μ PC1486C or the μ PC1487C is an interface IC for PLL frequency synthesizer digital tuning system of TV. This IC contains all circumferential function block of PLL system, so it can reduce many external components. This IC, with the μ PD1709C (PLL & controller) and the μ PB562AC (prescaler), constitutes a high performance PLL tuning system of TV. It's packed in 16 pins dual in-line package.

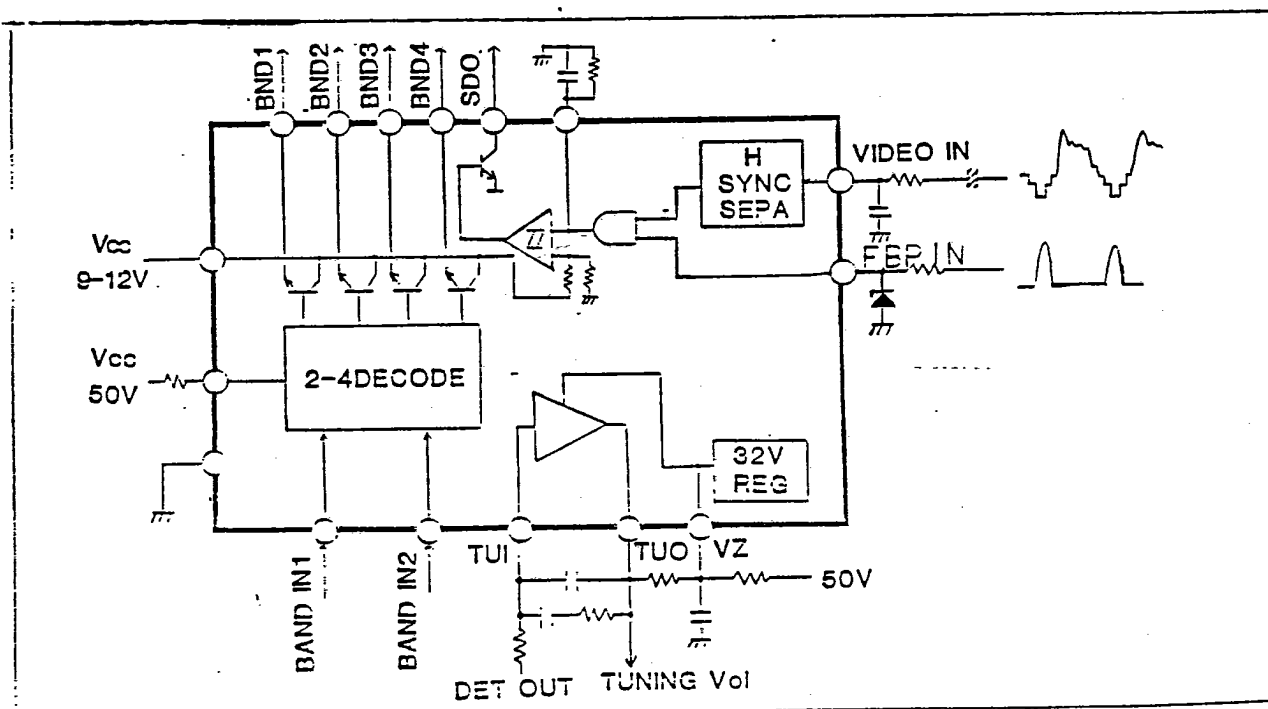
FEATURES

- It contains all circumferential function block of PLL system.
- Internal synch. separator for station detector.
- Band output : large supply current and low saturation voltage.
 $I_{OH} = -40 \text{ mA}$; $V_{Osat} = 0.3 \text{ V TYP.}$
- Compact package : 16 pins DIP.

PACKAGE DIMENSIONS in millimeters



IC BLOCK DIAGRAM



The diagram illustrates the architecture of a digital video receiver. It features a central microcontroller, the **PLL & Controller (μPD1709C)**, which is bidirectionally connected to an external memory or data bus. The system includes several key functional blocks:

- VHF/UHF Tuner**: Receives signals from an antenna and provides control signals to the **Decode & Drive** block and the **IF Block**.
- IF Block (μPC1413CA)**: Processes the intermediate frequency signal and outputs **Sound** and **Video** signals. It also provides control signals to the **Decode & Drive** block and the **PLL & Controller**.
- Decode & Drive**: Receives control signals from the **VHF/UHF Tuner** and **IF Block**, and provides control signals to the **PLL & Controller**.
- Error Amp.**: Receives control signals from the **Decode & Drive** block and the **PLL & Controller**.
- Prescaler (μPB552AG)**: Receives control signals from the **IF Block** and the **PLL & Controller**.
- 33V Zener**: Provides a reference voltage to the **Decode & Drive** block.
- Sync. Sep.**: Receives control signals from the **Decode & Drive** block and the **PLL & Controller**.
- Station Det.**: Receives control signals from the **Sync. Sep.** block and the **PLL & Controller**.

The **PLL & Controller (μPD1709C)** is the central processing unit, managing the system's operation and interfacing with the external bus. The **IF Block (μPC1413CA)** and **Prescaler (μPB552AG)** are specialized integrated circuits used for signal processing and frequency control.

Band Input 1	1	16	Band Output 1
Band Input 2	2	15	Band Output 2
Sync. Sep. Input	3	14	Band Output 3
FEP Input	4	13	Band Output 4
GND	5	12	Vcc 1
SD Filter	6	11	Vcc 2
SD Output	7	10	Vz
Error Amp. Input	8	9	Error Amp. Output

ABSOLUTE MAXIMUM RATINGS ($T_a=25\pm 3^\circ\text{C}$)

RATINGS	SYMBOL	CONDITION	LIMIT	UNIT
Supply Voltage	V_{CC}		14.4	V
Band Output Current	I_{OH}		-60	mA
Band Output Supply Voltage	V_{OL}		-15	V
Vz Current	I_z		15	mA
SD Output Supply Voltage	V_{OH}		15	V
Band Input Voltage	V_T		0 ~ V_{CC}	V
Sync. Sep. Input Voltage	V_{CV}		0 ~ 5	V _{p-p}
Error Amp. Input Voltage	V_{AT}		0 ~ V_{CC}	V
Error Amp. Output Current	I_{AO}		-5	mA
FBP Input Voltage	V_{FBP}		V_{CC}	V _p
Power Dissipation	P_D	$T_a=65^\circ\text{C}$	600	mW
Operating Temperature	T_{opt}		-20 ~ +65	$^\circ\text{C}$
Storage Temperature	T_{stg}		-40 ~ +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	RECOMMENDED VALUE	UNIT
Supply Voltage	V_{CC}	8.1 ~ 13.2	V
Band Input High Level Voltage	e_{BIH}	3.2 ~ 5.5	V _{DC}
Band Input Low Level Voltage	e_{BIL}	0 ~ 0.8	V _{DC}
Video Signal Input Voltage	e_{iv}	2	V _{p-p}
FBP Input Voltage	e_{FBP}	3.5 ~ V_{CC}	V _p

ELECTRICAL CHARACTERISTICS ($T_a=25\pm 3^\circ\text{C}$, $V_{cc}=12\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I_{cc}	Error Amp. Output: High Band Output: V_{cc}	2.0	6.0	12.0	mA
Band Input Threshold Voltage	V_{ITH}		1.0	2.0	3.0	V_{DC}
Band Output Saturation Voltage	V_{Osat}	$I_{OL} = -40\text{mA}$	-	0.3	0.7	V
Band Output Leak Current	I_{OL}	$V_{OL} = -15\text{V}$	-	-	-50	μA
Zener Stabilized Voltage	V_z	$I_z = 5\text{mA}$	31	33	35	V
Stabilized Voltage Temperature Drift	$\Delta V_z / \Delta T$	$T_a = -20 \sim +65^\circ\text{C}$, $I_z = 5\text{mA}$	-5	0	+5	$\text{mV}/^\circ\text{C}$
Dynamic Resistance	r_z	$I_z = 5\text{mA}$	-	10	25	Ω
Error Amp. Input Bias Current	I_{BIAS}		-	-	200	nA
Error Amp. Minimum Output Voltage	V_{AOI}		-	0.2	0.5	V

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Error Amp. Maximum Output Voltage	V_{AOH}		$V_Z-1.5$	$V_Z-0.6$	-	V
Error Amp. Reference Voltage	V_{Aref}		1.5	2.0	2.5	V
Comperator Reference Voltage	V_{cref1}	No signal → Signal	6.5	7.0	7.5	V
Comperator Reference Voltage	V_{cref2}	Signal → No signal	4.5	5.0	5.5	V
SD Output Low Level Voltage	V_{OL}	$I_{OL}=1mA$	-	0.2	0.5	V
SD Output Leak Current	I_{OH}	$V_{OH}=13.2V$	-	-	5	μA

BAND OUTPUT PATTERN

Pattern A (μ PC1486C).

B.I.1	B.I.2	B.O.1	B.O.2	B.O.3	B.O.4
L	L	H	Z	Z	Z
H	L	Z	H	Z	Z
L	H	Z	Z	H	Z
H	H	Z	Z	Z	H

Pattern B (μ PC1487C).

B.I.1	B.I.2	B.O.1	B.O.2	B.O.3	B.O.4
L	L	Z	Z	H	Z
H	L	H	Z	H	Z
L	H	H	H	H	Z
H	H	H	Z	Z	H

Z : High Impedance

APPLICATION CIRCUIT

