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SSI 79W2522
Dual 4-bit ADCs

Advance Information

September 1995

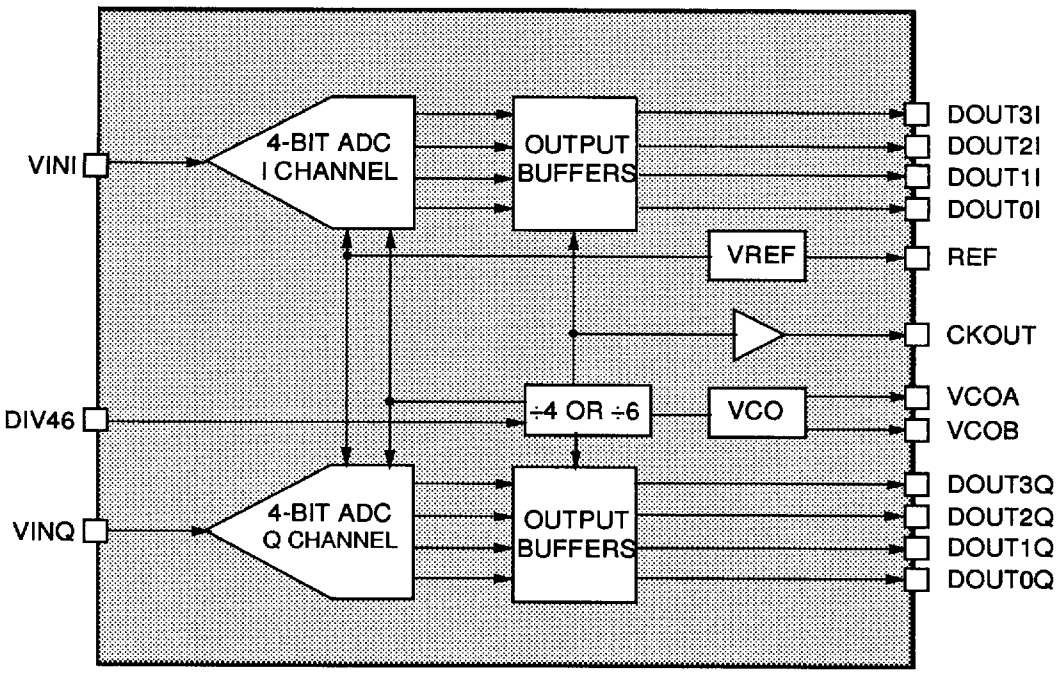
DESCRIPTION

The SSI 79W2522 is a low cost, high performance dual 4-bit (6-bit linearity) analog to digital converter IC with VCO and programmable clock divider. The device supports conversion rates from 20 to 60 M samples per second based on the VCO frequency and the clock divider selection. A typical application for the 79W2522 is analog-to-digital conversion in QPSK demodulation systems that require recovery of multiple baseband frequencies, such as digital satellite receiver boxes.

FEATURES

- **Matched 4-bit flash analog-to-digital converters**
  - **6-bit linearity (0.25 LSB)**
  - **Maximum 1% gain mismatch**
  - **Maximum phase mismatch of 2 degrees**
  - **Internal voltage reference**
- **20 to 60 Msps conversion rates**
- **Internal VCO drive circuitry (requires external LC and phase detector)**
  - **Internal divide-by-4 and divide-by-6 switching**
- **TTL compatible outputs**
- **5 volt operation**
- **28-pin SOL package (optional 28-pin PLCC or 32 pin QFP)**

BLOCK DIAGRAM



FINCTIONAL DESCRIPTION

The 79W2522 contains dual 4-bit flash analog-to-digital converters that are synchronously sampled by an internally generated clock signal. The device accepts two analog input signals within a range of 0 to 1.0 Vp-p that are AC coupled into the VINI and VINQ pins of the device. The device provides two 4-bit parallel outputs that represent the digitized value of the input signals. An internal VCO generates the internal sample clock for the ADCs. The sample clock is also buffered and provided as an external clock signal (CKOUT) for the parrallel data outputs.

ANALOG TO DATA DIGITAL CONVERTERS (ADCs)

The 79W2522 contains two matched 4-bit flash ADCs that support sampling frequencies up to 60 Msps. The input signals to the ADCs are typically AC coupled into pins VINI and VINQ. The input signals are referenced to an internally generated bandgap voltage that is also provided as an output, REF. This output is capable of driving 1 mA into a 1 kΩ load. The ADCs capture samples on the rising edge of the CKOUT signal with the data for that sample being valid on the falling edge of the next clock cycle (reference Figure 2). The 4-bit digitized output data is represented as a Gray code according to the following table:

VCO CLOCK GENERATOR

The internal VCO clock generator consists of a VCO core, output buffering, and a divider circuit that allows the VCO output to te divided either by 4 or 6. The VCO is connected to an external LC tank circuit that controls the ocillation of the VCO over a specified frequency range. The divider circuit allows the VCO to operate over a smaller frequency range while still supporting sample rates from 20 to 60 Msps. Driving the DIVB46 pin high (1) selects a divide-by-4 to support the highest sampling range of 30 to 60 Msps. Driving the DIV46 pin low (0) selects a divide-by-6 to support the lower sampling range of 20 to 40 Msps.

The CKOUT pin is a buffered version of the internal sampling clock. The falling edge of CKOUT is used by external devices to latch the data on the DOUTnI and DOUTnQ pins (reference Figure 2).

ANALOG INPUT	DIGITAL OUTPUT (GRAY CODE)
- (15/2) LSB	0000
- (13/2) LSB	0001
- (11/2) LSB	0011
- (9/2) LSB	0010
- (7/2) LSB	0110
- (5/2) LSB	0111
- (3/2) LSB	0101
- (1/2) LSB	0100
+ (1/2) LSB	1100
+ (3/2) LSB	1101
+ (5/2) LSB	1111
+ (7/2) LSB	1110
+ (9/2) LSB	1010
+ (11/2) LSB	1011
+ (13/2) LSB	1001
+(15/2) LSB	1000

LSB = Input Range/ 16

PIN DESCRIPTION

ANALOG PINS

(Pins marked N/C should be left unconnected during normal use)

NAME	TYPE	DESCRIPTION
VINI	I	I Input. This pin is the analog input to the In-phase ADC (IADC). The input to this pin should be AC coupled.
VINQ	I	Q Input. This pin is the analog input to the Quadrature ADC (QADC). The input to this pin should be AC coupled.
REF	O	Voltage Reference. This pin is an output from the internal voltage reference for the ADCs.
VCOA	I	VCO A. This pin is the input of the VCO. It is connected to an external LC resonator.
VCOB	I	VCO B. This pin is the gain control of the VCO. It is normally left open.
VCOVCC	O	VCO SUPPLY. This pin is the internally generated supply for the VCO. It is connected to an external LC resonator.

DIGITAL PINS

CKOUT	O	Clock Output. This is the output clock for the ADC. Data is clocked out on the rising edge of this output. The falling edge of this output can be used to latch data into an external device.
DIV46	I	Divider Select. This pin selects the divider for the VCO clock output. A low (0) level input selects the divide-by-6 mode. A high (1) level input selects the divide-by-4 mode.
DOUTn1	O	IADC Outputs. These four pins are the digital output of the IADC. They are clocked out on the rising edge of the CKOUT output and should be latched with the falling edge of the CKOUT output.
DOUTnQ	O	QADC Outputs. These four pins are the digital output of the QADC. They are clocked out on the rising edge of the CKOUT output and should be latched with the falling edge of the CKOUToutput.

POWER/GROUND

VPOSD	-	Digital power. These two pins are the power pins for the digital circuitry.
VNEGD	-	Digital ground. These two pins are the ground pins for the digital circuitry.
GND	-	Analog ground. These pins are the analog ground for the VCO and ADCs.
VPOS	-	Analog power. These pins are the analog power supply for the ADCs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage temperature	-55 to 150°C
Junction operating temperature	+110°C
Positive supply voltage (Vp)	-0.3 to 6V
Voltage applied to any pin	-0.3V to VPn+0.3V

TARGET SPECIFICATIONS

Unless otherwise specified: 0° ≤ Ta ≤ 70° C; positive power supply (VDn, VAn) = +5.0 V +/-5%.

OPERATING CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Analog supply current				TBD	mA
Digital supply current				TBD	mA
Power supply rejection ratio	TBD	30			dB

DIGITAL I/O CHARACTERISTICS

High level input voltage		2.0		VPD+0.6	V
Low level input voltage		-0.3		0.8	V
High level input current				50	µA
Low level input current				50	µA
High level output voltage	CL = 25 pF	2.4		VPOSD	V
Low level output voltage	CL = 25 pF	0		0.4	
Output rise time	CKOUT, DOUTnI, DOUTnQ: 0.4V to 2.4V			5	nS
Output fall time	CKOUT, DOUTnI, DOUTnQ: 2.4V to 0.4V			5	nS
Output set up time (Tsu)	DOUTnI, DOUTnQ stable to CKOUT↓	4			nS
Output hold time (Th)	CKOUT ↓ to DOUTnQ, DOUTnI inactive	3			nS
CLK duty cycle		40		60	%

ADC CHARACTERISTICS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input voltage range	AC coupled input	0.0		1.0	Vp-p
Input overvoltage	AC coupled input			2.5	Vp-p
Input resistance	VINI and VINQ	250			Ω
Input capacitance	VINI and VINQ			10	pF
Sampling frequency	VCO clock 150 to 240 MHz	20		60	Msps
Effective number of bits		3.8			bits
ADC Offset error				0.25	LSB
Linearity	Differential			0.25	LSB
	Integral			0.25	LSB
Gain mismatch	VINI=VINQ			1	%
Gain error				5	%
Phase mismatch	VINI=VINQ			2	degree
ADC crosstalk	VINI=1.0 Vp-p, 29 MHz;			-40	dB
	VINQ=1.0 Vp-p, 23 MHz				
	VINQ=1.0 Vp-p, 25 MHz;			-40	dB
	VINI=1.0 Vp-p, 29 MHz				
REF output voltage	VREF loaded with 1 kΩ; I_{VREF} = 1 mA	1.14	1.20	1.26	V

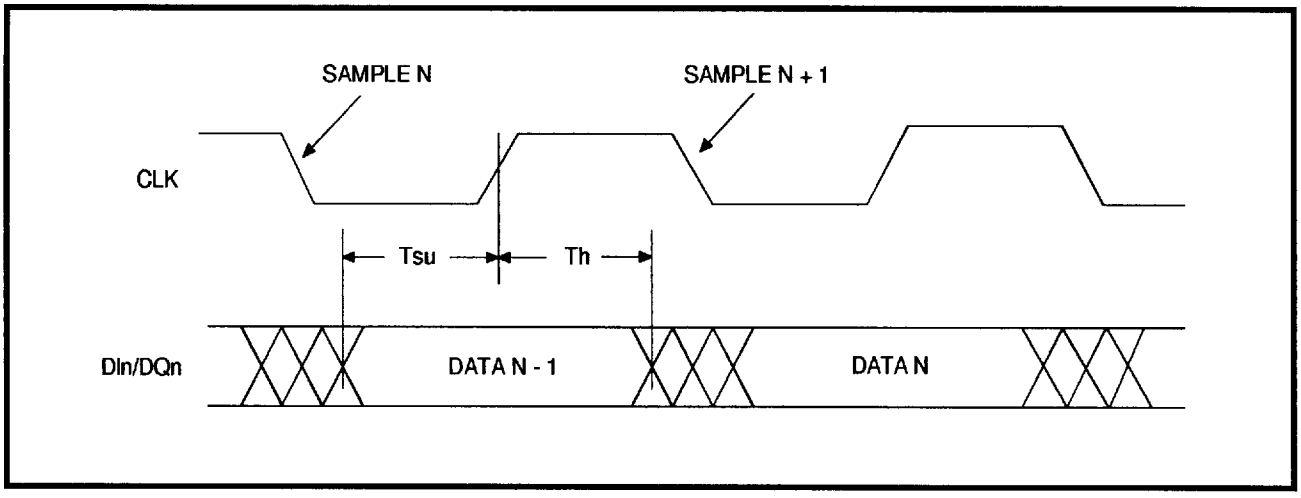
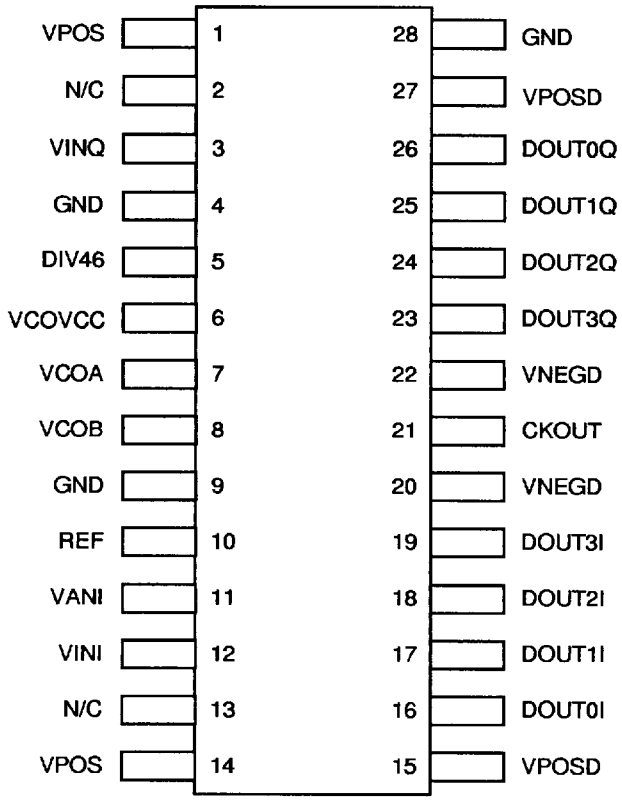


Figure 2: ADC Data Sampling and Output Timing

PACKAGE PIN DESIGNATIONS
(Top View)



79W2522
CL 28-Pin

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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