DN74LS145

BCD to Decimal Decoders / Drivers

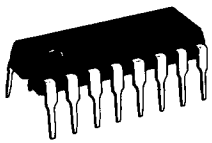
■ Description

DN74LS145 is a BCD to decimal decoder/ driver with open collector outputs.

■ Features

- Large output current ($I_{OL} \leq 80mA$ maximum)
- High withstand voltage level ($V_O \leq 15V$ maximum)
- All output become HIGH during invalid input
- Wide operating temperature range (Ta = −20 to +75°C)

P-2

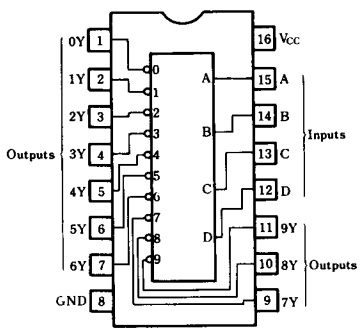


16-pin plastic DIL package

P-5

16-pin Panaflat package (SO-16D)

Pin configuration (top view)



■ Recommended operating conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output voltage	$V_{O(off)}$			15	V
Output current	I_{OL}			80	mA
Operating temperature range	Topr	−20	25	75	℃

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter	Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage	V_{IH}			2.0			V
	V_{IL}					0.8	V
Output current	$I_{O(off)}$	$V_{CC}=4.75V$, $V_{IH}=2V$ $V_{IL}=0.8V$, $V_{O(off)}=15V$				250	μA
Output voltage	$V_{O(on)}$	$V_{CC}=4.75V$ $V_{IH}=2V$ $V_{IL}=0.8V$	$I_{OL}=12mA$		0.25	0.4	V
			$I_{OL}=24mA$		0.35	0.5	V
			$I_{OL}=80mA$		2.3	3.0	V
Input current	I_{IH}	$V_{CC}=5.25V$ $V_I=2.7V$				20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$				−0.4	mA
	I_I	$V_{CC}=5.25V$ $V_I=7V$				0.1	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$ $I_I=-18mA$				−1.5	V
Supply current**	I_{CC}	$V_{CC}=5.25V$			7	13	mA

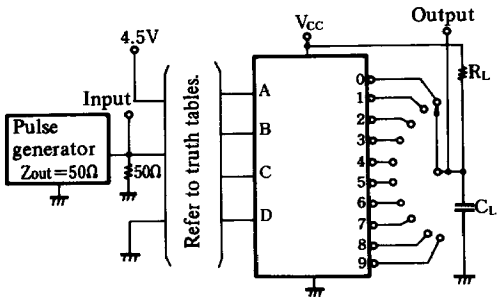
* When constant at V_{CC} = 5V, Ta = 25°C.
** Measured with all outputs open and all inputs grounded.

■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Test conditions	Min	Typ	Max	Unit
Propagation delay time	t_{PLH}	$C_L=45pF$ $R_L=665Ω$			50	ns
	t_{PHL}				50	

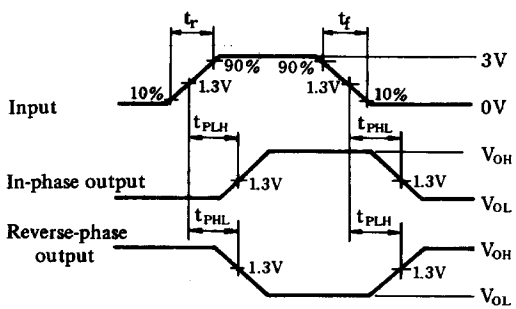
※ Switching parameter measurement information

1. Measurement circuit



Notes
1. C_L includes probe and tool floating capacitance.

2. Waveforms



Notes
1. Input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR = 1MHz, duty cycle = 50%.

■ Truth tables

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.

■ Logic diagram