

# CAT59C11A

## 1K BIT SERIAL E<sup>2</sup>PROM

Preliminary

### DESCRIPTION

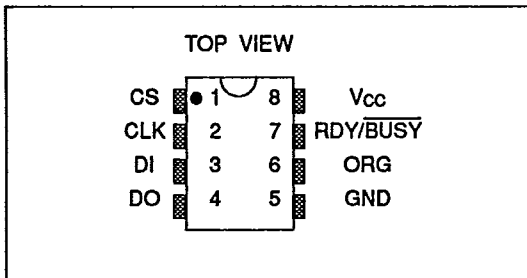
The CAT59C11A is a 1K bit Serial E<sup>2</sup>PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11A is manufactured using Catalyst's advanced CMOS E<sup>2</sup>PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201).

### FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection



### PIN CONFIGURATION

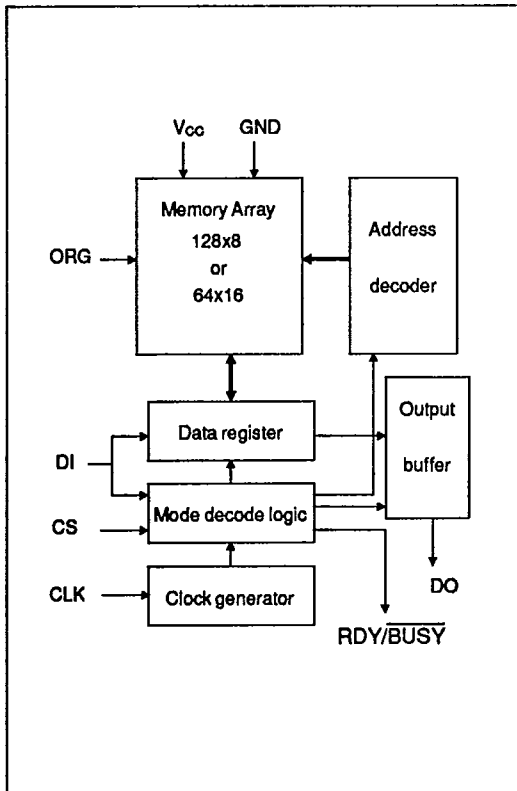


### PIN FUNCTIONS

<b>CS</b>	Chip select
<b>CLK</b>	Clock input
<b>DI</b>	Serial data input
<b>DO</b>	Serial data output
<b>Vcc</b>	+5V power supply
<b>RDY/BUSY</b>	Status output
<b>GND</b>	Ground
<b>ORG</b>	Memory organization

**Note:** When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

### BLOCK DIAGRAM





**ABSOLUTE MAXIMUM RATINGS \***

Storage temperature . . . . .	-65°C to +150°C
Power supply (Vcc) . . . . .	+7 V
Voltage on any input pin . . . . .	-0.3 to +7V
Voltage on any output pin . . . . .	-0.3V to Vcc +0.3V

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC CHARACTERISTICS**

(Vcc = +5V ±10%, TA = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Icc1	Current consumption (operating)	DI=0.0V, SK=5.5V Vcc =5.5V, CS = 5.5V DO unloaded			3	mA
Icc2	Current consumption (standby)	Vcc = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
ILI	Input leakage current	VIN = 5.5V			10	µA
ILO	Output leakage current	VOU = 5.5V, CS = 0			10	µA
VIH	High level input voltage		2.0		Vcc +1	V
VIL	Low level input voltage		-0.1		0.8	V
VOH	High level output voltage	I <sub>OH</sub> = -400µA	2.4			V
VOL	Low level output voltage	I <sub>OL</sub> = 2.1mA			0.4	V

**INSTRUCTION SET**

Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A <sub>6</sub> - A <sub>0</sub>	A <sub>5</sub> - A <sub>0</sub>			Read address A <sub>N</sub> - A <sub>0</sub>
PROGRAM	1	X100	A <sub>6</sub> - A <sub>0</sub>	A <sub>5</sub> - A <sub>0</sub>	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Program address A <sub>N</sub> - A <sub>0</sub>
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Write all addresses

**AC CHARACTERISTICS**

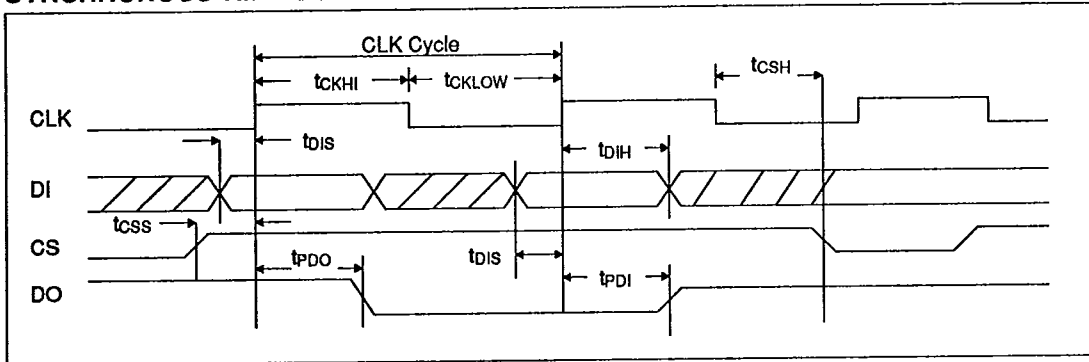
(V<sub>CC</sub> = +5V ±10%, T<sub>A</sub> = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t <sub>CSS</sub>	CS setup time		0.2			μs
t <sub>CSH</sub>	CS hold time		100			ns
t <sub>DIS</sub>	DI setup time	C <sub>L</sub> = 100pF V <sub>OL</sub> = 0.8V, V <sub>OH</sub> = 2.0V V <sub>IL</sub> = 0.45V, V <sub>IH</sub> = 2.4V	0.4			μs
t <sub>DIH</sub>	DI hold time		0.4			μs
t <sub>PD1</sub>	Output delay to 1				2	μs
t <sub>PD0</sub>	Output delay to 0				2	μs
t <sub>EW</sub>	Erase/Write pulse width			10	ms	
t <sub>SKHI</sub>	Minimum SK high time		1			μs
t <sub>SKLOW</sub>	Minimum SK low time		1			μs
CK <sub>MAX</sub>	Maximum clock frequency		DC		250	kHz





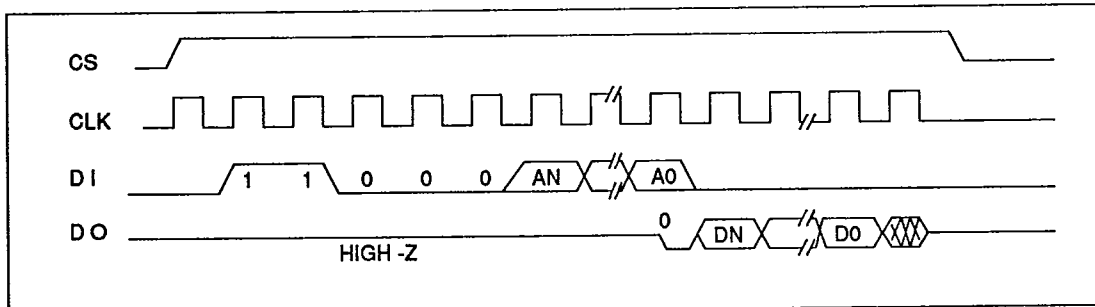
**SYNCHRONOUS TIMINGS**



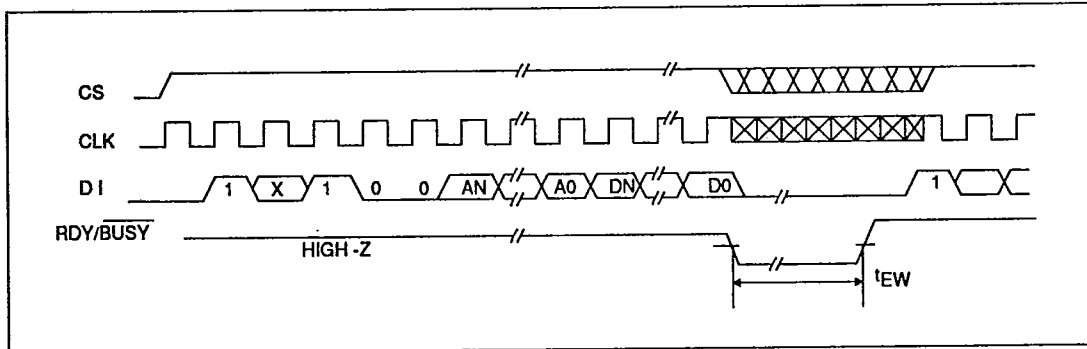
**INSTRUCTION TIMING <ORGANIZATION>**

Organization	$A_N$ (or $AN$ )	$D_N$ (or $DN$ )
128 x 8	$A_6$	$D_7$
64 x 16	$A_5$	$D_{15}$

**INSTRUCTION TIMING <READ>**

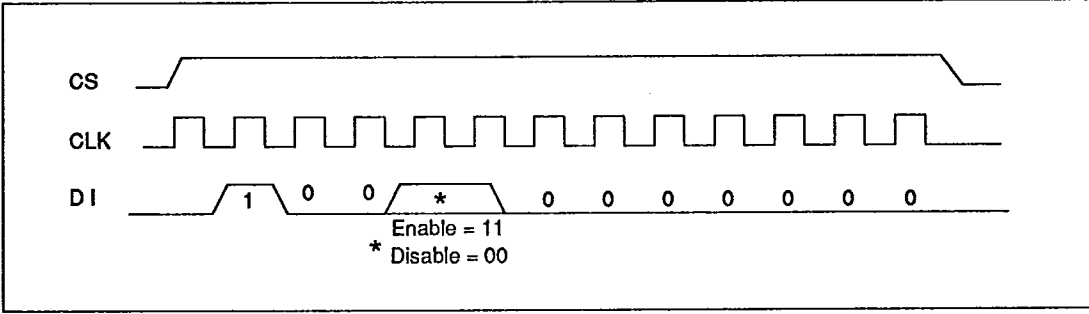


**INSTRUCTION TIMING <PROGRAM>**

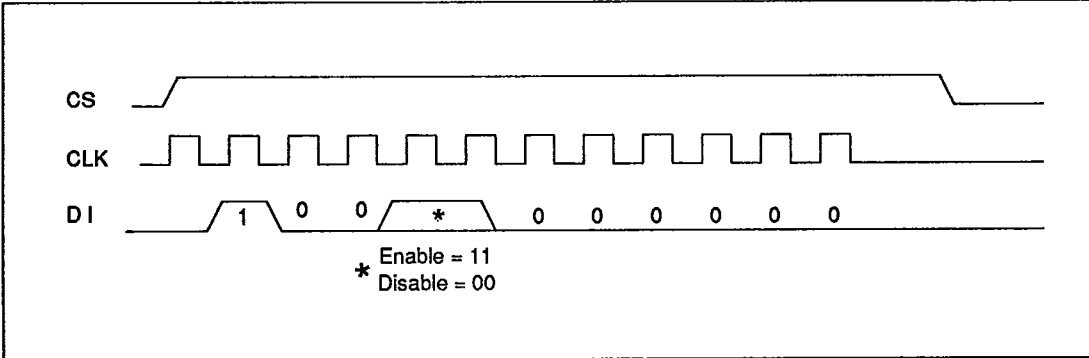




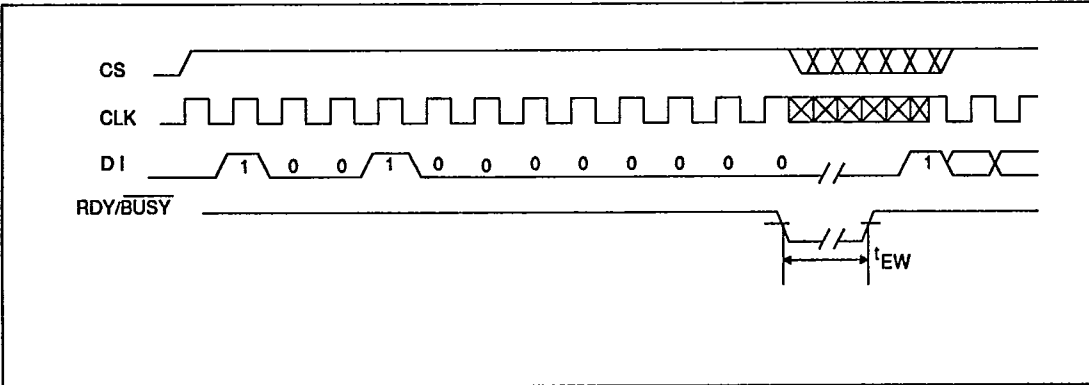
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



INSTRUCTION TIMING <ERAL 128 x 8 organization>







The format for all instructions sent to the CAT59C11A is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

#### READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11A will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay ( $t_{PD1}$  and  $t_{PD0}$ ).

#### ERASE/WRITE ENABLE AND DISABLE

The CAT59C11A powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11A's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the

CAT59C11A regardless of the programming enable/disable status.

#### PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/BUSY pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin.

#### ERASE ALL

Upon receiving an ERAL command, the RDY/BUSY pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin.



#### WRITE ALL

Upon receiving a WRAL command and data, the RDY/BUSY pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin. It IS necessary for all memory locations to be erased before the WRAL command is executed.