14-Bit, 80/105/125/150 MSPS, 1.8 V Dual Analog-to-Digital Converter

Preliminary Technical Data

AD9640

FEATURES

SNR = 71.7 dBc (72.7dBFS) to 70 MHz @ 150 MSPS
SFDR = 85 dBc to 70 MHz @ 150 MSPS
Low Power: 780 mW
1.8V analog supply operation
1.8V to 3.3V CMOS output supply or 1.8V LVDS supply
Integer 1 to 8 Input Clock Divider
IF sampling frequencies to 450 MHz
Internal ADC voltage reference
Integrated ADC sample-and-hold inputs
Flexible analog input: 1 V p-p to 2 V p-p range
Differential analog inputs with 650MHz bandwidth
ADC clock duty cycle stabilizer
95 dB channel isolation/crosstalk
Serial Port Control
User-configurable built-in self-test (BIST) capability
Energy-saving power-down modes
Integrated Receive Features:
- **Fast Detect/Threshold Bits**
- **Composite Signal monitor**

APPLICATIONS

Communications
Diversity radio systems
Multimode digital receivers:
- **GSM, EDGE, PHS, UMTS, WCDMA, CDMA-ONE, IS95, CDMA2000, IMT-2000, WiMax**

I/Q demodulation systems
Smart antenna systems
General-purpose software radios
Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

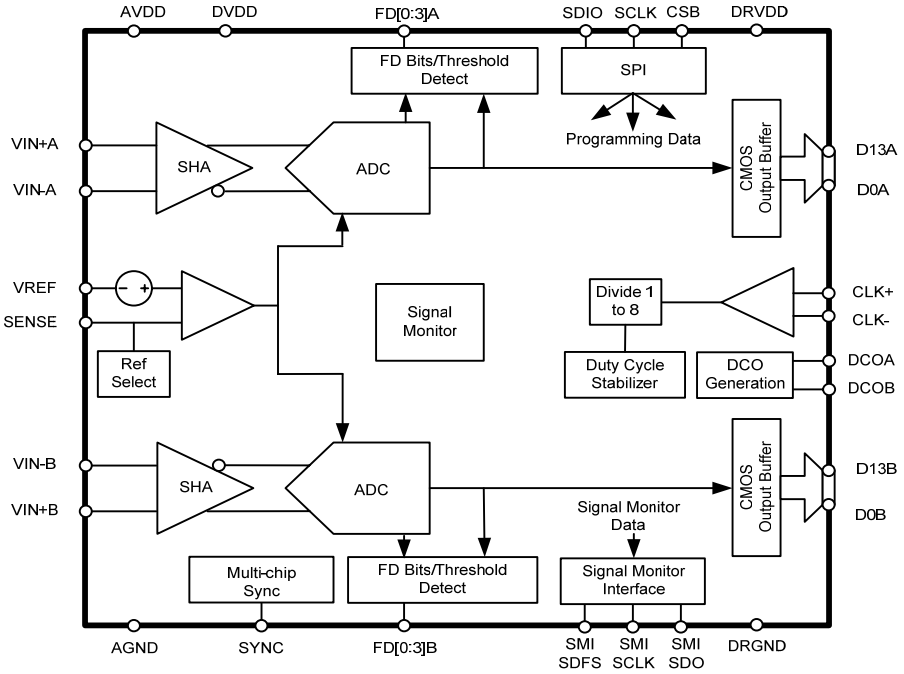


Figure 1. AD9640 Functional Block Diagram

Rev. PrD

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

12/06—Revision PrD:

9/06—Revision PrC:

8/06—Revision PrB: Preliminary Version

GENERAL DESCRIPTION

The AD9640 is a dual 14-Bit 150 MSPS ADC. The AD9640 is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The AD9640 has several functions which simply the AGC function in the system receiver. The fast detect feature allows fast overrange detection by outputting 4 bits of input level information with very short latency. Additionally, the programmable threshold detector allows monitoring of the incoming signal power from the ADC's 4 fast detect bits with very low latency. If the input signal level exceeds the programmable threshold, the decrement gain indicator will go high. Because this threshold is set from the 4 MSB's this allows the user to quickly turn down the system gain to avoid an overrange condition. The second AGC related function is the Signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal which aids in setting the gain to optimize the dynamic range of the overall system.

The ADC output data can be routed directly to the two external 14-bit output ports. These outputs can be set from 1.8V to 3.3V CMOS. Or 1.8V LVDS.

Flexible power-down options allow significant power savings, when desired.

PRODUCT HIGHLIGHTS

- Integrated dual 14-Bit 150 MSPS ADC.
- Fast Over-range Detect and Signal monitor with Serial Output
- Signal monitor block with dedicate serial output mode.
- Proprietary, differential input maintains excellent SNR performance for input frequencies up to 450 MHz.
- The AD9640 operates from a single 1.8 Volt supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
- A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, and voltage reference mode.
- The AD9640 is pin compatible with the AD9627, allowing a simple migration from 12 to 14 Bits.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, Fast Detect Outputs disabled, Signal Monitor disabled, unless otherwise noted.

Table 1.

		AD9640BCPZ-80			AD9640BCPZ-105			AD9640BCPZ-125			AD9640BCPZ-150			Unit
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
RESOLUTION	Full	14			14			14			14			Bits
ACCURACY														
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±TBD		±0.3	±TBD		±0.3	±TBD		±0.3	±TBD	% FSR
Gain Error	Full		±2.0			±2.0			±1.7			±1.7		% FSR
Differential Nonlinearity (DNL)[1]	Full			±TBD			±TBD			±TBD			±TBD	LSB
	25°C		±0.4			±0.4			±0.4			±0.4		LSB
Integral Nonlinearity (INL)	Full			±TBD			±TBD			±TBD			±TBD	LSB
	25°C		±2			±1.8			±2			±2		LSB
TEMPERATURE DRIFT														
Offset Error	Full		±15			±15			±15			±15		ppm/°C
Gain Error	Full		±95			±95			±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE														
Output Voltage Error (1 V Mode)	Full		TBD			TBD			TBD			TBD		mV
Load Regulation @ 1.0 mA	Full		TBD			TBD			TBD			TBD		mV
INPUT REFERRED NOISE														
VREF = 1.0 V	25°C		TBD			TBD			TBD			TBD		LSB rms
ANALOG INPUT														
Input Span, VREF = 1.0 V	Full		2			2			2			2		V p-p
Input Capacitance[2]	Full		8			8			8			8		pF
VREF INPUT RESISTANCE	Full		6			6			6			6		kΩ
POWER SUPPLIES														
Supply Voltage														
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	1.7	3.3	3.6	1.7	3.3	3.6	V
Supply Current														
IAVDD	Full		219			292			363			384		mA
IDVDD	Full		29			37			45			47.5		mA
IDRVDD (3.3V)	Full		30			39			47			53.3		mA
IDRVDD (1.8V)	Full		TBD			TBD			TBD			TBD		mA
PSRR	Full		±0.01			±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION														
DC Input	Full		TBD			TBD			TBD			TBD		mW
Sine Wave Input (DRVDD=1.8V)	Full		TBD			TBD			TBD			TBD		mW
Sine Wave Input (DRVDD=3.3V)	Full		546			721			890			953		mW
Standby Power[3]	Full		TBD			TBD			TBD			TBD		mW
Powerdown Power	Full		TBD			TBD			TBD			TBD		mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure x for the equivalent analog input structure.
[3] Standby power is measured with a dc input, the CLK pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS Enabled, Fast Detect Outputs disabled, Signal Monitor disabled, unless otherwise noted.

Table 2.

		AD9640BCPZ-80			AD9640BCPZ-105			AD9640BCPZ-125			AD9640BCPZ-150			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)														
f_{IN} = 2.4 MHz	25°C		72.0			71.9			71.9			71.9		dB
	Full													dB
f_{IN} = 70 MHz	25°C		71.9			71.9			71.7			71.7		dB
	Full	TBD			TBD			TBD			TBD			dB
f_{IN} = 100 MHz	25°C		71.6			71.6			71.6			71.6		dB
f_{IN} = 170 MHz	25°C		69.9			70.9			70.8			70.8		dB
SIGNAL-TO-NOISE-AND DISTORTION (SINAD)														
f_{IN} = 2.4 MHz	25°C		71.1			71.1			71.1			71.1		dB
	Full													dB
f_{IN} = 70 MHz	25°C		71.5			70.8			70.6			70.6		dB
	Full	TBD			TBD			TBD			TBD			dB
f_{IN} = 100 MHz	25°C		70.5			70.6			70.6			70.6		dB
f_{IN} = 170 MHz	25°C		68.0			69.9			69.8			69.8		dB
EFFECTIVE NUMBER OF BITS (ENOB)														
f_{IN} = 2.4 MHz	25°C		11.7			11.7			11.7			11.7		Bits
f_{IN} = 70 MHz	25°C		11.6			11.6			11.6			11.6		Bits
f_{IN} = 100 MHz	25°C		11.6			11.6			11.6			11.6		Bits
f_{IN} = 170 MHz	25°C		11.5			11.5			11.5			11.5		Bits
WORST SECOND OR THIRD HARMONIC														
f_{IN} = 2.4 MHz	25°C		90			90			90			90		dBc
	Full													dBc
f_{IN} = 70 MHz	25°C		85			85			85			85		dBc
	Full													dBc
f_{IN} = 100 MHz	25°C		85			85			85			83		dBc
f_{IN} = 170 MHz	25°C		84			83.4			83			83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)														
f_{IN} = 2.4 MHz	25°C		90			90			90			90		dBc
	Full													dBc
f_{IN} = 70 MHz	25°C		85			85			85			85		dBc
	Full													dBc
f_{IN} = 100 MHz	25°C		85			85			85			83		dBc
f_{IN} = 170 MHz	25°C		84			83.4			83			80		dBc
TWO TONE SFDR														
f_{IN} = 30 MHz, 31 MHz (−7 dBFS)	25°C		TBD			TBD			TBD			TBD		dBc
f_{IN} = 170 MHz, 171 MHz (−7 dBFS)	25°C		TBD			TBD			TBD			TBD		dBc
CROSSTALK	Full		95			95			95			95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650			650			650		MHz
MATCHING CHARACTERISTIC														
Offset Error	25°C		TBD			TBD			TBD			TBD		%FSR
Gain Error	25°C		TBD			TBD			TBD			TBD		%FSR

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure x for the equivalent analog input structure.
[3] Standby power is measured with a dc input, the CLK pin inactive (set to AVDD or AGND).

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8V, DRVDD = 1.8 V, maximum sample rate, −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	AD9640BCPZ-80			AD9640BCPZ-105			AD9640BCPZ-125			AD9640BCPZ-150			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK-)														
Logic Compliance			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2			1.2			1.2			1.2		V
Differential Input Voltage	Full	0.2		6	0.2		6	0.2		6	0.2		6	Vp-p
Input Voltage Range	Full	AVDD-0.3		AVDD+1.5	AVDD-0.3		AVDD+1.5	AVDD-0.3		AVDD+1.5	AVDD-0.3		AVDD+1.5	V
Input Common-Mode Range	Full	1.1V		AVDD	1.1V		AVDD	1.1V		AVDD	1.1V		AVDD	V
High Level Input Voltage	Full	TBD			TBD			TBD			TBD			V
Low Level Input Voltage	Full			0.8			0.8			0.8			0.8	V
High Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Input Capacitance	Full		TBD			TBD			TBD			TBD		pF
Input Resistance	Full	8	10	12	8	10	12	8	10	12	8	10	12	KΩ
LOGIC INPUTS (CSB, SCLK/DCS, OE, PWDN)														
High Level Input Voltage	Full	TBD			TBD			TBD			TBD			V
Low Level Input Voltage	Full			0.8			0.8			0.8			0.8	V
High Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Input Resistance	Full		TBD			TBD			TBD			TBD		kΩ
Input Capacitance	Full		TBD			TBD			TBD			TBD		pF
LOGIC INPUTS (SDIO/DFS)														
High Level Input Voltage	Full	1.2			1.2			1.2			1.2			V
Low Level Input Voltage	Full			0.8			0.8			0.8			0.8	V
High Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	−10		+10	−10		+10	−10		+10	−10		+10	µA
Input Resistance	Full		TBD			TBD			TBD			TBD		kΩ
Input Capacitance	Full		TBD			TBD			TBD			TBD		pF
DIGITAL OUTPUTS														
DRVDD = 3.3 V														
High Level Output Voltage (I_{OH} = 50 µA)	Full	3.29			3.29			3.29			3.29			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	3.25			3.25			3.25			3.25			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2			0.2			0.2			0.2	V
Low Level Output Voltage (I_{OL} = 50 µA)	Full			0.05			0.05			0.05			0.05	V
DRVDD = 1.8 V														
High Level Output Voltage (I_{OH} = 50 µA)	Full	1.79			1.79			1.79			1.79			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	1.75			1.75			1.75			1.75			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2			0.2			0.2			0.2	V
Low Level Output Voltage (I_{OL} = 50 µA)	Full			0.05			0.05			0.05			0.05	V

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Temp	AD9640BCPZ-80			AD9640BCPZ-105			AD9640BCPZ-125			AD9640BCPZ-150			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CLOCK INPUT PARAMETERS														
Maximum Conversion Rate	Full	80			105			125			150			MSPS
Minimum Conversion Rate	Full			10			10			10			10	MSPS
CLK Period(t_{CLK})	Full	12.5			9.5			8			6.66			ns
CLK Pulse Width High[1] (t_{CLKH})	Full	TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		ns
CLK Pulse Width Low[1] (t_{CLKL})	Full	TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		ns
CLK Pulse Width High[2] (t_{CLKH})	Full	TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		ns
CLK Pulse Width Low(t_{CLKL})	Full	TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		TBD	t_{CLK}/2		ns
DATA OUTPUT PARAMETERS														
Data Propagation Delay (t_{PD})[3]	Full		TBD			TBD			TBD			TBD		ns
DCO Propagation Delay (t_{DCO})	Full		TBD			TBD			TBD			TBD		ns
Setup Time (t_S)	Full		8.5			8.5			8.5			8.5		ns
Hold Time (t_H)	Full		8.5			8.5			8.5			8.5		ns
Pipeline Delay (Latency)	Full		12			12			12			12		Cycles
Aperture Delay (t_A)	Full		TBD			TBD			TBD			TBD		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1			0.1		ps rms
Wake-Up Time[4]	Full		TBD			TBD			TBD			TBD		ms
OUT-OF-RANGE RECOVERY TIME	Full		TBD			TBD			TBD			TBD		

Parameter (Conditions)		Min	Typ	Max	Unit
$\overline{\text{RESET}}$ TIMING REQUIREMENTS					
t_{RESL}	$\overline{\text{RESET}}$ Width Low	TBD			ns
SYNC TIMING REQUIREMENTS					
t_{SS}	SYNC to ↑CLK Setup Time	TBD			ns
t_{HS}	SYNCto ↑CLK Hold Time	TBD			ns
SPI TIMING REQUIREMENTS					
t_{DS}	Set-up time between the data and the rising edge of SCLK	5			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	5			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Set-up time between CSB and SCLK	TBD			ns
t_H	Hold time between CSB and SCLK	TBD			ns
t_{HI}	Minimum period that SCLK should be in a logic high state	TBD			ns
t_{LO}	Minimum period that SCLK should be in a logic low state	TBD			ns

[1] With duty cycle stabilizer (DCS) enabled.
[2] With duty cycle stabilizer (DCS) disabled.
[3] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[4] Wake-up time is dependant on the value of the decoupling capacitors.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD, DVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
VIN+A/B, VIN-A/B to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to +3.9V
D0A/B through D13A/B to DRGND	−0.3 V to DRVDD + 0.3 V
FD0A/B through FD3A/B to DRGND	−0.3 V to DRVDD + 0.3 V
DCOA/B to DRGND	−0.3 V to DRVDD + 0.3 V
VREF to AGND	−0.3 V to AVDD + 0.3 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64 lead LFCSP 9 mm sq. (CP-64-3)	24	TBD	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. LFCSP Parallel CMOS Pin Configuration (Top View)

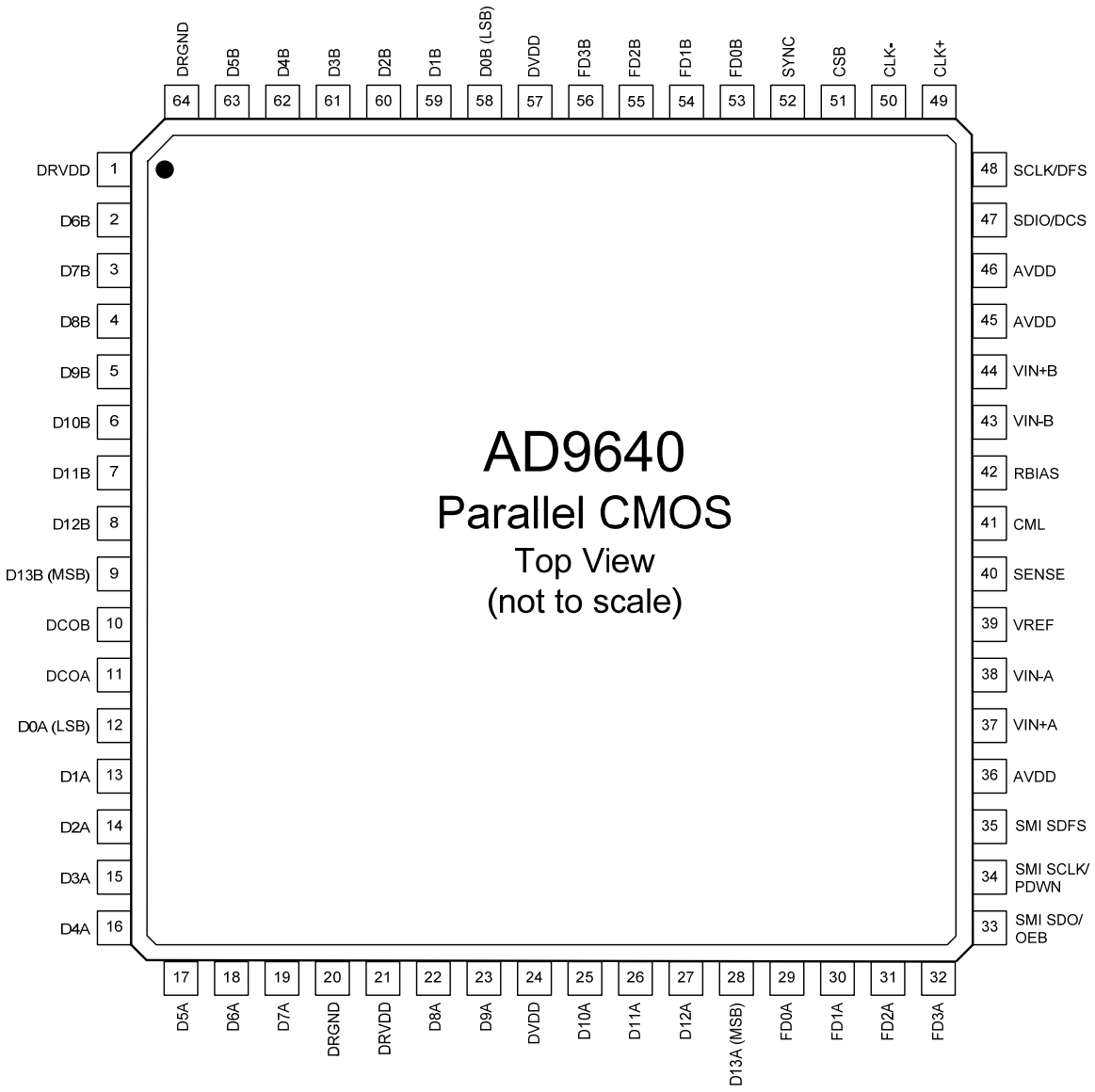
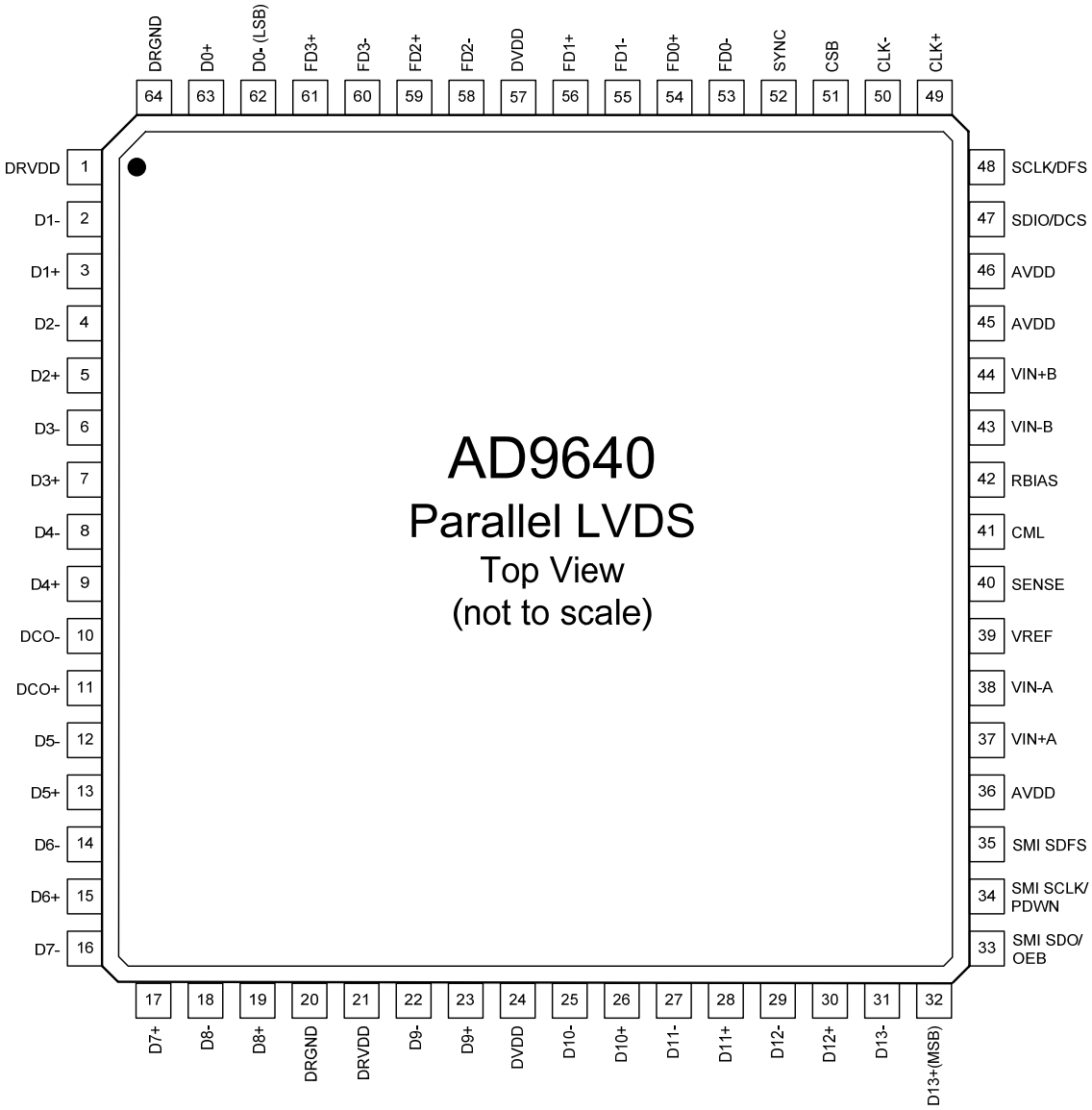


Table 8. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Function
20, 64	DRGND	Gnd	Digital Output Ground
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8V to 3.3V)
24, 57	DVDD	Supply	Digital Power Supply (1.8V Nominal)
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8V Nominal)
0	AGND	Gnd	Analog Ground (Pin 0 is the exposed thermal pad on the bottom of the package)

Pin No.	Mnemonic	Type	Function
ADC INPUTS			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN-A	Input	Differential Analog Input Pin (–) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
39	VREF	I/O	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select (See Table x for details)
42	RBIAS	Input	External Reference Bias Resistor
41	CML	Output	Common Mode Level Bias Output for Analog Inputs
49	CLK+	Input	ADC Master Clock – True (ADC Clock can be driven using single ended CMOS – See Figure x.x for recommended connection)
50	CLK-	Input	ADC Master Clock - Complement (ADC Clock can be driven using single ended CMOS – See Figure x.x for recommended connection)
ADC Fast Detect Outputs			
29	FD0A	Output	Channel A Fast Detect Indicator (See Table x for full detials)
30	FD1A	Output	Channel A Fast Detect Indicator (See Table x for full detials)
31	FD2A	Output	Channel A Fast Detect Indicator (See Table x for full detials)
32	FD3A	Output	Channel A Fast Detect Indicator (See Table x for full detials)
53	FD0B	Output	Channel B Fast Detect Indicator (See Table x for full detials)
54	FD1B	Output	Channel B Fast Detect Indicator (See Table x for full detials)
55	FD2B	Output	Channel B Fast Detect Indicator (See Table x for full detials)
56	FD3B	Output	Channel B Fast Detect Indicator (See Table x for full detials)
Digital INPUTS			
52	SYNC	Input	Digital Synchronization Pin(Slave Mode Only)
Digital OUTPUTS			
12, 13, 14, 15, 16, 17, 18, 19, 22, 23, 25, 26, 27, 28	D0A-D13A	Output	Channel A CMOS output data
58, 59, 60, 61, 62, 63, 2, 3, 4, 5, 6, 7, 8, 9	D0B-D13B	Output	Channel B CMOS output data
11	DCOA	Output	Channel A Data Clock Output
10	DCOB	Output	Channel B Data Clock Output
SPI CONTROL			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode
47	SDIO/DCS	I/O	SPI Serial Data I/O/Duty Cycle Stabilizer in External Pin Mode
51	CSB	Input	SPI Chip Select (Active Low)
Serial Port			
33	SMI SDO/OEB	I/O	Signal monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode
35	SMI SDFS	Output	Signal monitor Serial Data Frame Sync
34	SMI SCLK/PDWN	I/O	Signal monitor Serial Clock Output/Power Down Input in External Pin Mode

Table 9. LFCSP LVDS Pin Configuration (Top View)



EQUIVALENT CIRCUITS

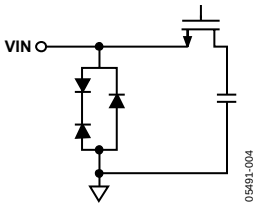


Figure 2. Analog Input Circuit

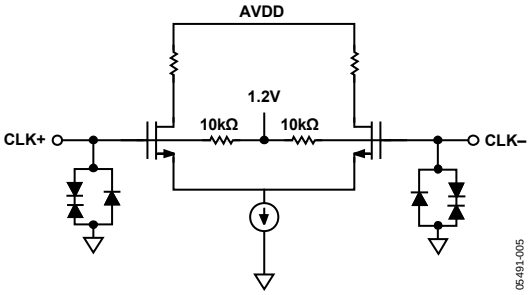


Figure 3. Equivalent Clock lInput Circuit

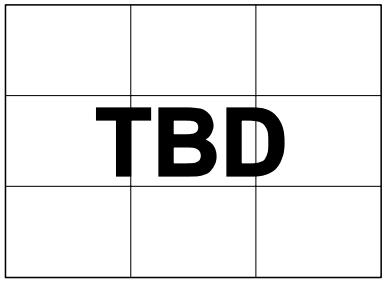


Figure 4. Digital Output

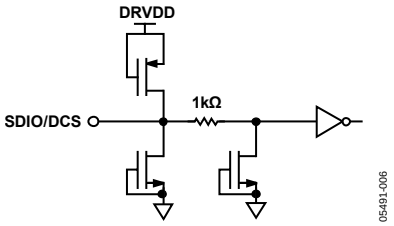


Figure5x. Equivalent SDIO/DCS Input Circuit

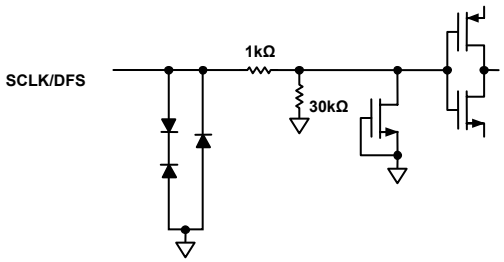


Figure 6. Equivalent SCLK/DFS Input Circuit

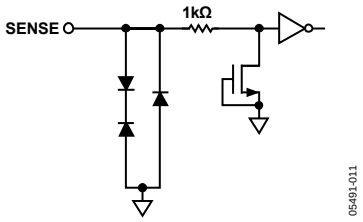


Figure7. Equivalent SENSE Circuit

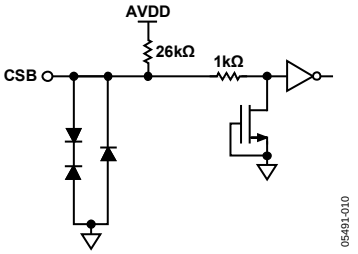


Figure 8. Equivalent CSB Input Circuit

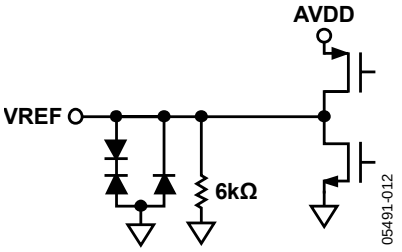


Figure 9. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V; DVDD =1.8V; DRVDD = 1.8 V; Sample Rate = 150 MSPS, DCS enabled, 1 V internal reference; 2 V p-p differential input; VIN = -1.0 dBFS; 64k sample; T_A = 25°C, unless otherwise noted.

TIMING DIAGRAMS

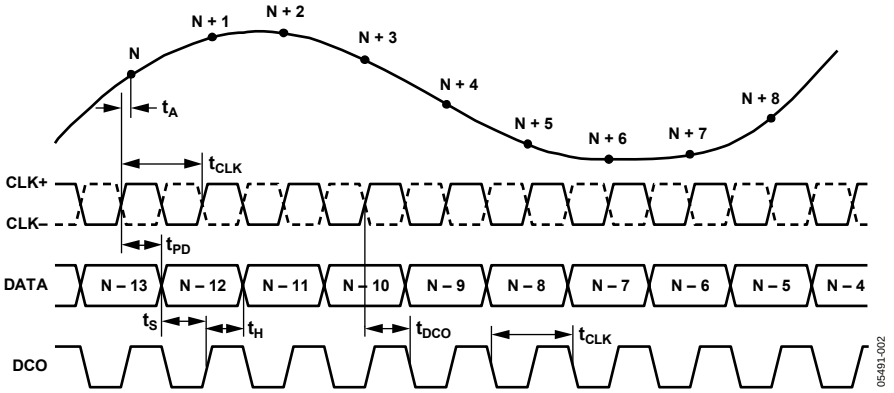


Figure18. Data and Fast Detect Output Timing

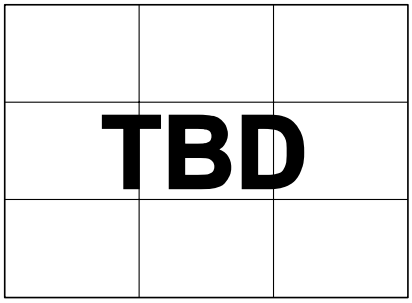


Figure 39. Reset Timing Requirements

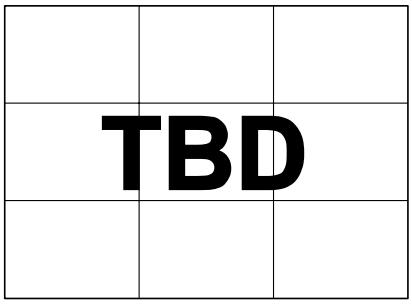


Figure 20. SYNC Input Timing

TERMINOLOGY

Crosstalk
Coupling onto one channel being driven by a (−0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

IF Sampling (Undersampling)
Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Frequencies above Nyquist are aliased and appear in the first Nyquist zone (dc to Sample Rate/2). Care must be taken to limit the bandwidth of the sampled signal so that it does not overlap Nyquist zones and alias onto itself. IF sampling performance is limited by the bandwidth of the input SHA (sample-and-hold amplifier) and clock jitter. (Jitter adds more noise at higher input frequencies.)

Nyquist Sampling (Oversampling)
Oversampling occurs when the frequency components of the analog input signal are below the Nyquist frequency ($F_{clock}/2$), and requires that the analog input frequency be sampled at least two samples per cycle.

Out-of-Range Recovery Time
Out-of-range recovery time is the time it takes for the analog-to-digital converter (ADC) to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components within the programmed DDC filter bandwidth, excluding the first six harmonics and dc. The value for SNR is expressed in decibels (dB).

Two-Tone IMD Rejection
The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.ADC Equivalent Circuits

THEORY OF OPERATION

The AD9640 dual ADC design may be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any fs/2 frequency segment from dc to 100 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 200 MHz analog input is permitted, but at the expense of increased ADC distortion.

In non-diversity applications, the AD9640 can be used as a baseband receiver where one ADC is used for I input data and the other used for Q input data.

Synchronizaton capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD9640 is accomplished using a 3-bit SPI compatible serial interface.

ADC ARCHITECTURE

The AD9640 architecture consists of a dual front-end sample and hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9640 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the SHA between sample mode and hold mode (see x). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependant upon the application.

In IF undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, they would limit the input bandwidth. See the application notes AN-742 and AN-827, and the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" for more information on this subject. In general, the precise values are dependent on the application.

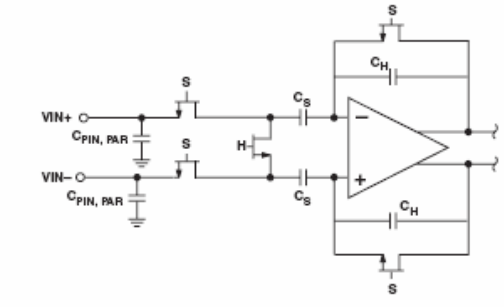


Figure21. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by the buffer to be 2X VREF.

Input Common Mode

The analog inputs of the AD9640 are not internally dc-biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure x). An on-board common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage (typically 0.55 × AVDD).

Differential Input Configurations

Optimum performance is achieved while driving the AD9640 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode

voltage of the AD8352 is easily set with the CML pin of the AD9640 (see Figure 4), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

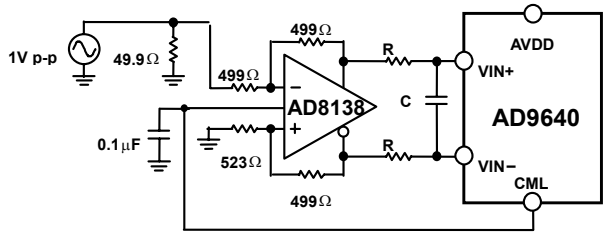


Figure 4. Differential Input Configuration Using the AD8138

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 5. The CML voltage can be connected to the center tap of the transformer's secondary winding to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

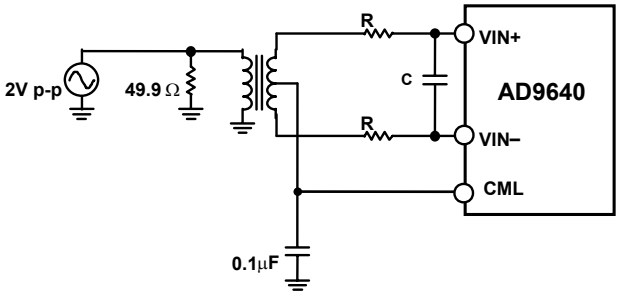


Figure 5. Differential Transformer-Coupled Configuration

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9640. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration. An example is shown in Figure 6.

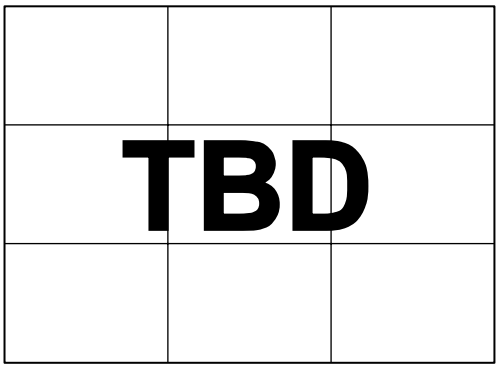


Figure 6. Differential Double Balun Input Configuration

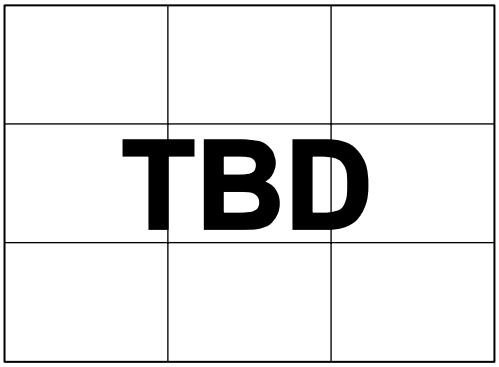


Figure 7. Differential Input Configuration Using the AD8352

An alternative to using a transformer coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 7. See the AD8352 datsheet for more information.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 1 displays recommended values to set the RC network. However, these values will be dependant on the input signal and should only be used as a starting guide.

Table 1 Example RC Network

Frequency Range MHz	R series (Ω, each)	C differential (pF)
0-70	33	15
70-200	33	5
200-300	15	5
>	15	Open

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance.

Figure 8 details a typical single-ended input configuration.

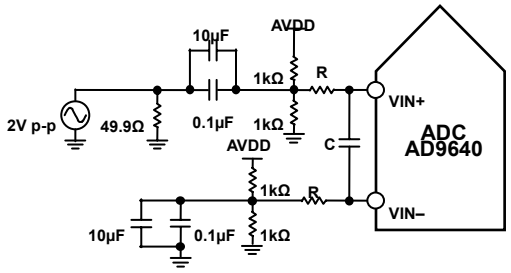


Figure 8. Single-Ended Input Configuration

Table 2. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5\times\left(1+\frac{R2}{R1}\right)$ (See Figure 10)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9640. The input range can be adjusted by varying the reference voltage applied to the AD9640, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in the next few sections. The Reference Decoupling section describes the best practices PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9640 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table x. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 9), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected external to the chip as shown in Figure 10, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$\text{VREF} = 0.5\times\left(1+\frac{\text{R2}}{\text{R1}}\right)$$

The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

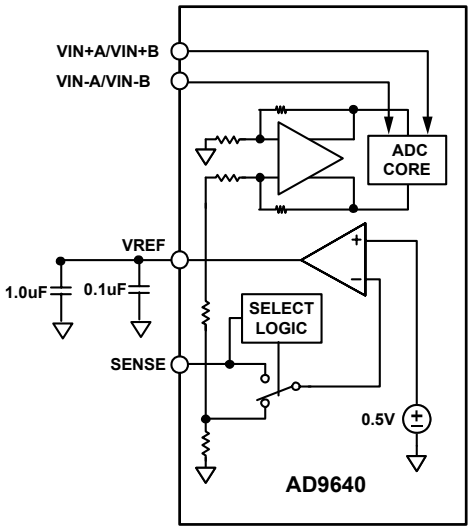


Figure 9. Internal Reference Configuration

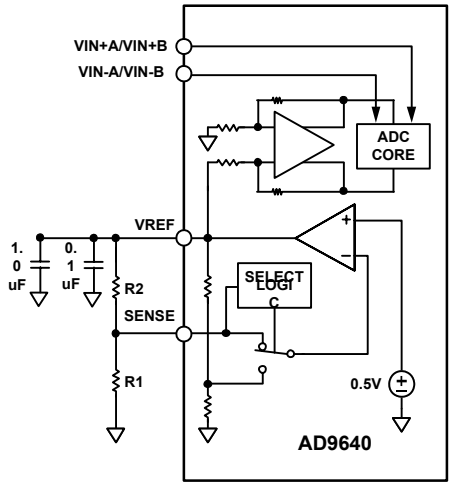


Figure 10. Programmable Reference Configuration

If the internal reference of the AD9640 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 11 depicts how the internal reference voltage is affected by loading.

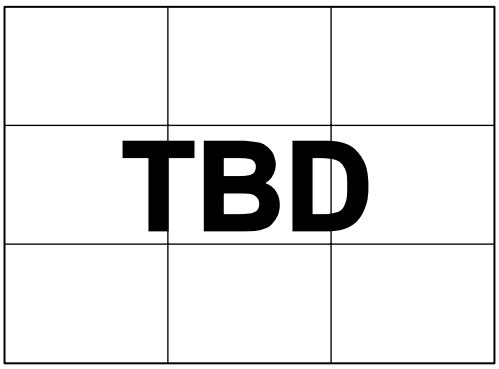


Figure 11. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 12 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

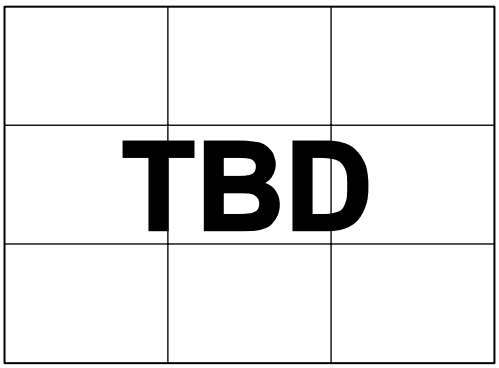
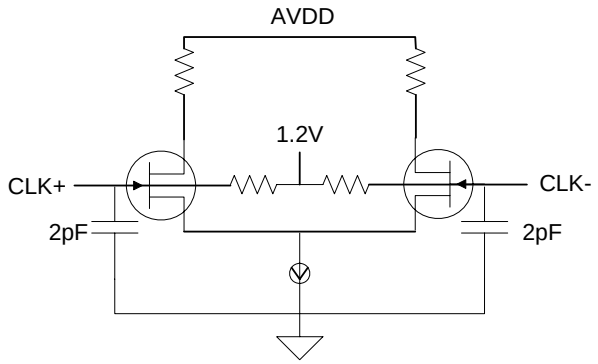


Figure 12. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent TBD kΩ load. The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9640 sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally (See Figure 13) and require no external bias.



Figure

Figure 13.Equivalent Clock Input Circuit

Clock Input Options

The AD9640 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, the jitter of the clock source is of the most concern, as described in the Jitter Considerations section.

Figure 14 shows one preferred method for clocking the AD9640 (at clock rates to 150MSPS). A low jitter clock source is converted from single-ended to differential signal using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9640 to approximately 0.8 Vp-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9640 while preserving the fast rise and fall times of the signal, which are critical to a low jitter performance.

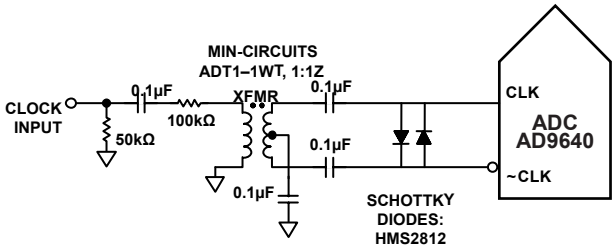


Figure 14. Transformer Coupled Differential Clock(up to 150MSPS)

If a low jitter clock source is not available, another option is to ac-couple a differential PECL signal to the sample clock input pins as shown in Figure 15. The AD9510/AD9511/AD9512/ AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

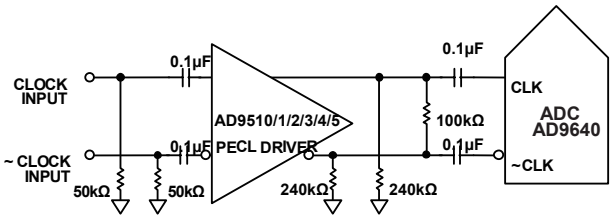


Figure 15. Differential PECL Sample Clock (up to 150MSPS)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins as shown in Figure 16. The AD9510/AD9511/AD9512/ AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.

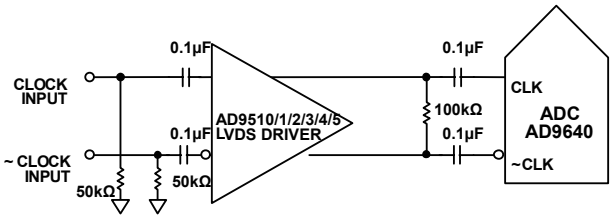


Figure 16 Differential LVDS Sample Clock (up to 150MSPS)

In some applications it may acceptable to drive the sample clock inputs with a single ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, while the CLK- pin should be bypassed to ground with a 0.1uF capacitor in parallel with a 39 kΩ resistor (see Figure 17). CLK+ may be directly driven from a CMOS gate. Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.6V, making the selection of the drive logic voltage very flexible.

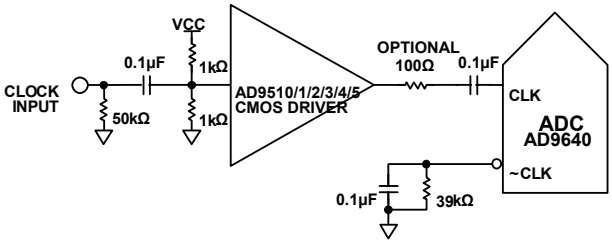


Figure 17. Single-ended 1.8V CMOS Sample Clock (up to 150MSPS)

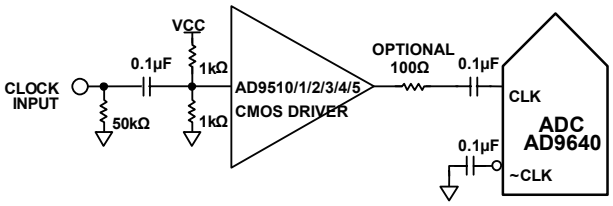


Figure 18 Single-ended 3.3V CMOS Sample Clock (up to 150MSPS)

Input Clock Divider

The AD9640 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. If a divide ratio other than 1 is selected the duty cycle stabilizer will be automatically enabled.

The AD9640 clock divider can be synchronized using the external SYNC input. Register 0x100 bits bits 1 and 2 allow the clock divider to be re-synchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance
characteristics. The AD9640 contains a duty cycle stabilizer (DCS) that retimes the nonsampling, or falling, edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9640. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure x.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately TBD clock cycles to allow the DLL to acquire and lock to the new rate.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{INPUT}) due to jitter (t_J) can be calculated by:

$$SNR = -20\log\left[2\pi f_{INPUT} \times t_J\right]$$

In the equation, the rms aperture jitter represents the root-mean square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as

illustrated in Figure 19.

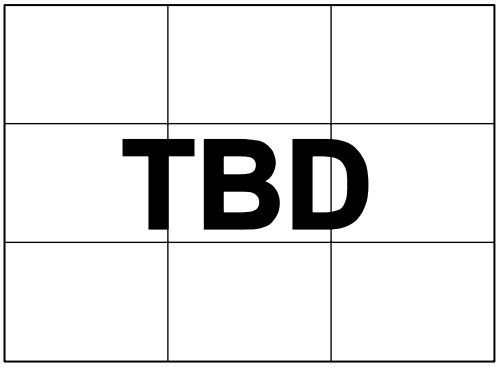


Figure 19. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9640. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs. See www.analog.com.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 20, the power dissipated by the AD9640 is proportional to its sample rate. In CMOS output mode, the digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current (I_{DRVDD}) can be calculated as:

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where *N* is the number of output bits, 14 in the case of the AD9640. This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal. Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 20 was taken with the same operating conditions as the Typical Performance Characteristics with a 5 pF load on each output driver.

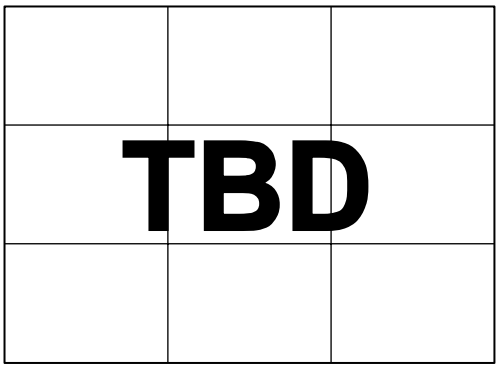


Figure 20. Power vs. Clock Frequency@ 30 MHz

By asserting the PDWN mode (either through the SPI port or by asserting the PDWN pin high), the AD9640 is placed in power-down mode. In this state, the ADC typically dissipates TBD mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9640 to its normal operational mode. This pin is both 1.8V and 3.3V tolerant.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in power-down mode and shorter power-down cycles result in proportionally shorter wake-up times. It takes approximately TBD sec to fully discharge the internal reference buffer decoupling capacitors and TBD ms to restore full operation.

When using the SPI port interface, the user can place the ADC in power-down or standby modes. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the SPI Register Map Description section for more details.

DIGITAL OUTPUTS

The AD9640 output drivers can be configured to interface with 1.8 V to 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic.

In CMOS output mode, the output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

The output data format can be selected for either offset binary or twos complement by setting the CLK/DFS pin when operating in the external pin mode (see Table 3). As detailed in the memory map register description section the data format can be selected for either offset binary, twos complement, or

Gray code when using the SPI control.

Table 3. CLK/DFS Mode Selection (external pin mode)

Voltage at pin	SCLK/DFS	SDIO/DCS
AGND (default)	Binary	DCS Disabled
AVDD	Twos Complement	DCS Enabled

Digital Output Enable Function (OEB)

The AD9640 has a flexible three-state ability for the digital output pins. The three-state mode can be enabled using the OEB pin or through the SPI interface. If the OEB pin is low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. It is not intended for rapid access to the data bus. Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

When using the SPI interface each channel's data and fast detect outputs can be independently three-stated by using the Output Enable Bar bit in register 0x14.

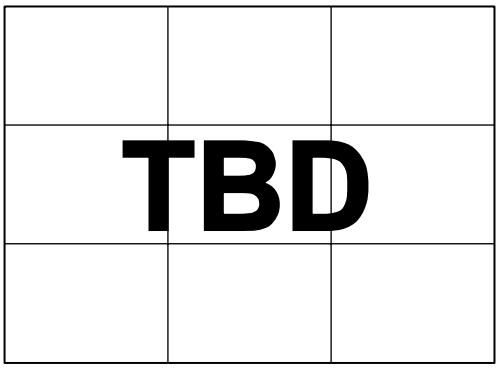


Figure 21. OR Relation to Input Voltage and Output Data

TIMING

The AD9640 provides latched data with a pipeline delay of twelve clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9640. These transients can degrade the converter's dynamic performance. The AD9640 also provides data clock output (DCO) intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO. See Figure x for a graphical timing description.

The lowest typical conversion rate of the AD9640 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

Table 4. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Twos Complement Mode	OR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	1

ADC OVERRANGE AND GAIN CONTROL

It is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides after the fact information which is of limited usefulness. Therefore it is useful to have a programmable threshold below full-scale that would allow time to reduce the gain before the clip actually occurs. In addition, since input signals can have significant slew rates, latency of this function is a big concern. Highly pipelined converters can have significant latency. A good compromise of this function is to use the output bits from the first stage of the ADC for this function. Latency for these output bits is very low, and overall resolution is not highly significant. Peak input signals are typically between full-scale and 6 to 10 dB below full-scale. A 3 or 4 bit output should give more than adequate range and resolution for this function.

Via the SPI port, the user can provide a threshold above which a fast over-range output would be active. As long as the signal is below that threshold, the output should remain low. This pin could also be programmed via the SPI port to function as a traditional over-range pin for customers who currently use this feature. In this mode, all 14 bits of the converter would be examined in the traditional manner and the output would be high for the condition normally defined as overflow. In either mode, the sign of the data is not considered in the calculation of the condition. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

FAST DETECT OVERVIEW

The AD9640 contains circuitry to facilitate fast over-range detection allowing very flexible external gain control implementations. Each ADC has four Fast Detect (FD) bits that are utilized to output information about the current state of the ADC input level. The FD bit function is programmable allowing range information to be output from several points in the internal data path. These bits can also be set up to indicate the presence of overrange or underrange conditions according to programmable threshold levels. Table X.x below shows the 6 configurations available for the Fast Detect bits. These configurations are selecting by setting bits 3:1 in the register at SPI address 0x104.

Table xx. Fast Detect Bit Configuration Settings

Fast Detect Mode Select - Register 104h<3:1>	Information Presented on FD Bits[3:0]
000	ADC Fast Magnitude[3:0]
001	ADC Fast Magnitude[2:0], OVR
010	ADC Fast Magnitude[2:1], OVR, F_LT
011	ADC Fast Magnitude[2:1], C_UT, F_LT
100	OVR, C_UT, F_UT, F_LT
101	OVR, F_UT, IG, DG

ADC FAST MAGNITUDE

When the FD bits are configured to output the ADC fast magnitude the information presented is the ADC level with only a 1 clock cycle latency. Using the FD bits in this configuration provides the earliest possible level indication information. Since this information is provided from early in the data path there is a significant uncertainty in the level indicated. The nominal levels along with the uncertainty indicated by the ADC fast magnitude are shown in table x.x.

Table xx. ADC Fast Magnitude Bits Nomimal Levels (Using Mag[3:0])

ADC_Fast_Mag[3:0]	Nominal Input magnitude in dB below FS	Nominal Input magnitude Uncertainty in dB
0000	-30.14	+12.07 to Min
0001	-18.07	+6.03/-12.07
0010	-12.04	+3.52/-6.03
0011	-8.52	+2.5/-3.52
0100	-6.02	+1.94/-2.5
0101	-4.08	+1.58/-1.94
0110	-2.5	+1.34/-1.58
0111	-1.16	+1.16/-1.34
1000	-0.28	+0.28/-0.88

When fast detect modes 001, 010, or 011 are selected a subset of the FD bits are available. Table xx shows the corresponding ADC input levels when Fast Magnitude[2:0] is selected using 001.

Table xx. ADC Fast Magnitude Bits Nomimal Levels (Using Mag[2:0])

ADC_Fast_Mag[2:0]	Nominal Input magnitude in dB below FS	Nominal Input magnitude Uncertainty in dB
000	-30.14	+12.07 to Min
001	-18.07	+6.03/-12.07
010	-12.04	+3.52/-6.03
011	-8.52	+2.5/-3.52
100	-6.02	+1.94/-2.5
101	-4.08	+1.58/-1.94
110	-2.5	+1.34/-1.58
111	-1.16	+1.16/-1.34

When ADC Fast Magnitude[2:1] is selected the LSB is not provided. The Input ranges for this mode are shown in Table x.

Table xx. ADC Fast Magnitude Bits Nomimal Levels (Using Mag[2:1])

ADC_Fast_Mag[2:1]	Nominal Input magnitude in dB below FS	Nominal Input magnitude Uncertainty in dB
00	-22.14	+10.1 to Min
01	-10.10	+4.08/-7.97
10	-5.00	+2.5/-3.52
11	-1.48	+1.48/-2.6

ADC OVERRANGE (OVR)

The ADC Overrange bit becomes active when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipline and is therefore subject to the TBD ADC clock cycle latency. So an overrange at the input would be indicated by this bit TBD clock cycles after it occurred.

GAIN SWITCHING

The AD9640 includes circuitry that is useful in applications where either large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper and a lower threshold can be programmed. Fast detect modes 2 through 7 support various combinations of the gain switching options.

One such use of this may be to detect when an ADC is about to reach full scale with a particular input condition. The results would be to provide a flag that could be used to quickly insert an attenuator that would prevent ADC overdrive.

Coarse Upper Threshold (C_UT)

The coarse upper threshold bit is asserted if the input level present on the ADC Fast Magnitude bits is greater than the level programmed in the coarse upper threshold register at address 0x105 bits [2:0]. This value is compared with the ADC Fast Magnitude Bits [2:0]. The coarse upper threshold levels are shown in Table x.x. This bit remains asserted for a minimum of 2 ADC clock cycles or until the signal drops below the threshold level.

Table xx. Fast Magnitude Nominal Threshold Levels

Coarse Upper Threshold Register [2:0]	C_UT active when signal magnitude in dB below FS is greater than
000	
001	TBD
010	TBD
011	TBD
100	TBD
101	TBD
110	TBD
111	TBD

Fine Upper Threshold (F_UT)

The Fine Upper Threshold bit will be asserted if the input magnitude exceeds the value programmed in the Fine Upper Threshold Register located at addresses 0x106 and 0x107. This is a 13 bit threshold register that is compared with the magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but allows a finer, more accurate comparison. The fine threshold magnitude is defined by equation x.x.

dBFS = 20 log (threshold mag/2^13)

Fine Lower Threshold (F_LT)

The Fine Lower Threshold bit will be asserted if the input magnitude is less than value programmed in the Fine Lower Threshold Register located at addresses 0x108 and 0x109. The fine lower threshold register is a 13 bit register that is compared with the magnitude at the output of the ADC. This comparison is delayed by the ADC clock latency but provides an accurate comparison. The fine threshold magnitude is defined by equation x.x.

dBFS = 20 log (threshold mag/2^13)

Increment Gain (IG) and Decrement Gain (DG)

The Increment Gain and decrement gain outputs are intended to be used together to provide information to enable external gain control. The Decrement Gain output works identically to the Coarse Upper Threshold output. This bit is asserted when the input magnitude is greater than the three bit value in the Coarse Upper Threshold Register. The Increment Gain output is similar to the Fine Lower Threshold bit except that it will be asserted only if the input magnitude is less than value programmed in the Fine Lower Threshold Register for greater than the 16 bit Dwell Time value located at addresses 0x10A and 0x10B. The dwell time is set in units of ADC input clock cycles ranging from 1 to 65535. The fine lower threshold register is a 13 bit register that is compared with the magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but allows a finer, more accurate comparison. The fine threshold magnitude is defined by equation x.x.

The decrement gain output works off the ADC fast detect bits providing a fast indication of potential overrange conditions. The increment gain uses the comparison at the output of the ADC requiring the input magnitude to remain below an accurate programmable level for a predefined period before signaling external circuitry to increase the gain.

The operation of the increment gain and decrement gain bits is shown in Figure x.x.

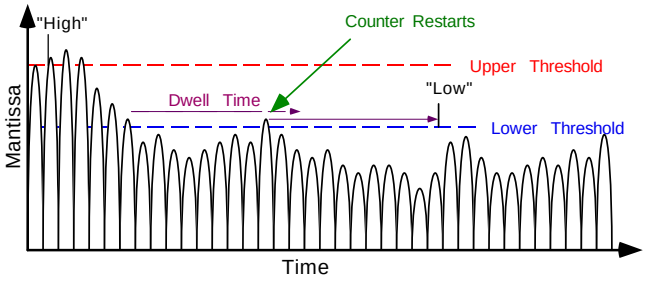


Figure 22. Threshold Settings for IG and DG

SIGNAL MONITOR

The Signal monitoring block serves to characterize the signal being digitized by the ADC. It operates in one to three modes to compute the RMS Input Magnitude, Peak Magnitude, and/or the number of samples that the Magnitude crosses a particular threshold. Together these functions can be used to gain insight into the signal characteristics and can be used to estimate the Peak/Average ratio or even the shape of the CCDF curve (peak to average ratio) of the input signal. This information can be used to drive an AGC loop and to optimize the range of the ADC in the presence of real world signals.

The signal monitor result values can be obtained from the part by either reading back internal registers at addresses 0x116 to 0x11B using the SPI port or by using the signal monitor SPORT output. The output contents of the SPI accessible signal monitor registers is set via the 2 power-monitor mode bits of the signal monitor control register. Both ADC channels must be configured for the same signal monitor mode. Separate SPI accessible 20 bit Signal monitor Value (PMV) output registers are provided for each ADC channel. Any combination of the signal monitor functions can also be output to the user via a serial SPORT interface. These outputs are enabled using the Peak Power Output Enable, RMS Magnitude Output Enable, and Threshold Crossing Output Enable bits in the Signal monitor SPORT Control Register.

For each of the signal monitor measurements a programmable Signal Monitor Period Register (SMPR) controls the duration of the measurement. This time period is programmed as the number of input clock cycles in a 24-bit ADC monitor period register located at addresses 0x113, 0x114, and 0x115. This register can be programmed with a period from 128 samples to 16.78 (2^24) million samples.

Since the DC offset of the ADC can be significantly larger than the signal of interest a simple DC correction circuit is included as part of the signal monitor block to null the DC offset before measuring the power.

PEAK DETECTOR MODE (MODE BITS 01)

The magnitude of the input port signal is monitored over a programmable time period (given by SMPR) to give the peak value detected. This function is enabled by programming a logic 1 in the power-monitor mode bits of the power-monitor control register or by setting the Peak Power Output Enable bit in the Signal monitor SPORT Control Register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer and the countdown is started. The magnitude of the input signal is compared to the internal peak level holding register, and the greater of the two is updated back into the peak level holding register. The initial value of the peak level holding register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13 bit value in the peak level holding register is transferred to a holding register, which can be read through the SPI port or output through the SPORT serial interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is started. Also, the first input sample's magnitude is updated in the peak level holding register, and the comparison and update procedure, as explained above, continues.

Figure 23 is a block diagram of the peak detector logic. The PMV contains the absolute magnitude of the peak detected by the peak detector logic.

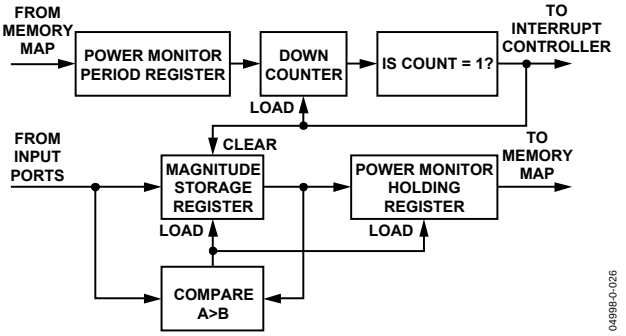


Figure 23. ADC Input Peak Detector Block Diagram

RMS/MS MAGNITUDE MODE (MODE BITS 00)

In this mode, the RMS or MS magnitude of the input port signal is integrated (by adding an accumulator) over a programmable time period (given by SMPR) to give the RMS or MS magnitude of the input signal. This mode is set by programming Logic 0 in the signal monitor mode bits of the signal monitor control register or by setting the RMS Magnitude Output Enable bit in the Signal monitor SPORT Control Register. The 24-bit SMPR, representing the period over which integration is performed, must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started immediately. Each input sample is converted to floating point format and squared. It is then converted to 11 bit fixed point format and is added to the contents of a 24-bit holding register, thus performing an accumulation. The integration continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the square root of the value in the holding register is taken and transferred to the power-monitor holding register (after some formatting), which can be read through the SPI port or output through the

SPORT serial port. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. Also, the first input sample signal power is updated in the holding register, and the accumulation continues with the subsequent input samples. Figure 24 illustrates the RMS magnitude monitoring logic.

For RMS magnitude mode, the value in the PMV is a 20 bit fixed point number. The equation shown below can be used to determine the RMS magnitude in dBFS from the MAG value in the register. Note that if the signal monitor period (SMP) is a power of 2, the 2nd term in the equation goes to zero.

$$\text{RMS\_Magnitude} := 20\cdot\log\left(\frac{\text{MAG}}{2^{20}}\right) - 10\cdot\log\left[\frac{\text{SMP}}{2^{\text{ceil}\left[\log_2(\text{SMP})\right]}}\right]$$

For MS magnitude mode, the value in the PMV is a 20 bit fixed point number. The equation shown below can be used to determine the MS magnitude in dBFS from the MAG value in the register. Note that if the signal monitor period (SMP) is a power of 2, the 2nd term in the equation goes to zero.

$$\text{MS\_Magnitude} := 10\cdot\log\left(\frac{\text{MAG}}{2^{20}}\right) - 10\cdot\log\left[\frac{\text{SMP}}{2^{\text{ceil}\left[\log_2(\text{SMP})\right]}}\right]$$

TBD

Figure 24. ADC Input RMS Magnitude Monitoring Block Diagram

THRESHOLD CROSSING MODE (MODE BITS 1X)

In this mode of operation, the magnitude of the input port signal is monitored over a programmable time period (given by SMPR) to count the number of times it crosses a certain programmable threshold value. This mode is set by programming Logic 1x (where x is a don't care bit) in the power-monitor mode bits of the signal monitor control register or by setting the Threshold Crossing Output Enable bit in the Signal monitor SPORT Control Register. Before activating this mode, the user needs to program the 24-bit SMPR and the 13-bit upper threshold register for each individual input port. The same upper threshold register is used for both signal monitoring and gain control (see the ADC Overrange and Gain Control section).

After entering this mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started. The magnitude of the input signal is compared to the upper threshold register (programmed previously) on each input clock cycle. If the input signal has magnitude greater than the upper threshold register, then the internal count register is incremented by 1. The initial value of the internal count register is set to 0. This comparison and increment of the internal count register continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the internal count register is transferred to the signal monitor holding register, which can be read through the SPI port or output through the SPORT serial port. The monitor period timer is reloaded with the value in the SMPR, and the countdown is started. The internal count register is also cleared to a value of 0. Figure 25 illustrates the threshold crossing logic. The value in the PMV is the number of samples that have a magnitude greater than the threshold register.

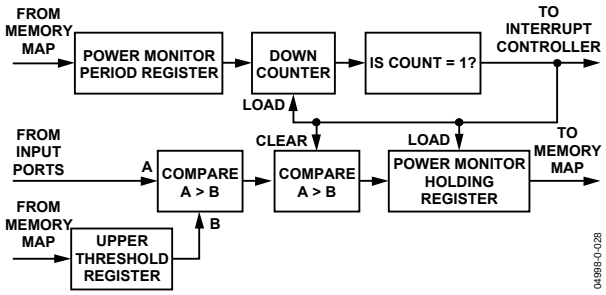


Figure 25. ADC Input Threshold Crossing Block Diagram

ADDITIONAL CONTROL BITS

For additional flexibility in the signal monitoring process, two control bits are provided in the power-monitor control register. They are the signal monitor enable bit and the complex power bit.

Signal monitor Enable Bit

The signal monitor enable bit located in bit 0 or register 0x112 enables operation of the signal monitor block. If the signal monitor function is not needed in a particular application then this bit should be cleared to conserver power.

Measure Complex Power Bit

When this bit is set the part assumes that Channel A is digitizing the I data and Channel B is digitizing the Q data for a complex input signal (or vice versa). In this mode the power reported is the sqrt(I^2 + Q^2). This complex power measurement result is presented in the Channel A signal monitor value register if the signal monitor mode bits are set to 00. The channel B signal monitor will continue to compute the channel B value.

DC CORRECTION

Since the DC offset of the ADC can be significantly larger than the signal we are trying to measure a simple DC correction circuit is included to null the DC offset before measuring the power. The DC Correction circuit can also be switched into the main signal path but this may not be appropriate if the ADC is digitizing a time-varying signal with significant DC content such as GSM.

DC Correction Bandwidth

The DC correction circuit is basically a HP filter with a programmable BW ranging between 0.15Hz and 1.2kHz. The BW is controlled by writing the 4-bit DC correction register located in bits 5:2 at address 0x10C. Table xx shows the BW values for each of the 16 possible programmed values.

Table xx. DC Correction Bandwidth Settings

DC Correction Factor reg.10C<5:2>	Bandwidth (Hz)
0000	1218.56
0001	609.28
0010	304.64
0011	152.32
0100	76.16
0101	38.08
0110	19.04
0111	9.52
1000	4.76
1001	2.38
1010	1.19
1011	0.60
1100	0.30
1101	0.15
1110	0.15
1111	0.15

DC Correction Readback

The current DC correction value can be read back in registers 0x10D and 0x10E for channel A and registers 0x10F and 0x110 for channel B. The DC correction value is a 14 bit value that can span the entire input range of the ADC.

DC Correction Freeze

Setting the DC Correction Freeze bits freezes the DC correction at its current state and continues to use the last updated value as the DC correction value. Clearing this bit restarts the DC correction and adds the currently calculated value to the data.

DC Correction Enable Bits

Setting bit 0 of register 0x10C enables the DC correction for use in the Signal monitor calculations. The calculated DC correction value can be added to the output data signal path by setting bit 1 of register 0x10C.

SIGNAL MONITOR SPORT OUTPUT

The SPORT is a serial interface with three output pins, the SMI SCLK (SPORT clock), SMI_SDFS (SPORT frame sync) and SMI_SDO (SPORT data). The SPORT is the master, and drives all three pins out of the chip.

SMI SCLK

The data and frame sync are driven on the positive edge of the SMI SCLK. The SMI SCLK has three possible baud rates. They are ½, ¼, or 1/8 the ADC clock rate, based on the SPORT controls. The SMI SCLK can also be gated off when not sending any data, based on the SMI SCLK sleep bit. Gating off the SMI SCLK when it is not needed will reduce the coupling errors back into the signal path if these prove to be a problem in the system. This has the disadvantage of spreading the frequency content of the clock so this can be left running to ease frequency planning if desired.

SMI SDFS

The SMI_SDFS is the Serial Data Frame Sync, and defines the start of a frame. One SPORT frame includes data from both datapaths. The data from Datapath A is sent just after the frame sync, followed by data from Datapath B.

SMI SDO

The SMI_SDO is the serial data out of the block. The data is sent MSB first on the next positive edge after the SMI_SDFS. Each data output block includes one or more of RMS magnitude, Peak level, and Threshold Crossing values from both datapaths in the stated order. If enabled the data is sent RMS first, followed by Peak, and Threshold as shown in Figure x.

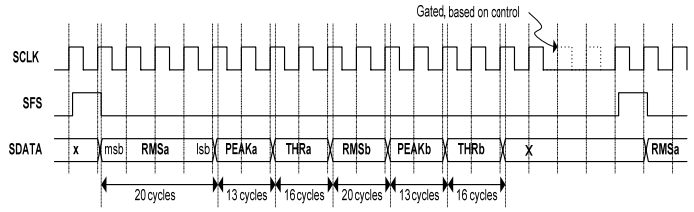


Figure 26. Signal monitor SPORT Output Timing (RMS, Peak, and Threshold Enabled)

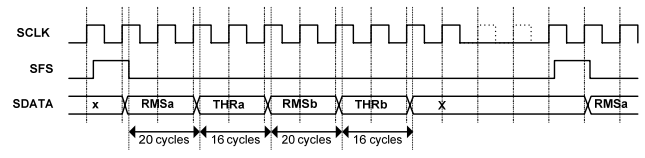


Figure 27. Signal monitor SPORT Output Timing (RMS and Threshold Enabled)

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9640 includes built-in test features to enable verification of the integrity of each channel as well as to facilitate board level debugging. A BIST (built-in self-test) feature is included which verifies the integrity of the digital data path of the AD9640. Various output test options are also provided to place predictable values on the outputs of the AD9640.

BUILT IN SELF TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9640 signal path. When enabled, the test runs from a user selectable internal source (PN or sine) through the digital data path starting at the ADC block output. The BIST sequence will run for 256 cycles and stop. The BIST signature value for channel A or B will be placed in registers 0x024 and 0x025. If one channel is chosen, its BIST signature is written to the two registers. If both channels are chosen, the two channels' results are XOR'ed and placed in the BIST signature register. The outputs are not disconnected during this test, so the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or start from the beginning based on the value programmed in register 0x00E bit 2. The BIST signature result will vary based on the channel configuration.

OUTPUT TEST MODES

The output test options are shown in table x.x. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital backend blocks and the test pattern is run through the output formatting block. As indicated in table x.x some of the test patterns are subject to output formatting and some are not. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting bits 4 or 5 of register 0x0D. These tests can be performed with or without an analog signal, but do require an encode clock.

CHANNEL/CHIP SYNCHRONIZATION

The AD9640 has a SYNC input that allows the user flexible synchronization options for syncing the internal blocks. The sync feature is useful to guarantee synchronized operation across multiple ADCs. The input clock divider and the signal monitor block can be synchronized using the SYNC input. The input clock divider can be enabled to sync on a single occurrence of the sync signal or on every occurrence. The signal monitor syncs on every SYNC input.

The SYNC input is internally synchronized to the sample clock, however to ensure there is no timing uncertainty between multiple parts the SYNC input signal should be synchronized to the input clock signal. The SYNC input should be driven using a single ended CMOS type signal.

SERIAL PORT INTERFACE (SPI)

The AD9640 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This gives the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and may be written to or read from via the port. Memory is organized into bytes that can be further divided down into fields, which are documented in the Memory Map section. Detailed operational information can be found in the Analog Devices user manual titled *Interfacing to High Speed ADCs via SPI* at www.analog.com.

CONFIGURATION USING THE SPI

There are three pins that define the SPI of this ADC. They are the SCLK/DFS, SDIO/DCS, and CSB pins (summarized inTable x). The SCLK/DFS (serial clock) is used to synchronize the read and write data presented from/to the ADC. The SDIO/DCS (serial data input/output) is a dual purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) is an active low control that enables or disables the read and write cycles.

Table xx. Serial Port Interface Pins

Pin	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is active low controls that gates the read and write cycles.

The falling edge of the CSB in conjunction with the rising edge of the SCLK determines the start of the framing. An example of the serial timing and its definitions can be found in Figure x and Table x.

Other modes involving the CSB are available. The CSB can be held low indefinitely which permanently enabling the device, this is called streaming. The CSB may stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance more. This mode turns on any SPI pin secondary functions.

During an instruction phase a 16bit instruction is transmitted. Data follows the instruction phase and it's length is determined by the W0 and W1 bits. All data is composed of 8bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used both to program the chip as well as read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/ output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data may be sent in MSB or in LSB first mode. MSB first is default on power up and may be changed via the configuration register. For more information about this and other features see *"Interfacing to High Speed ADCs via SPI"* at www.analog.com.

Table xx. SPI Timing Diagram Specifications

Spec Name	Meaning
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between CSB and SCLK
t_H	Hold time between CSB and SCLK
t_{HI}	Minimum period that SCLK should be in a logic high state
t_{LO}	Minimum period that SCLK should be in a logic low state

HARDWARE INTERFACE

The pins described in Table x**Error! Reference source not found.** comprise the physical interface between the user's programming device and the serial port of the AD9640. All serial pins are inputs, which should be tied to an external pull-up or pull-down resistor (suggested value 10 kΩ).

The SPI interface is flexible enough to be controlled by either FPGAs or mirocontrollers. This provides the user the ability use an alternate method to program the ADC other than a dedicated SPI controller.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Since the SCLK, CSB and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade the converter's performance. If the on board SPI Bus is utilized for other devices it may be necessary to provide buffers between this bus and the AD9640 in order to keep these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to AVDD or ground during device power on, they are associated with a specific function. The TBD section describes the strappable functions supported on the AD9640.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS, SCLK/DFS, MON SDO/OEB, and MON SCLK/PDWN pins serve as stand alone CMOS compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, output enable, and power down feature control. In this mode the CSB chip select should be connected to AVDD, which will disable the serial port interface.

Table 5. Mode Selection

Pin	External Voltage	Configuration
SDIO/DCS	AVDD (default)	Duty Cycle Stabilizer Enabled
	AGND	Duty Cycle Stabilizer Disabled
SCLK/DFS	AVDD	Twos Complement Enabled
	AGND (default)	Offset Binary Enabled
MON SDO/ OEB	AVDD	Outputs in High Impedance
	AGND (default)	Outputs Enabled
MON SCLK/ PDWN	AVDD	Chip in PowerDown/Standby
	AGND (default)	Normal Operation

MEMORY MAP

Reading the Memory Map Table

Each row in the memory map table has eight bit locations. The memory map is roughly divided into four sections: chip configuration and ID register map (Address 0x00 to Address 0x05), ADC setup, control and test (Addresses 0x08 to Address 0x25), transfer register map (Address 0xFF), and digital feature control (Address 0x100 to Address 0x11B).

Starting from the right hand column, the memory map register in Table x documents the default hex value for each hex address shown. The column with the heading Bit 7 (MSB) is the start of the default hex value given. For example, hex address 0x18, reference select, has a hex default value of 0xC0. This means Bit 7 = 1, Bit 6 = 1, and the remaining bits are zeros. This setting is the default reference selection setting. The default value uses a 2.0V peak to peak reference. For more information on this function and others consult *"Interfacing to High Speed ADCs via SPI"* at www.analog.com.

Open Locations

All address and bit locations that are not included in Table x are currently not supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), then this address location should not be written.

Default Values

Coming out of reset, critical registers are loaded with default values. The default values for the registers are given in the Memory Map Table.

Logic Levels

An explanation of various registers follows: "bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit." Similarly "clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Addresses 0x08 to 0x18 are shadowed. Writes to these addresses do not affect the part operation until a transfer command is issued by writing a 0x01 to address 0xFF setting the transfer bit. This allows these registers to be updated internally simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set and the bit autoclears.

Channel Specific Registers

Some channel setup functions such as the signal monitor thresholds can be programmed differently for each channel. In these cases channel address locations are internally duplicated for each channel. These registers are designated in the 'Parameter Name' column of Table x as (local) registers. These local registers can be accessed by setting the appropriate Channel A or Channel B bits in register 0x05. If both bits are set the subsequent write will affect both channels' registers. In a read cycle only Channel A or Channel B should be set to read one of the two registers. If both bits are set during a SPI read cycle the part returns the value for channel A. Registers designated as (global) in the 'Parameter Name' column of Table x affect the entire part or the channel features where independent settings are not allowed between the channels. The settings in register 0x05 do not affect the global registers.

SPI ACCESSIBLE FEATURES

A brief description of all features accessible via the SPI follows. They are described in great detail in the Analog Devices user manual titled *Interfacing to High Speed ADCs via SPI* at www.analog.com.

Modes: Allows the user to set either power-down or standby mode.

Clock: Allows the user to access the DCS via the SPI.

Offset: Allows the user to digitally adjust the converter offset.

Test IO: Allows the user to set test modes to have known data on output bits.

Output Mode: Allows the user to setup outputs.

Output phase: Allows user to set the output clock polarity.

Output Delay: Allows user to vary the strength of the output drivers.

Vref: Allows the user to set the reference voltage.

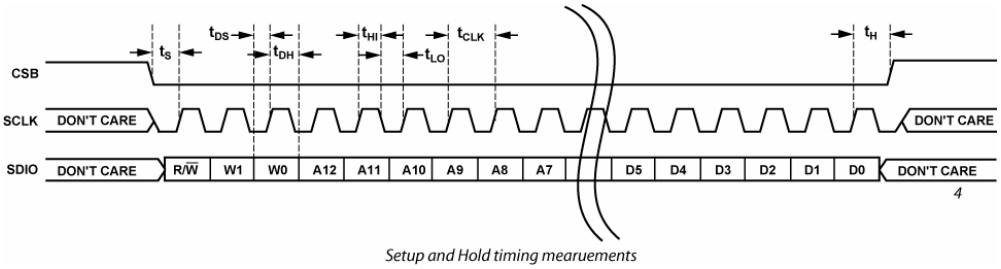


Figure 28. Serial Port Interface Timing Diagram

EXTERNAL MEMORY MAP

Table 6. Memory Map Register

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
00	SPI Port Configuration (global)	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles should be mirrored so that LSB- or MSB-first mode register correctly regardless of shift mode.
01	Chip ID (global)	8-bit Chip ID Bits 7:0 (AD9640 = 0x11), (default)								0x0F Read Only	Default is unique chip ID, different for each device. This is a read-only register.
02	Chip Grade (global)	X	X	Speed Grade ID 4:3 00 = 80 MSPS 01 = 105 MSPS 10 = 125 MSPS 11 = 150 MSPS		X	X	X	X	Read only	Speed Grade ID used to differentiate devices.
Channel Index and Transfer Registers											
05	Channel Index	X	X	X	X	X	X	Data Channel B (default)	Data Channel A (default)	0x03	Bits are set to determine which device on chip receives the next write command. Applies to local registers
FF	Device Update	X	X	X	X	X	X	X	Transfer	0x00	Synchronousl transfers data from the master shift register to the slave.
ADC Functions											
08	Power modes	X	X	External Power Down Pin Function (global) 0 = pdwn 1 = stndby	X	X		Internal power-down mode (local) 00—normal operation 01—full power-down 10—standby 11—normal operation		0x00	Determines various generic modes of chip operation.
09	Global clock (global)	X	X	X	X	X	X	X	Duty cycle stabilize (default)	0x01	
0B	Clock divide (global)	X	X	X	X	X	Clock Divide Ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically causes the Duty Cycle Stabilization to become active

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0D	Test Mode (local)	X	X	Reset PN23 gen	Reset PN9 gen	X	Output test mode 000—off (default) 001—midscale short 010—+positive FS 011—−negative FS 100—alternating checker board 101—PN 23 sequence 110—PN 9 sequence 111—one/zero word toggle			0x00	When set, the test data is placed on the output pins in place of normal data.
0E	Bist enable (local)	X	X	X	X	X	Reset BIST Sequence	X	BIST Enable	0x00	
10	Offset adjust (local)	X	X	Offset Adjust in LSBs from +31 to -32 (twos compliment format)						0x00	
14	Output Mode	Drive Strength 0—3.3V CMOS or ANSI LVDS 1—1.8V CMOS or Reduced LVDS (global)	Output Type 0 = CMOS 1 = LVDS (global)	Interleaved CMOS (global)	Output Enable Bar (local)	X	Output invert (local)	00—offset binary 01—twos complement 01—greycode 11—offset binary (local)		0x00	Configures the outputs and the format of the data.
15	Output Adjust (global)	X	X	X	X	CMOS 3.3V Drive Strength (00 is lowest drive and 11 is highest drive)		CMOS 1.8 V Drive Strength (00 is lowest drive and 11 is highest drive)		0x02	Determines CMOS output drive strength – Selecting higher drive strengths can affect converter performance
16	Clock Phase Control (global)	Invert DCO Clock	X	X	X	X	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles			0x00	On devices that utilize global clock divide, allows selection of clock delays into the dividerb.
18	Vref Select (global)	Reference Voltage Selection 00 = 1.25V pk-pk 01 = 1.5V pk-pk 10 = 1.75V pk-pk 11 = 2.0V pk-pk (default)		X	X	X	X	X	X	0x30	
24	BIST Signature lsb (local)	BIST Signature [7:0]								0x00	Read Only
25	BIST Signature msb (local)	BIST Signature [15:8]								0x00	Read Only
100	Synch_Control (global)	PM Sync Enable	X	X	X	X	Clock Divider Next Sync Only	Clock Divider Sync Enable	Master Sync Enable	0x00	
104	Fast Detect Control (local)	X	X	X	X	Fast Detect Mode Select [2:0]			Enable Fast Detect	0x00	
105	Coarse Upper Threshold (local)	X	X	X	X	X	Coarse Upper Threshold [2:0]			0x00	

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
106	Fine Upper Threshold Register 0 (local)	Fine Upper Threshold [7:0]								0x00	
107	Fine Upper Threshold Register 1 (local)	X	X	X	Fine Upper Threshold [12:8]					0x00	
108	Fine Lower Threshold Register 0 (local)	Fine Lower Threshold [7:0]								0x00	
109	Fine Lower Threshold Register 1 (local)	X	X	X	Fine Lower Threshold [12:8]					0x00	
10A	Increase Gain Dwell Time Register 0 (local)	IncreaseGain Dwell Time [7:0]								0x00	In ADC Clock Cycles
10B	Increase Gain Dwell Time Register 1 (local)	IncreaseGain Dwell Time [15:8]								0x00	In ADC Clock Cycles
10C	Signal monitor DC Correction Control (global)	X	DC Correction Freeze	DC Correction Bandwidth [3:0]				DC Correction for Signal Path Enable	DC Correction for PM Enable	0x00	
10D	Signal monitor DC Value Channel A Register 0 (global)	DC Value Channel A [7:0]									Read only
10E	Signal monitor DC Value Channel A Register 1 (global)	X	X	DC Value Channel A [13:8]							Read only
10F	Signal monitor DC Value Channel B Register 0 (global)	DC Value Channel B [7:0]									Read only
110	Signal monitor DC Value Channel B Register 1 (global)			DC Value Channel A [13:8]							Read only
111	Signal monitor SPORT Control (global)	X	RMS Magnitude Output Enable	Peak Power Output Enable	Threshold Crossing Output Enble	SPORT Clock Divide 00 = Undefined 01 = divide by 2 10 = divide by 4 11 = divide by 8		SPORT SCLK Sleep	SPORT Enable	0x04	
112	Signal monitor Control (global)	Enable Complex Power Calculation Mode	X	X	X	MS Mode 0 = RMS 1 = MS	Signal monitor Mode 00 = RMS/MS Magnitude 01 = Peak Power 1x = Threshold Count		Signal monitor Enable	0x00	
113	Signal monitor Period Register 0 (global)	Signal monitor Period [7:0]								0x80	In ADC Clock Cycles
114	Signal monitor Period Register 1 (global)	Signal monitor Period [15:8]								0x00	In ADC Clock Cycles
115	Signal monitor Period Register 2 (global)	Signal monitor Period [23:16]								0x00	In ADC Clock Cycles
116	Signal monitor	Signal monitor Value Channel A [7:0]									Read only

Addr. (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
	Value Channel A Register 0 (global)										
117	Signal monitor Value Channel A Register 1 (global)	Signal monitor Value Channel A [15:8]									Read only
118	Signal monitor Value Channel A Register 2 (global)	X	X	X	X	Signal monitor Value Channel A [19:16]					Read only
119	Signal monitor Value Channel B Register 0 (global)	Signal monitor Value Channel B [7:0]									Read only
11A	Signal monitor Value Channel B Register 1 (global)	Signal monitor Value Channel B [15:8]									Read only
11B	Signal monitor Value Channel B Register 2 (global)	X	X	X	X	Signal monitor Value Channel B [19:16]					Read only

MEMORY MAP REGISTER DESCRIPTION

APPLICATIONS

DESIGN GUIDELINES

When designing the AD9640 into a system, it is recommended that, before starting design and layout, the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements required for certain pins.

Power and Ground Recommendations

When connecting power to the AD9640, it is recommended that two separate 1.8 V supplies be used: one supply should be used for analog (AVDD) and digital (DVDD) and a separate supply for the digital outputs (DRVDD). The AVDD and DVDD supplies, while derived from the same source, should be isolated with a ferrite bead or filter choke and separate decoupling capacitors. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the part's pins with minimal trace length.

A single PC board ground plane should be sufficient when using the AD9640. With proper decoupling and smart partitioning of the PC board's analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC is connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9640. A continuous exposed (no solder mask) copper plane on the PCB should mate to the AD9640 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions only guarantees one tie point between the ADC and PCB. See the evaluation board for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, "A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)," at www.analog.com.

CML

The CML pin should be decoupled to ground with a 0.1uF capacitor, as shown in Figure 5.

RBIAS

The AD9640 requires the user to place a 10KΩ resistor between the RBIAS pin and ground. This resister sets the master current reference of the ADC core and should have at least a 1% tolerance.

Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR 1.0uF capacitor in parallel with a 0.1uF ceramic low ESR capacitor.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Since the SCLK, CSB and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade the converter's performance. If the on board SPI Bus is utilized for other devices it may be necessary to provide buffers between this bus and the AD9640 in order to keep these signals from transitioning at the converter inputs during critical sampling periods.

AD9640 EVALUATION BOARD AND SOFTWARE

The AD9640 evaluation board kit contains a fully populated AD9640 PCB, schematic diagrams, operating software, and a comprehensive instruction manual.

Users can preview the evaluation board schematic, the software, and the instruction manual on the product Web page of the Analog Devices website.

OUTLINE DIMENSIONS

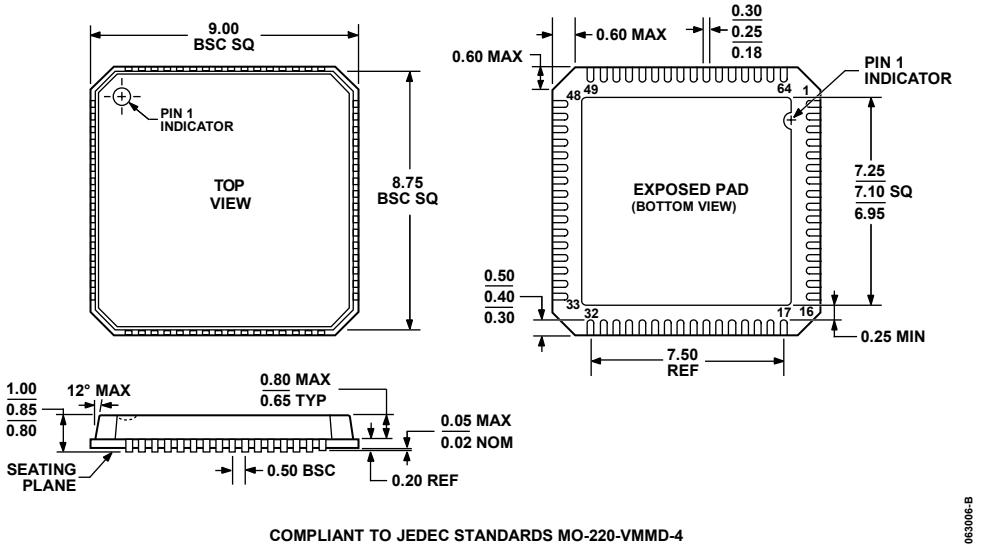


Figure 29. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9mm x 9mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9640BCPZ-150	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-125	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-105	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-80	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640/PCB		Evaluation Board with AD9640 and Software	

PR06547-0-12/06(PrA)

ANALOG DEVICES

www.analog.com