

100182



Not Intended For New Designs
T-45-07

100182 9-Bit Wallace Tree Adder

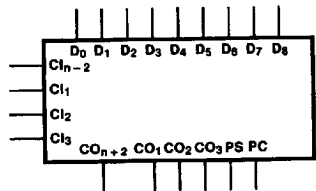
General Description

The 100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The 100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the

100183 Recode Multiplier, the 100179 Carry Lookahead, and the 100180 High-speed Adder, the 100182 assists in performing parallel multiplication of two signed numbers to produce a signed two's complement product. See 100183 data sheet for additional information. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

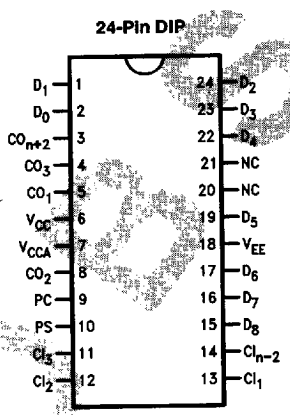
Logic Symbol



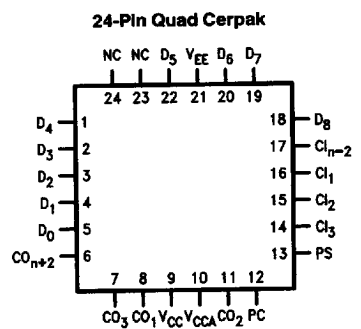
Pin Names	Description
D ₀ -D ₈	Data Inputs
Cl ₁ -Cl ₃ , Cl _{n-2}	Carry Inputs
CO ₁ -CO ₃ , CO _{n+2}	Carry Outputs
PS	Partial Sum Output
PC	Partial Carry Output



Connection Diagrams

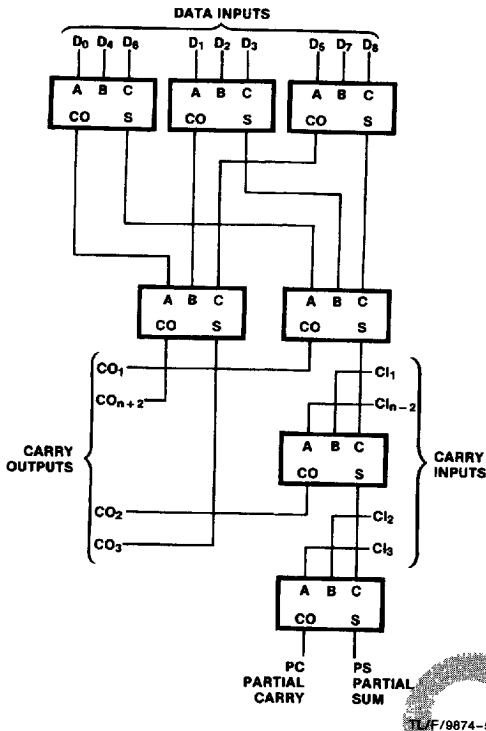


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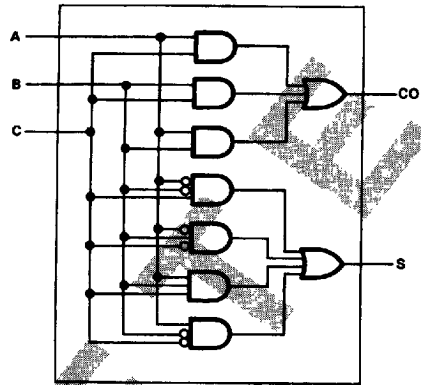


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Logic Diagram



Adder Logic Diagram



Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
 Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
 V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
 Input Voltage (DC) V_{EE} to +0.5V
 Output Current (DC Output HIGH) -50 mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1025	-955	-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810	-1705	-1620			
V _{OHC}	Output HIGH Voltage	-1035			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1020		-870	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1810		-1605			
V _{OHC}	Output HIGH Voltage	-1030			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1595			
V _{IH}	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V _{OH}	Output HIGH Voltage	-1035		-880	mV	V _{IN} = V _{IH} (Max) or V _{IL} (Min)	Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1830		-1620			
V _{OHC}	Output HIGH Voltage	-1045			mV	V _{IN} = V _{IH} (Min) or V _{IL} (Max)	Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610			
V _{IH}	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V _{IL}	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $C_{I1}-C_{I3}, C_{I_{n-2}}$ $D_1, D_3, D_4, D_5, D_6, D_8$			300	μA	$V_{IN} = V_{IH} (Max)$
	D_0, D_2, D_7			250		
I_{EE}	Power Supply Current	-260	-180	-125	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.50	1.40	4.50	1.50	4.70	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.80	1.30	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.20	2.20	6.10	2.30	6.40	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.70	1.40	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.20	2.50	7.20	2.70	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.50	1.00	3.40	1.10	3.70	ns	Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.50	1.50	4.45	1.60	4.60	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.30	0.80	3.20	0.90	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	Figures 1 and 2

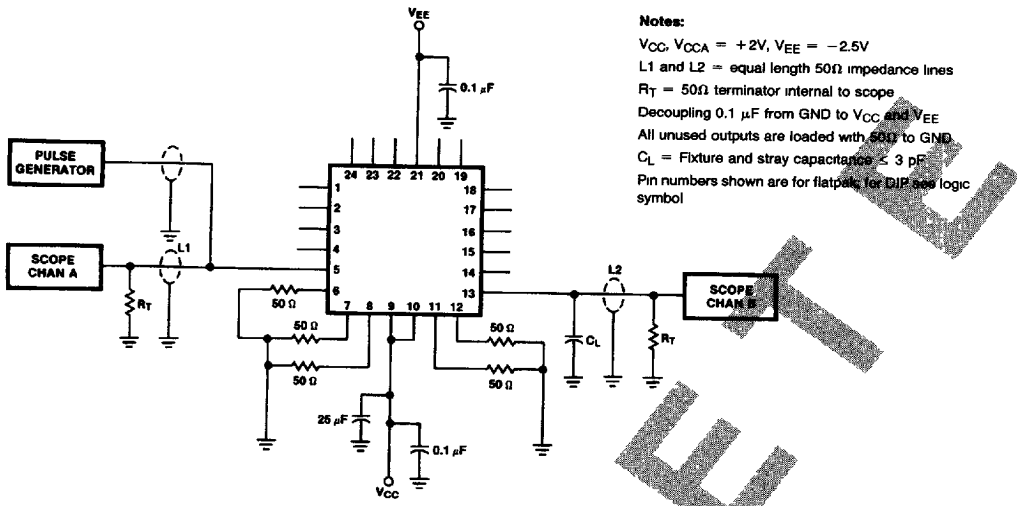
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Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.30	1.40	4.30	1.50	4.50	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.60	1.30	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.00	2.20	5.90	2.30	6.20	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.50	1.40	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.00	2.50	7.00	2.70	7.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Cl_{n-2}, Cl_1 to CO_2	1.00	3.30	1.00	3.20	1.10	3.50	ns	<i>Figures 1 and 2</i>
t_{PLH} t_{PHL}	Propagation Delay Cl_{n-2}, Cl_1 to PS, PC	1.50	4.30	1.50	4.25	1.60	4.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Cl_3, Cl_2 to PS, PC	0.80	3.10	0.80	3.00	0.90	3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	<i>Figures 1 and 2</i>

OBSOLETE



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$
 Pin numbers shown are for flatpack; for DIP see logic symbol

FIGURE 1. AC Test Circuit

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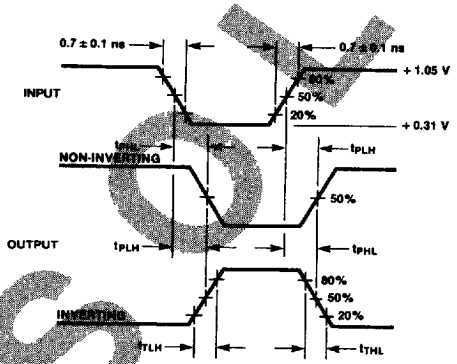


FIGURE 2. Propagation Delay and Transition Times

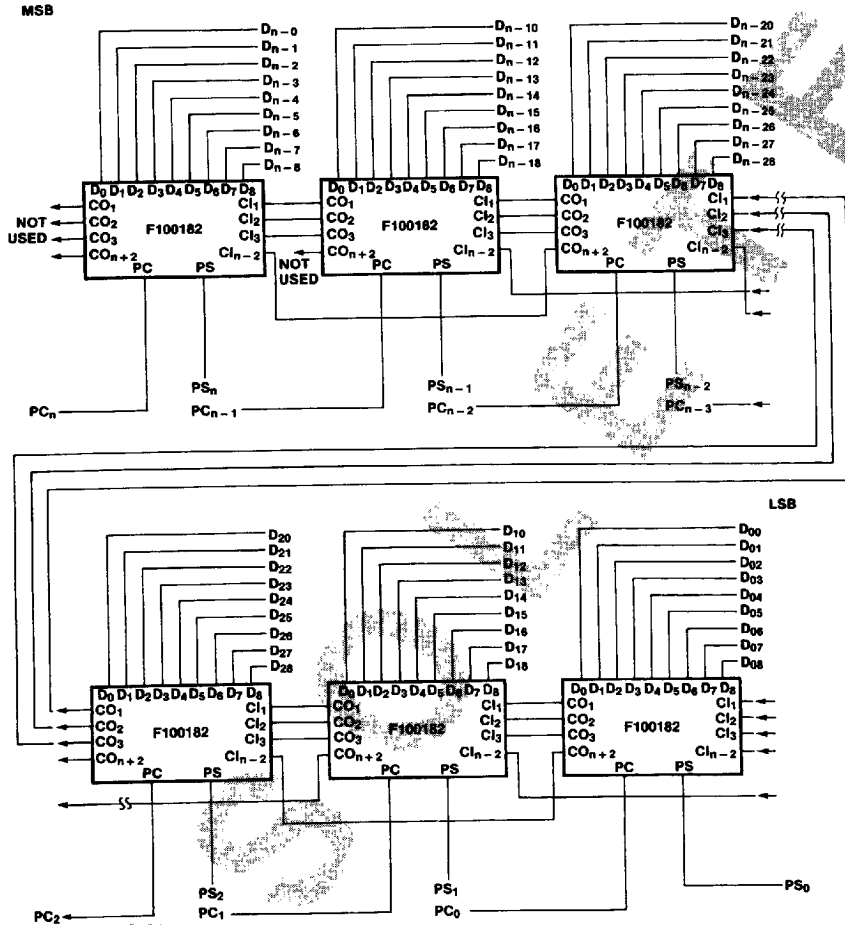
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Application

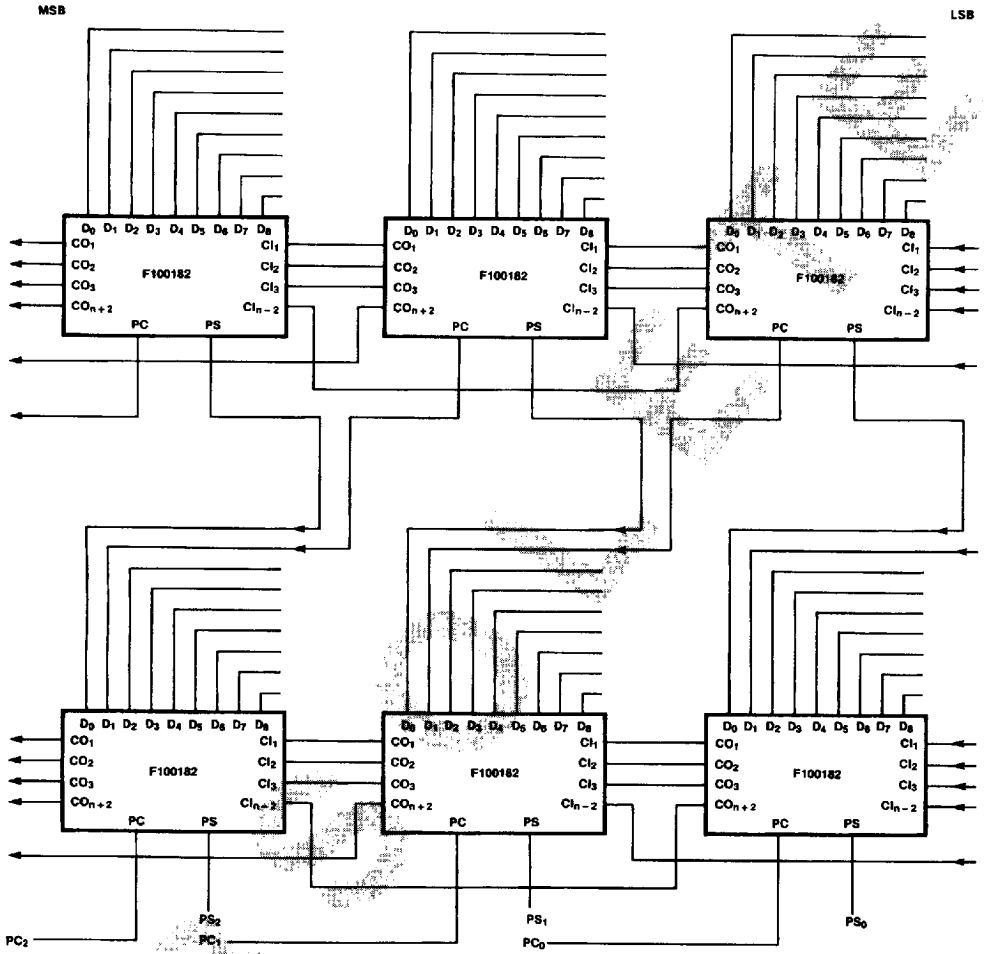
Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182



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Application (Continued)

16-Bit Vertical Expansion of Wallace Tree Adders



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