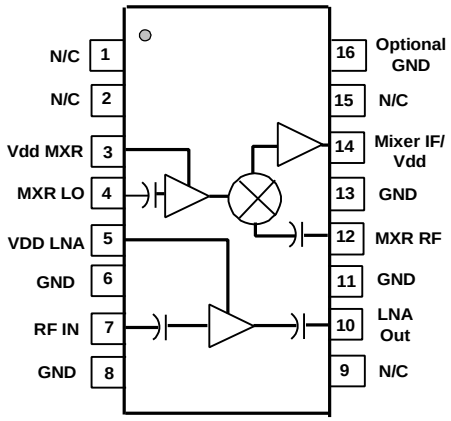
TriQuint SEMICONDUCTOR

WIRELESS COMMUNICATIONS DIVISION

TQ5121

DATA SHEET

3V Cellular TDMA/AMPS LNA/mixer Receiver IC



Features

- *Pin compatible with TQ9222 (dual-band TDMA receiver)*
- *Single 3V operation*
- *Low-current operation*
- *50 W matched inputs*
- *QSOP-16 plastic package*

Applications

- *IS-136 Mobile Phones*
- *AMPS Mobile Phones*
- *ISM 900MHz*

Product Description

The TQ5121 is a 3V, RF receiver IC designed specifically for Cellular band TDMA applications. It's RF performance meets the requirements of products designed to the IS-136 and AMPS standards. The TQ5121 is pin compatible with TQ9222, which enables handset designers to use strategic board platform strategy. The TQ5121 contains LNA+Mixer circuits to handle the 800MHz cellular band.

The mixer uses a high-side LO frequency, with the IF covering a range of 70 to 140MHz. Most RF ports are internally matched to 50 W, greatly simplifying the design and keeping the number of external components to a minimum. The TQ5121 achieves good RF performance with low current consumption, supporting long standby times in portable applications. Coupled with the very small QSOP-16 package, the part is ideally suited for Cellular band mobile phones.

Electrical Specifications[1]

Parameter	Min	Typ	Max	Units
Frequency	869		894	MHz
Gain		17.5		dB
Noise Figure		2.7		dB
Input 3rd Order Intercept		-8.5		dBm
DC supply Current		10.0		mA

Note 1: Test Conditions: Vdd=2.8V, Ta=25C, filter IL=2.5dB, RF=881MHz, LO=991MHz, IF=110MHz, LO input=-7dBm

Electrical Characteristics

Parameter	Conditions	Min.	Typ/Nom	Max.	Units
RF Frequency	Cellular band	869		894	MHz
LO Frequency	Cellular band	950		1040	MHz
IF Frequency	Cellular band	70		140	MHz
LO input level		-7	-4	0	dBm
Supply voltage		2.7	2.8	4.0	V
Gain		16.0	17.5		dB
Gain Variation vs. Temp.	-40 to 85C	-2.0		+2.0	dB
Noise Figure			2.7	3.5	dB
Input 3rd Order Intercept		-11.0	-8.5		dBm
Return Loss	LNA input – external match	10			dB
	LNA output	10			dB
	Mixer RF input	10			dB
	Mixer LO input	10			dB
Isolation	LO to LNA in	40			dB
	LO to IF; after IF match		40		dB
	RF to IF; after IF match		40		dB
IF Output Impedance	Vdd = 2.8V; "ON"		500		Ohm
	Vdd = 0V; "OFF"		<50		Ohm
Supply Current			10	13	mA
Temperature		-40	25	85	C

Note 1: Test Conditions: Vdd=2.8V, filter IL=2.5dB, RF=881MHz, LO=991MHz, IF=110MHz, LO input=-7dBm, T_C = 25 °C, unless otherwise specified.

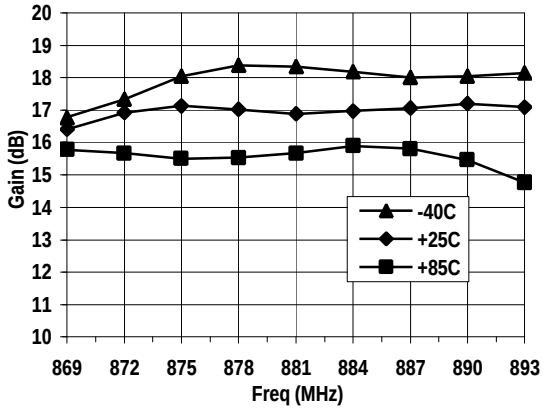
Absolute Maximum Ratings

Parameter	Value	Units
DC Power Supply	5.0	V
Power Dissipation	500	mW
Operating Temperature	-55 to 100	C
Storage Temperature	-60 to 150	C
Signal level on inputs/outputs	+20	dBm
Voltage to any non supply pin	+.3	V

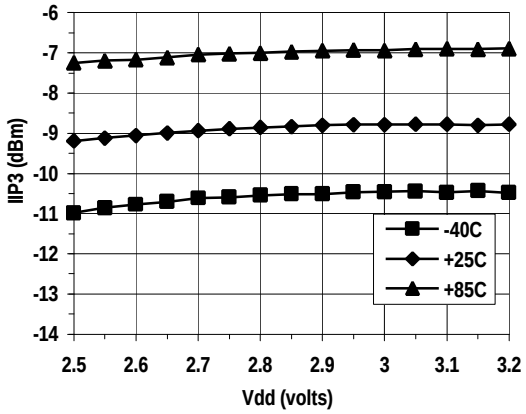
Typical Performance

Test Conditions *(Unless Otherwise Specified): Vdd=2.8V, Ta=25C, filter IL=2.5dB, RF=881MHz, LO=991MHz, IF=110MHz, LO input=-7dBm*

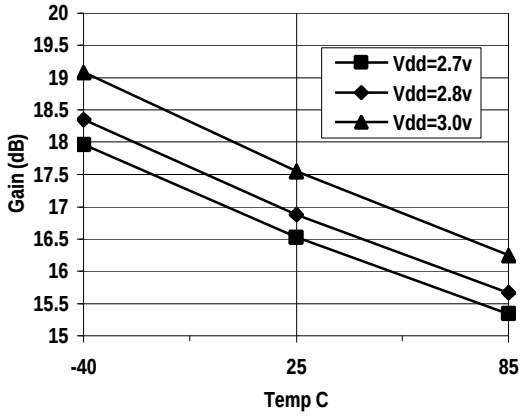
CG vs. Freq vs. Temp



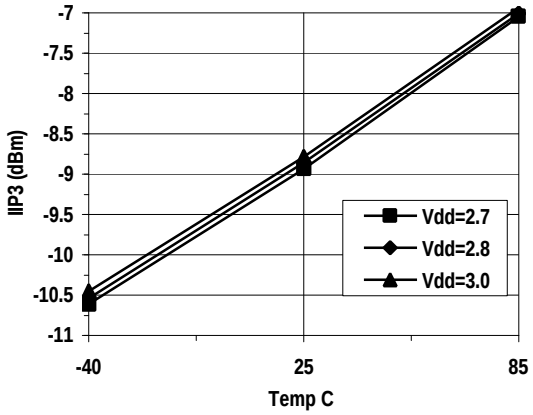
IIP3 vs. Vdd vs. Temp



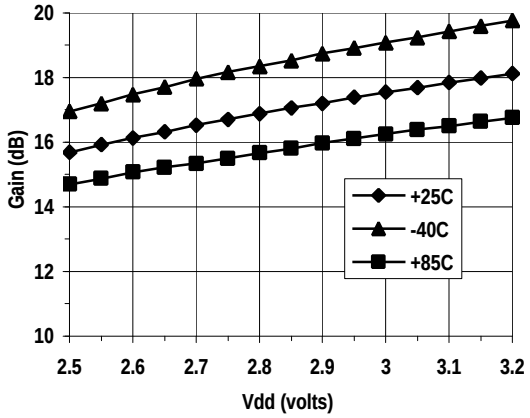
CG vs. Temp vs. Vdd



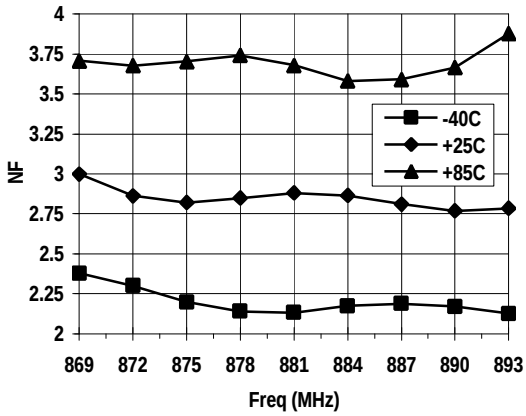
IIP3 vs. Temp vs. Vdd



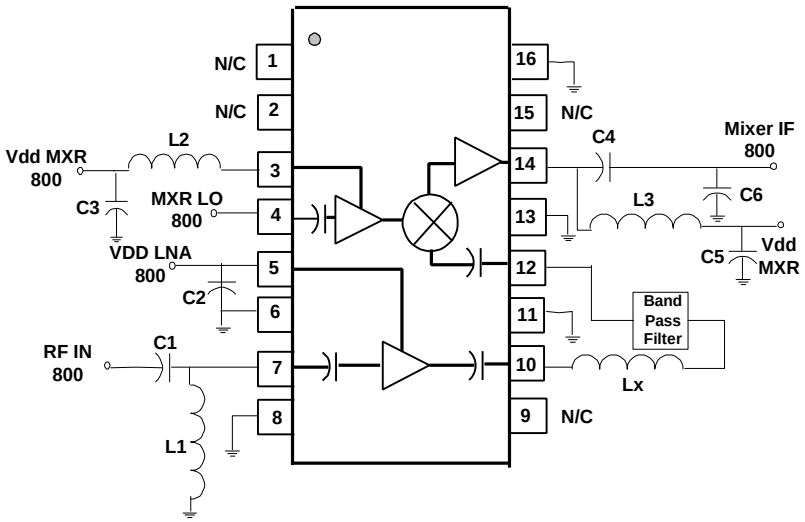
CG vs. Vdd vs. Temp



Noise Figure vs. Freq vs. Temp



Application/Test Circuit



Bill of Material for TQ5121 Receiver Application/Test Circuit

Component	Reference Designator	Part Number	Value	Size	Manufacturer
Receiver IC	U1	TQ5121		QSOP-16	TriQuint Semiconductor
Capacitor	C1		1.2pF	0402	
Capacitor	C2, C3		1000pF	0402	
Capacitor	C4		10pF	0402	
Capacitor	C5		.01µF	0402	
Capacitor	C6		8.2 pF	0402	
Inductor	L1, L2		10nH	0402	
Inductor	L3		180nH	0402	
Inductor	Lx (filter dependent)		10nH	0602	
Toyocom (select)	F1	T726881A	627-881A		Toyocom

TQ5121 Product Description

The TQ5121 3V RFIC Downconverter is designed specifically for cellular band TDMA applications. The TQ5121 contains a LNA+Mixer circuit to handle the 800 MHz cellular band. The IF frequency range covers 70 to 140 MHz with most of the ports internally matched to 50 Ω simplifying the design and keeping the number of external components to a minimum.

Operation

Please refer to the test circuit above.

Low Noise Amplifier (LNA)

The LNA section of the TQ5121 consists of a cascaded common source FETs (see Fig 1). The LNA is designed to operate on supply voltages from 3V to 5V. The source terminal has to be grounded very close to the pin, this will avoid a significant gain reduction due to degeneration. The LNA requires a matching circuit on the input to provide superior noise, gain and return loss performance. The output is close to 50 Ω for direct connection to a 50 Ω image stripping filter.

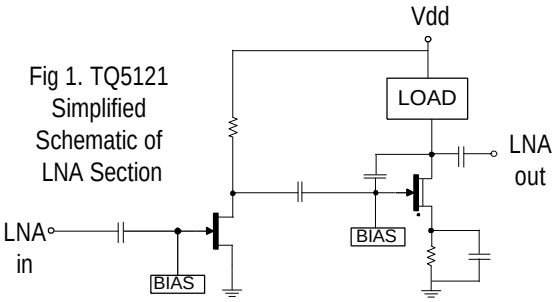


Fig 1. TQ5121 Simplified Schematic of LNA Section

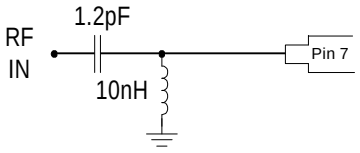
LNA Input Match

To obtain the best possible combination of performance and flexibility, the LNA was designed to be used with off-chip impedance matching on the input. Based on the system requirements, the designer can make several performance trade-offs and select the best impedance match for the particular application.

The input matching network primarily determines the noise and gain performance. Fig 2 shows a suggested input match using a series 1.2pF capacitor and a shunt 10nH inductor.

The LNA gain, noise figure and input return loss are a function of the source impedance (Z_s), or reflection coefficient (Γ_s),

Fig 2. Suggested LNA Input Match



Note: These values assume ideal components and neglect board parasitic. The discrepancy between these values and those of the typical application circuit are the board and component parasitic

presented to the input pin. Highest gain and lowest return loss occur when Γ_s is equal to the complex conjugate of the LNA input impedance. A different source reflection coefficient, Γ_{opt}, which is experimentally determined, will provide the lowest possible noise figure, F_{min}.

The noise resistance, R_n, provides an indication of the sensitivity of the noise performance to changes in Γ_s as seen by the LNA input.

$$F_{LNA} = F_{MIN} + \frac{4R_N}{Z_0} \cdot \frac{|\Gamma_{opt} - \Gamma_S|^2}{|1+\Gamma_{opt}|^2 \cdot \left(1-|\Gamma s|^2\right)}$$

Components such as filters and mixers placed after the LNA degrade the overall system noise figure according to the following equation:

$$F_{SYSTEM} = F_{LNA} + \frac{F_2 - 1}{G_{LNA}}$$

F_{LNA} and G_{LNA} represent the linear noise factor and gain of the LNA and F_2 is the noise factor of the next stage. Thus, the system noise figure depends on the highest gain and minimum noise figure of the LNA.

Designing the input matching network involves a compromise between optimum noise performance and best input return loss. For example, when the TQ5121 LNA is matched for optimum noise figure (1.35dB @ 880 MHz), the input return loss is approximately 4dB. On the other hand, when the LNA is matched for best return loss, the LNA noise figure is approximately 1.95dB @ 881 MHz. See Table 1 for noise parameters.

Table 1. TQ5121 Noise Parameters

Freq (MHz)	|Gopt|	<Gopt	Fmin (dB)	Rn (W)
835	0.678	33	1.34	61.6
850	0.655	34	1.38	61.1
865	0.652	36	1.36	61.2
880	0.652	38	1.35	60.9
895	0.649	38	1.36	61.3
910	0.659	40	1.35	61.2
925	0.687	41	1.35	65.6

LNA Output Match

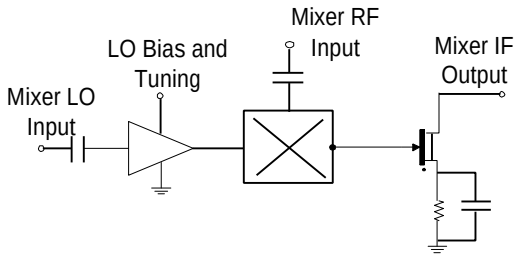
The output impedance of the LNA was designed to interface directly with 50Ω terminations. This internal match serves to reduce the number of external components required at this port. An additional benefit accrues as an improvement in IP3 performance, return loss and power gain.

The output of the LNA will most often be connected to an image stripping filter. Depending on the filter type, additional components might be needed to present a better match to the LNA output. The TQ5121 general applications circuit (page 4) shows a TOYOCOM (637-881A) saw filter. A series inductor "Lx" of 10nH is added to the filter input to improve the match. This series inductor also smoothes out excessive ripple in the filter passband improving the overall performance of the circuit.

Mixer

The mixer of the TQ5121 is implemented by a common source depletion FET. The mixer is designed to operate on supply voltages from 3V to 5V. An on-chip buffer amplifier simplifies direct connection of the LO input to a commercial VCO at drive levels down to -7dBm. The common-gate LO buffer provides a good input match, and supplies the voltage gain necessary to drive the mixer FET gate. The "*open-drain* " IF output allows for flexibility in matching to various IF frequencies and filter impedance's. See Figure 3.

Fig 3. Mixer Section



Mixer: LO Port

As mentioned earlier, a common gate buffer amplifier is positioned between the LO port and the mixer FET gate in order to provide a good impedance to the VCO and to allow operation at lower LO drive levels. The buffer amplifier provides the voltage gain needed to drive the gate of the mixer FET while consuming very little current (approximately 1.5mA).

Because of the broadband 50Ω input impedance of the buffer amplifier and the internal DC blocking capacitor, the user's VCO can be directly connected to the LO input via a 50Ω line with no additional components.

Mixer Input

Although the mixer input port has been designed with a 50Ω impedance, it has been found that LO leakage out through the pin, can in some cases, reflect off the SAW filter and travel back to the mixer input out of phase, causing some degradation in conversion gain and system noise figure. Sensitivity to the phenomena depends on the particular filter model and SAW-mixer transmission line length.

LO Buffer Tune

While the broadband input match of the LO buffer amplifier makes interfacing easy, the broadband gain means that thermal and induced noise at other frequencies can be amplified and injected directly into the LO port of the mixer. Noise at the IF frequency, and at LO +/- IF will be downconverted and emerge at the IF port, degrading the downconverter noise figure.

As indicated on the diagram of Fig 4, in order to test the LO response to these spurious signals, a two-tone signal was injected into the LO port with the RF port terminated in 50Ω. One signal generator is set to the LO frequency at its normal LO drive level usually (-7 dBm). The second signal generator (spurious signal) is set to the LO +/- the IF frequency. The combined input power at mixer LO port has to be less than -50 dBm. The results shown in Table 3 indicate a good suppression of the interfering signals.

Fig 4. LO Spurious Response Diagram

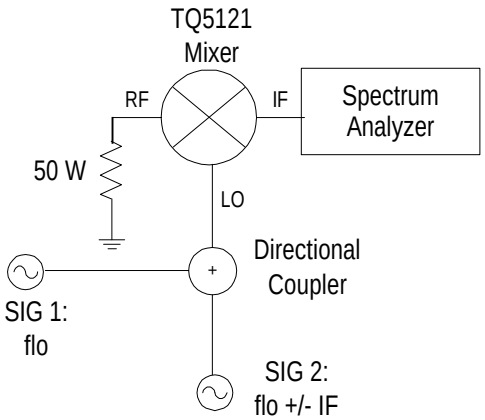


Table 3. LO Spurious Response Data

LO/Spurious (MHz)	Mixer LO Port Input Power	C/V (dB)
991/1101	-57	-71.7
991/1101	-58.9	-71.8

Calculation of Nominal L Value

The node between the LO buffer amplifier and the mixer FET is brought out to Pin 3 (L_tune) and connected to a shunt inductor to AC ground. This inductor is selected to resonate with internal capacitance at the LO frequency in order to suppress out-of-band gain and improve noise performance.

The internal capacitance of the LO amplifier output plus the stray capacitance on the board surrounding Pin 3 is approximately 1.8 pF. The inductor is selected to resonate with the total capacitance at the LO frequency using the following equation:

$$L = \frac{1}{C(2\Pi f)^2}, where \cdot C = 1.5pF$$

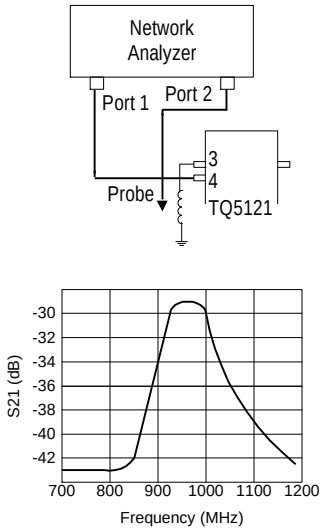
Must be confirmed with measurements on a board approximating the final layout.

Measuring the LO Frequency Response

The frequency response of the LO driver amplifier can be measured using a semi-rigid probe (see Fig. 5) and a network analyzer.

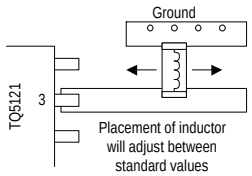
Connect port 1 to the LO input (Pin 4) of the TQ5121 with the source power set to deliver -7 dBm. Connect the coaxial probe to Port 2 and place the probe tip approximately 0.1 inch away from either Pin 3 or the inductor.

Fig 5. LO Buffer Frequency Response



If the calculated shunt inductor (L2) is not a standard value, the AC ground, implemented with C3, can be slide along the transmission line to adjust for the right inductance (fig 6). Once this is completed, the peak of the response should be centered at the center of the LO frequency band.

Fig 6. Adjusting the AC Ground



Mixer IF Port

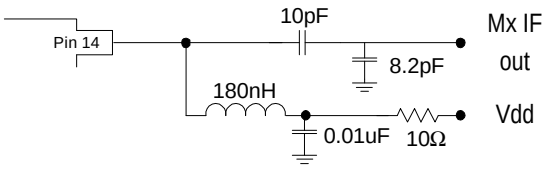
The Mixer IF output is an "open-drain" configuration, allowing for flexibility in efficient matching to various filter types and at various IF frequencies.

For evaluation of the LNA and mixer, it is usually necessary to impedance match the IF port to the 50Ω test systems. When verifying or adjusting the matching circuit on the prototype circuit board, the LO drive should be injected at pin 4 at the nominal power level of -7 dBm, since the LO level does have an impact on the IF port impedance.

There are several networks that can be used to properly match the IF port to the SAW or crystal IF filter. The mixer supply voltage is applied through the IF port, so the matching circuit topology must contain either an RF choke or shunt inductor. An extra DC blocking capacitor is not necessary if the output will be attached directly to a SAW or crystal bandpass filters.

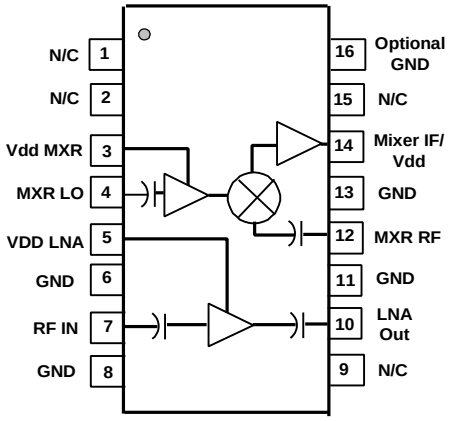
Figure 7 shows the IF matching network, A shunt L, series C, shunt C, is the simplest and requires the fewest components. DC current can be easily injected through the shunt inductor and the series C provides a DC block, if needed. The shunt C, is used to reduce the LO leakage.

Fig 7. IF Output Match (110MHz)



Note: These values assume ideal components and neglect board parasitics. The discrepancy between these values and those of the typical application circuit are the board and component parasitics

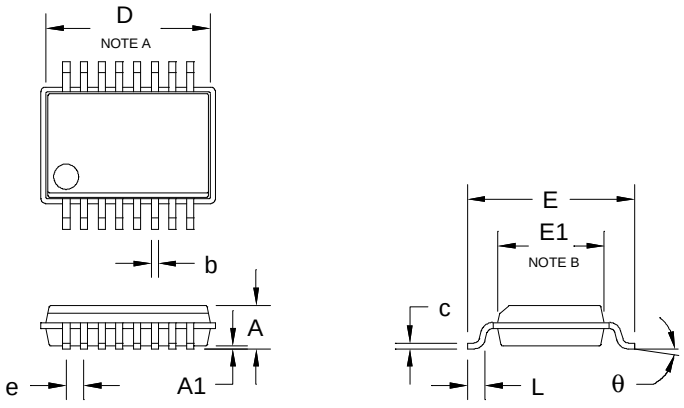
Package Pinout



Pin Descriptions

Pin Name	Pin #	Description and Usage
N/C	1	No Connection
N/C	2	No Connection
VDD_MXR	3	Mixer LO buffer supply voltage. Local bypass capacitor required.
MXR_LO	4	Mixer LO input. DC blocked, matched to 50Ω
VDD_LNA	5	LNA supply voltage. Local bypass capacitor required.
GND	6	Ground
LNA_IN	7	LNA input. DC blocked. Requires external matching elements for noise match and match to 50Ω
GND_LNA	8	LNA first stage ground connection. Connection to ground.
N/C	9	No connection
LNA_OUT	10	LNA output. DC blocked. Matched to 50Ω.
GND	11	Ground
MXR_RF	12	Mixer RF input, DC blocked. Matched to 50Ω.
GND	13	Ground
MXR_IF	14	Mixer IF output. Open drain output, connection to Vdd required. External matching is required.
N/C	15	No connection
Optional GND	16	Optional ground

Package Type: Power QSOP-16 Plastic Package



DESIGNATION	DESCRIPTION	ENGLISH		METRIC		NOTE
A	OVERALL HEIGHT	0.064	+/-.005 in	1.63	+/-.13 mm	C
A1	STANDOFF	0.007	+/-.003 in	0.18	+/-.08 mm	C
b	LEAD WIDTH	0.010	+/-.002 in	0.25	+/-.05 mm	C
c	LEAD THICKNESS	0.085	+/-.015 in	2.16	+/-.38 mm	C
D	PACKAGE LENGTH	0.193	+/-.004 in	4.90	+/-.10 mm	A, C
e	LEAD PITCH	0.025	BSC	0.635	BSC	
E	LEAD TIP SPAN	0.236	+/-.008 in	5.99	+/-.20 mm	C
E1	PACKAGE WIDTH	0.154	+/-.003 in	3.91	+/-.08 mm	B, C
L	FOOT LENGTH	0.033	+/-.017 in	0.84	+/-.43 mm	C
θ	FOOT ANGLE	4	+/-4 DEG	4	+/-4 DEG	

NOTES:

A. THE D DIMENSION DOES NOT INCLUDE MOLD FLASHING AND MISMATCH. MOLD FLASHING AND MISMATCH SHALL NOT EXCEED .006 in (.15 mm) PER SIDE.

B. THE E1 DIMENSION DOES NOT INCLUDE MOLD FLASHING AND MISMATCH. MOLD FLASHING AND MISMATCH SHALL NOT EXCEED .010 in (.25 mm) PER SIDE.

C. PRIMARY UNITS ARE ENGLISH INCHES. THE METRIC EQUIVALENTS ARE SUBJECT TO ROUNDING ERROR.

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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