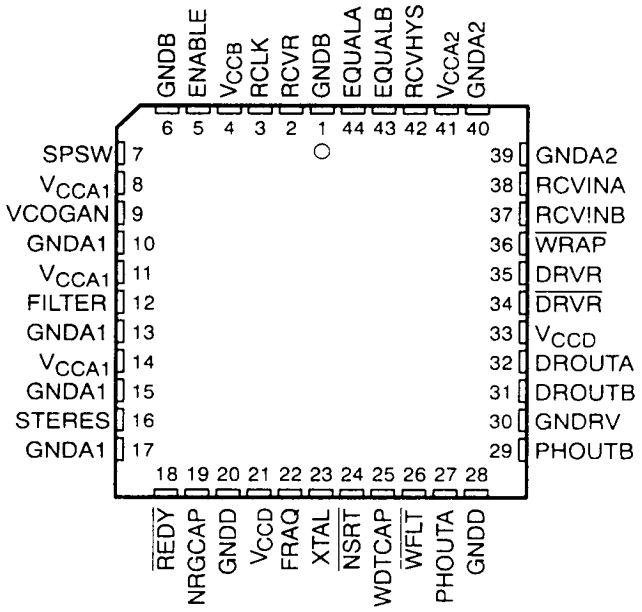
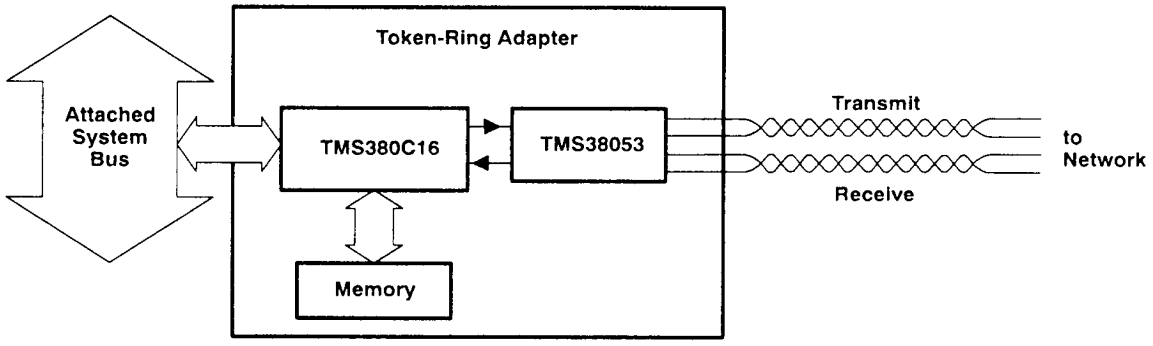
SPWS007 — MARCH 1991

- Facilitates Connection of the TMS380C16 to a Token-Ring Network
- Compatible With Electrical Interface of IEEE Std. 802.5-1989 Token-Ring Access Method and Physical Layer Specifications
- Phase-Locked Loop for Clock Generation and Data Signal Recovery
- Independent Transmit and Receive Channels
- Phantom Drive for Physical Insertion onto Ring
- 16 and 4 Megabit-per-Second Token-Ring Data Rates
- Integrated Receiver Frequency Equalization
- Loop Back (Wrap Mode) for Self-Test Diagnostics
- On-Chip Watchdog Timer
- ESD Protection Exceeds 2KV per MIL-STD-883C, Method 3015
- Advanced Low-Power Schottky Technology
- Cost Effective 44-Lead Plastic Chip Carrier Package (FN Suffix)

FN Package
(Top View)



token-ring LAN application diagram



description

The TMS38053 Ring Interface device with its associated external passive components form a full duplex electrical interface to the Token Ring. Coupling the TMS38053 with the TMS380C16 single-chip Token-Ring COMMprocessor forms a highly integrated Token-Ring LAN adapter compatible with the IEEE Std. 802.5 –1989 Token-Ring Access Method and Physical Layer Specifications.

The TMS38053 operates at the IEEE standard 16 megabit-per-second and 4 megabit-per-second data rates. The Token-Ring data stream is received by the TMS38053 and phase aligned using an on-chip Phase-Locked Loop (PLL). Both the recovered clock and data are passed to the TMS380C16 single-chip Token-Ring COMMprocessor's protocol handling circuits for serial-to-parallel conversion and data processing. On transmit, the TMS380C16 provides a differential signal which the TMS38053 converts to analog levels for transmission on the media. A watchdog timer is also included to provide fail-safe de-insertion from the ring in the event of a station failure.

The major functional blocks of the TMS38053 include the Receiver, Data Latch, Transmitter, Wrap, Phantom Driver and Wire-Fault Detector, Watchdog Timer, Phase-Locked Loop, Energy Detect, and Voltage Regulator, as shown in Figure 1.

The TMS38053 is available in a 44-lead plastic chip carrier package and is rated for operation from 0°C to 60°C.

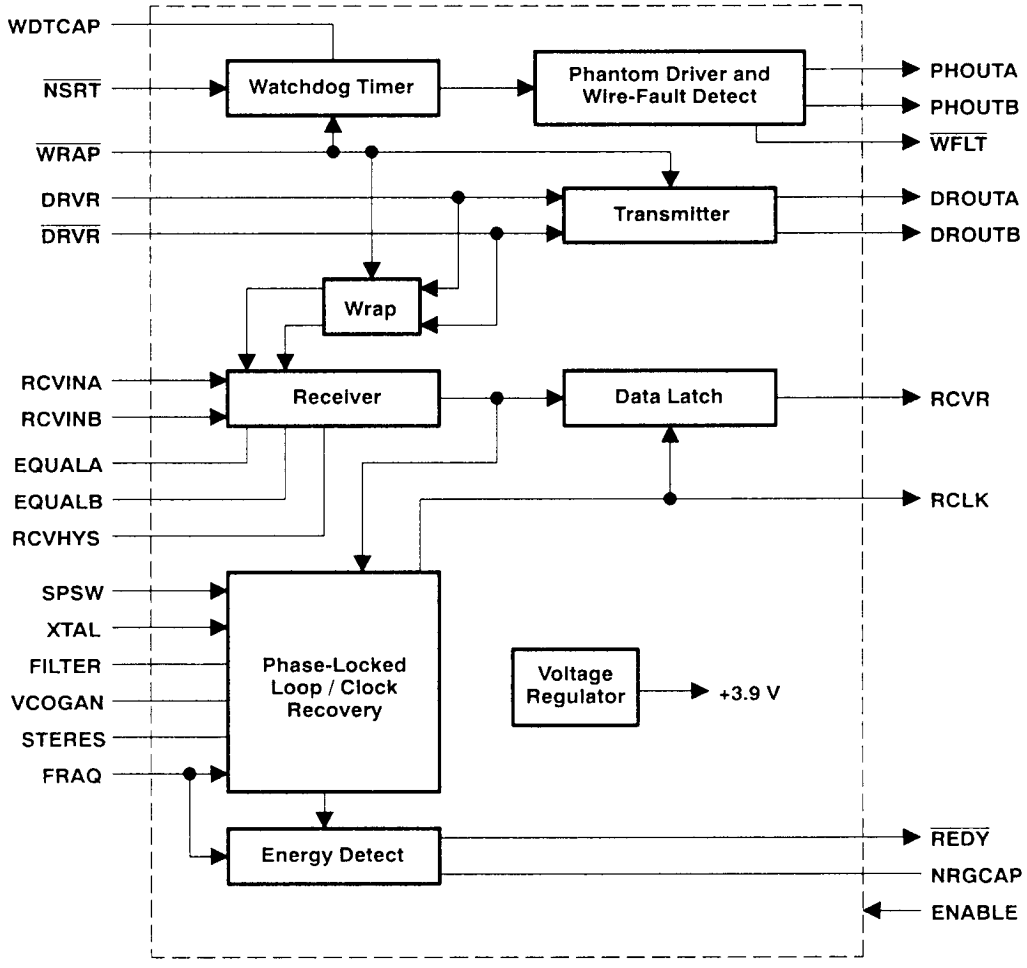


Figure 1. Functional Block Diagram

Terminal Functions

NAME	PIN NO.	I/O/E†	Type‡	DESCRIPTION
DROUTA DROUTB	32 31	O O	N N	Driver Outputs A and B. These pins are the differential driver outputs to the token ring via isolation transformers.
$\overline{\text{DRVR}}$ DRVR	35 34	I I	T T	Differential Driver Data Inputs. These pins are the differential inputs that receive the TMS380C16 transmit data.
ENABLE	5	I	T	Output-Enable Control: TTL input pin used to enable a board test mode. High = TMS38053 operates normally Low = All TTL outputs and Phantom Drive outputs are driven to high impedance. DROUTA and DROUTB are not affected.
EQUALA EQUALB	44 43	E E	N N	Equalization/Gain Point A and B. Connections to allow frequency tuning of equalization circuit.
FILTER	12	E	N	Charge Pump Output/Filter Buffer Input. This pin allows connection of external components for the PLL filter.
FRAQ	22	I	T	Frequency Acquisition Control. This TTL input pin determines the use of frequency or phase acquisition mode. High = Wide range. Frequency centering to XTAL reference. Low = Narrow range. Phase-Locked onto the incoming data (RCVINA and RCVINB).
NRGCAP	19	E	N	Energy-Detect Capacitor. This pin allows connection to an external capacitor for sensing received data transitions (energy).
$\overline{\text{NSRT}}$	24	I	T	Phantom-Driver Control. This TTL input pin enables the phantom driver outputs (PHOUTA and PHOUTB) through the watchdog timer for insertion onto the token ring. Static High = Inactive, phantom current removed (due to watchdog timer) Static Low = Inactive, phantom current removed (due to watchdog timer) Falling edge = Active, current output on PHOUTA and PHOUTB.
PHOUTA PHOUTB	27 29	O O	N N	Phantom Driver Outputs A and B. These pins are the outputs that cause insertion onto the token ring.
RCLK	3	O	T	Recovered Clock. This output signal is the clock recovered from the token ring received data. For 16 Mbps operation it is a 32-MHz clock. For 4 Mbps operation it is an 8-MHz clock.
RCVHYS	42	E	N	Receiver Hysteresis Resistor. This connection allows setting of the receiver hysteresis threshold.
RCVINA RCVINB	38 37	I I	N N	Receiver Input A and B. These differential inputs receive the token-ring data via isolation transformers.
RCVR	2	O	T	Recovered Data. This output signal contains the data recovered from the token ring.
$\overline{\text{REDY}}$	18	O	T	Ready Signal. This TTL output pin to the TMS380C16 provides an indication that sufficient time has elapsed since the last transition of FRAQ for the PLL to achieve lock as monitored by the energy detect capacitor. High = Received data not valid. Low = Received data valid.
SPSW	7	I	T	Speed Switch. This TTL input pin specifies the token-ring data rate. High = 4 Mbps data rate. Low = 16 Mbps data rate.
STERES	16	E	N	Static Timing Error Resistor. This pin allows connection to an external resistor for adjusting the static timing error.
VCOGAN	9	E	N	VCO Gain Resistor. This pin allows connection to an external resistor for setting the VCO gain.

† I = Input, O = Output, E = Provides external component connection to the internal circuitry for tuning.
‡ T = TTL signal, N = Non TTL signal

Terminal Functions (continued)

NAME	PIN NO.	I/O/E†	Type‡	DESCRIPTION
WDTCAP	25	E	N	Watchdog Timer Capacitor. This pin allows connection to an external capacitor, which sets the watchdog timeout period.
$\overline{WFLT}$	26	O	T	Phantom Wire Fault Output. This TTL output pin provides an indication of the presence of a short circuit or open on the PHOUTA or PHOUTB pins. High = No fault. Low = Open or short.
$\overline{WRAP}$	36	I	T	Internal-Wrap Mode Control. This TTL input pin allows the TMS38053 to be placed in the loopback "wrap" mode for adapter self test. High = Normal ring operation. Low = Transmit data drives the Receive data.
XTAL	23	I	T	Crystal-Oscillator Input. This crystal input pin (normally externally gated by FRAQ) is used to synchronize the PLL. This signal is 32 MHz for 16 Mbps ring, and 8 MHz for 4 Mbps ring.
V_{CCD}§	21,33			Positive supply voltage for digital circuits (5 V).
GNDD§	20,28			Ground reference for digital circuits.
V_{CCB}§	4			Positive supply voltage for input and output buffers.
GNDB§	1,6			Ground reference for input and output buffers.
V_{CCA1}§	8,11,14			Positive supply voltage for VCO and filter input.
GNDA1§	10,13,15,17			Ground reference for VCO and filter input.
V_{CCA2}§	41			Positive supply voltage for receiver circuits.
GNDA2§	39,40			Ground reference for receiver circuits.
GNDRV§	30			Ground reference for driver output circuits.

† I = Input, O = Output, E = Provides external component connection to the internal circuitry for tuning.
‡ T = TTL signal, N = Non TTL signal
§ These pins should be connected to a single power or ground plane as appropriate.

architecture

The major blocks of the TMS38053 include the Receiver, Data Latch, Transmitter, Wrap, Voltage Regulator, Energy Detect, Phase-Locked Loop, Watchdog Timer, and Phantom Driver and Wire-Fault Detect. The functionality of each block is described in the following sections.

receiver

The purpose of the receiver circuit is to read incoming data from the ring. The receiver circuit provides five functions:

1. DC bias for the differential input.
2. Clamping of large signal swings.
3. Gain and equalization.
4. Definition of thresholds.
5. Hysteresis for data detection.

Gain, as a function of frequency, is set by the equalizer impedance. Equalization characteristics are determined by the external equalization circuit across the EQUALA and EQUALB pins. Equalization is effective at low signal amplitudes. At larger signal levels, nonlinear effects reduce the effective equalization. The signal level where saturation occurs is determined by the impedance between EQUALA and EQUALB. The circuit is suitable for Differential Manchester-encoded data at 16- or 4-megabits-per-second (Mbps).

data latch

The output of the Receiver drives two internal circuits: the Data Latch and the Phase Detector. The latch samples the internal receiver output signal on the rising edge of the internal recovered clock. Data (RCVR) is therefore stable and may be sampled at the rising edge of RCLK. The timing of this edge is set by the Phase Detector and other loop components so that the received signal is sampled at the optimum time for error free data recovery.

Both the sampled data and the recovered clock signal are buffered and sent to the TMS380C16 Token Ring COMMprocessor as the RCVR and RCLK signals respectively, to provide decoding of the Differential Manchester data.

Static-timing error is defined as the amount of error that the rising edge of the recovered clock has from midpoint of the data signal into the data latch. An error of zero is optimum sampling, as this places the rising edge of the sampling clock in the middle of the data pulse. A positive offset represents early sampling.

transmitter

The transmit driver provides differential current drive at a suitable level for driving the data onto the ring. Both outputs (DROUTA and DROUTB) are open collector, intended to drive a center-tapped transformer, with the center tap connected to V_{CC}. The output stage controls a fixed current between the two outputs, under the control of the driver data input (DRVR and $\overline{\text{DRVR}}$).

The DRVR and $\overline{\text{DRVR}}$ inputs drive a differential transmit circuit that enhances the symmetry of the current switching on DROUTA and DROUTB.

The DRVR and $\overline{\text{DRVR}}$ inputs are not retimed within the TMS38053. Consequently, low skew in the input is important in order to avoid degrading the transmitted output waveform. The transmitter-drive outputs are not affected by the ENABLE signal. When DRVR is high and $\overline{\text{DRVR}}$ is low, the output current is directed to driver output DROUTA and, when reversed, to output DROUTB.

wrap

The wrap function is designed to provide an internal signal path used for system self-test diagnostics. When the internal-wrap mode control input ($\overline{WRAP}$) is taken low, the transmitter outputs are disabled and the receiver inputs are ignored. An alternate path is provided from the transmitter output circuitry to the receiver input circuitry through the wrap circuit. This wrap path to the RCVR pin inverts the transmitted signal. In the internal-wrap mode, attenuation can be checked by observing the signal amplitude at the equalization pins EQUALA and EQUALB. Equalization will be active at this signal level although the signal will not exhibit the high-frequency attenuation effects for which equalization is intended to compensate.

phantom driver and wire-fault detector

The phantom drive circuit under control of the $\overline{NSRT}$ input generates a DC signal on both of the two drive outputs, PHOUTA and PHOUTB. To maintain the DC signal, $\overline{NSRT}$ must provide a positive (low-to-high) clock edge once every 20 milliseconds. An internal watchdog timer (oneshot) is designed so that the PHOUTA and PHOUTB DC signal is removed if the $\overline{NSRT}$ input fails to have the required transitions. The PHOUTA and PHOUTB signal is sent over the transmit-signal pair to the Trunk Coupling Unit (TCU) to request that the station be inserted into the ring. The signal current is detected by the TCU, causing the external-wrap path from the transmitter outputs back to the receiver inputs to be broken. A connection is established from the ring to the receiver inputs and from the transmitter outputs to the ring. The phantom drive outputs are short circuit protected and will detect a short circuit from either output to ground or when there is an abnormally low load current at either output corresponding to an open circuit in the signal or TCU wiring. Either type of fault results in the wire-fault indicator output ($\overline{WFLT}$) to be driven low. The logic state of $\overline{WFLT}$ will go high when $\overline{NSRT}$ is high. All three outputs, PHOUTA, PHOUTB, and $\overline{WFLT}$, are in a high-impedance state when the output-enable control (ENABLE) is low.

watchdog timer

The watchdog timer provides protection against a failed adapter remaining on the ring. The $\overline{NSRT}$ pin must be toggled low or the watchdog timer will turn off the phantom drive. The period of the watchdog timer is determined by the value of the external capacitor connected to the WDTCAP pin.

The capacitor is chosen to give a period of 21 milliseconds minimum and 50 milliseconds maximum. This assures compatibility with a system that toggles $\overline{NSRT}$ at a rate faster than once every 20 milliseconds, and to ensure a de-insertion from the ring will occur within 50 milliseconds of the last $\overline{NSRT}$ high-to-low transition.

The duty cycle of $\overline{NSRT}$ is not critical. Phantom drive will be turned on following a falling $\overline{NSRT}$ edge. De-insertion will occur if $\overline{NSRT}$ is left high or low, or if the internal wrap mode is selected from pin $\overline{WRAP}$. The following describes the operation of the watchdog timer and indicates the priorities of the control signals.

- $\overline{WRAP}$-low (internal mode selected).
  - Phantom drive will be off. Operation of the watchdog timer is not defined but may continue and if the timer has not expired, taking $\overline{WRAP}$ high may result in the phantom drive being turned on.
- $\overline{WRAP}$-high.
  - If the timing capacitor is connected and $\overline{NSRT}$ goes from high to low, then the timing capacitor is charged or recharged to a defined level. Phantom drive will be on, and the timing capacitor discharging will continue.
  - If the timing capacitor is connected and $\overline{NSRT}$ goes from low to high, there is no effect on the watchdog timer, and the timing capacitor discharging will continue.
  - If the timing capacitor is connected and the capacitor discharges to a defined level, the phantom drive will be turned off, regardless of the state of $\overline{WRAP}$.
  - If the timing capacitor is not connected and the timing capacitor pin is held to V_{CC}, then the phantom drive will be controlled directly by $\overline{NSRT}$. This serves to disable the watchdog timer function.

voltage regulator

The internal voltage regulator is used to make the performance of the TMS38053 less dependent on the supply voltage. The regulator consists of a "band gap" reference, scaled up to a nominal 3.9 V, with a temperature coefficient designed to compensate for coefficients in circuits referenced to the voltage regulator.

phase-locked loop/clock recovery

The TMS38053 contains a Phase-Locked Loop (PLL) for recovering a data clock from the received bit stream. The elements of the phase-locked loop are: phase and frequency detectors, a charge pump, an external filter (connected to the FILTER pin), a filter buffer, a voltage-to-current converter, and a voltage-controlled oscillator. There are three pins on the TMS38053 which allow connection to external components and tuning of the characteristics of the phase-locked loop. These pins are FILTER, STERES, and VCOGAN. Figure 2 illustrates these blocks. The following paragraphs describe the PLL elements.

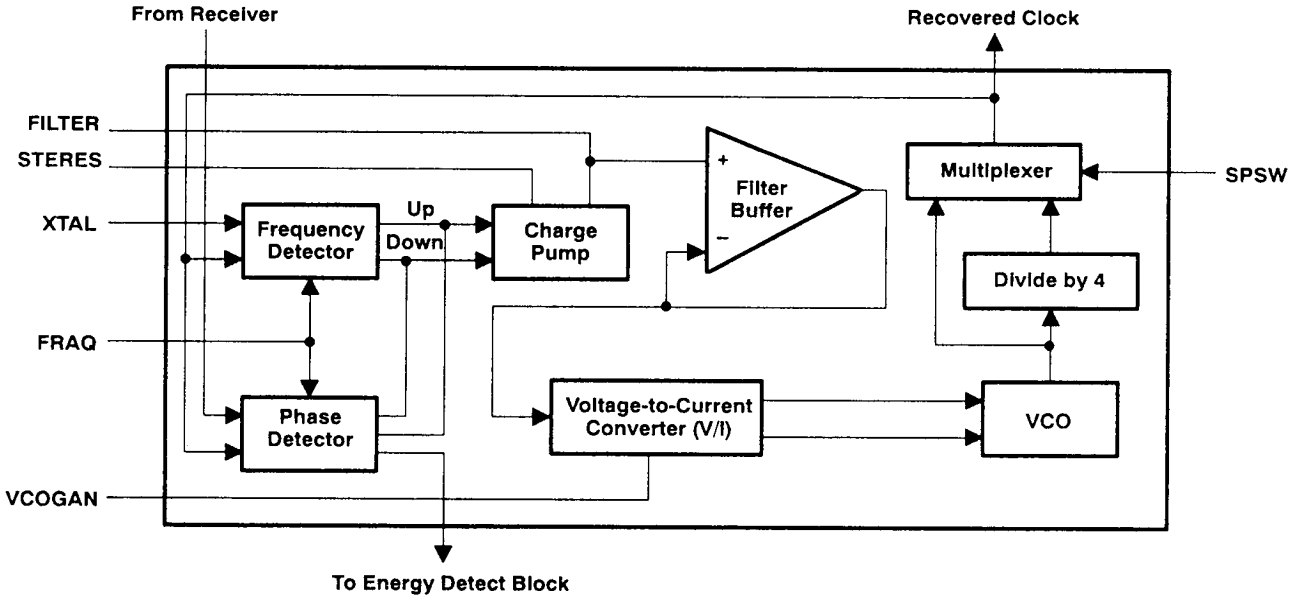


Figure 2. Phase-Locked Loop Block Diagram

phase and frequency detectors

The phase and frequency detector blocks generate control signals suitable for controlling the charge pump. The frequency detector is used to bring the frequency of the voltage-controlled oscillator (VCO) close to the frequency of the crystal-oscillator input, XTAL. The phase detector is then used to provide precise phase alignment of the recovered clock to the incoming data. The circuit is not capable of locking the PLL in cases where the VCO frequency and incoming data frequency differ substantially, hence the need for frequency centering before phase alignment to incoming data occurs.

The phase detector compares the phase of the received data and the recovered clock and generates a pair of phase error correction signals for the charge pump on each rising edge of a data transition. The charge pump UP-pulse is enabled on a rising edge of received data and disabled on the rising edge of the recovered clock. The charge pump DOWN-pulse is enabled on the rising edge of the recovered clock and disable on the falling edge of the recovered clock after each charge pump UP-cycle. Thus, if received data (for 16 Mbps) consists of all 0s which is an effective 16 MHz, a charge pump sequence is initiated at a 16-MHz rate. If received data (for 16 Mbps) consists of all 1s, which is an effective 8 MHz, the charge pump sequence is initiated at an 8-MHz rate.

A multiplexer selects the required detection mode during insertion onto the ring. The frequency-detection mode is selected by taking FRAQ high, and the phase-detection mode is selected by taking FRAQ low. The phase or frequency detectors supply the necessary charge (or UP) and discharge (or DOWN) control signals to the charge pump.

charge pump

The charge pump is designed to supply charge to and to remove charge from the external filter components.The output of either the phase detector or frequency detector drives the charge pump as selected by the FRAQ input. The charge pump has two internal inputs so there are four possible states of the charge pump.

1. Pump up – current into the filter increasing the voltage.
2. Pump down – current out of the filter reducing the voltage.
3. No pump – high-impedance state, holding the voltage on the filter.
4. Pump up and pump down – both currents on, not allowed by the detector logic.

The pump UP and pump DOWN currents are approximately equal, the net charge supplied by the charge pump in a given time therefore depends primarily on the relative duration and frequency of "UP" and "DOWN" controls from the Phase and Frequency Detectors. If the net current output is positive, the voltage at the FILTER pin will rise causing an increase in the VCO clock frequency. If the net output is negative, then the FILTER pin voltage will fall slowing the VCO clock.

The charge-pump block has two constant current circuits operating continuously, one for pump UP and one for pump DOWN. They are designed for stability under all operating conditions. The UP current is fixed and directly affects the magnitude of the loop gain and therefore the bandwidth and damping factor of the loop. Any difference between the UP and DOWN currents will create an offset in the Loop, which will introduce static timing error. An external resistor at STERES (pin 16) is included to allow slight variation in the DOWN current and therefore allows the static timing error of the loop to be adjusted to compensate for error introduced by the charge pump and other elements of the PLL.

external filter

The external filter consists of passive external components connected from the FILTER pin to ground.

A system diagram for the PLL circuit is shown in Figure 3. The Phase Detector/Charge Pump Gain, G_d, is given in the Electrical Specifications at 16 Mbps for a data pattern of all 0s. This result is in μA/ns, which can be converted to A/rad by multiplying by using the equation on the following page. The value in A/rad is the same at both 16 Mbps and 4 Mbps.

The VCO Gain, G_O, is given in the Electrical Specifications at 16 Mbps. This value is in MHz/volt, which can be converted to rad/volt by using the equation on the following page. The value at 4 Mbps is one-fourth this value because of the 4x divider on the VCO output at 4 Mbps.

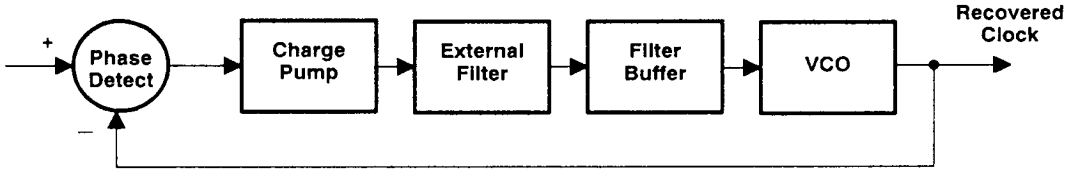


Figure 3. Analytical PLL Diagram

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A typical external filter circuit is shown in Figure 4. The capacitor C5 limits the filter buffer ripple, but should be chosen as small as possible to reduce PLL overshoot. The resistor R5 sets the effective bandwidth of the PLL closed loop, and capacitor C4 sets the damping factor. The filter buffer is an amplifier with bandwidth at 3–5 MHz. Inductor L1 is used to compensate for the effects of the filter buffer and R16 can optionally be used to adjust the correlated jitter.

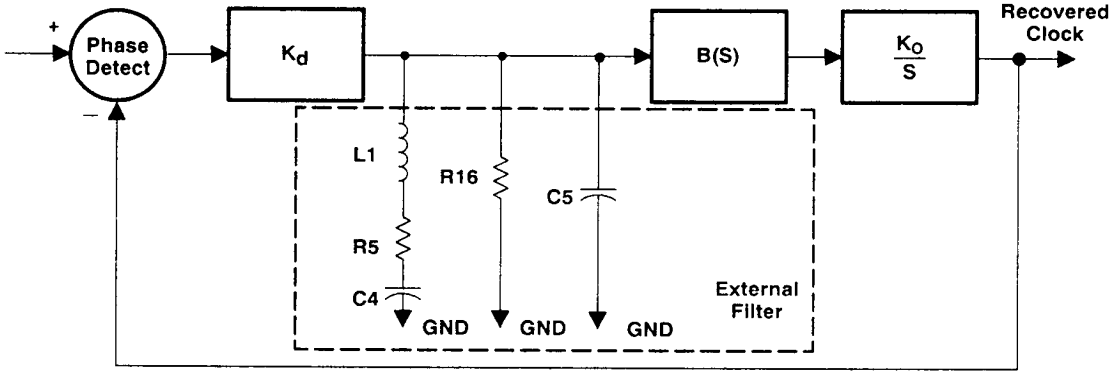

Figure 4. Analytical PLL Model

The simplified equations for the PLL are:

VCO Gain	$K_O = (G_O)(10^6)(2\pi)(F)$	rad/(S • V)
Phase Detector Gain	$K_d = \frac{(G_d)(10^3)(D)(31.25)(10^{-9})}{2\pi}$	A/rad
PLL Noise Equivalent Bandwidth	$B_L = \frac{(K_O)(K_d)(R5 \text{ in ohms})}{4}$	Hz

G_O = the VCO gain measured in MHz/V

G_d = Phase Detector gain measured in μA/ns

F = the Frequency Divider Factor; i.e.,
F = 1.0 for 16 Mbit/s operation
F = 0.25 for 4 Mbit/s operation

D = the Data Transition Density Factor; i.e.,
D = 1.0 for Manchester-encoded 0 data
D = 0.5 for Manchester-encoded 1 data
D = 0.75 for random data

These above equations are only a guide and the actual bandwidth and PLL damping characteristics should be obtained through correlation and modeling on specific hardware implementations that take into effect all circuit card parasitics. Both 16 Mbps and 4 Mbps ring operation can be achieved by suitable selection of glue components at each frequency. More information on PLL characteristics are found in:

— Gardner, Floyd, *PhaseLock Techniques*, John Wiley & Sons, 1979.
— *Token Ring Access Method and Physical Layer Specification*, ANSI/IEEE Standard 802.5 –1989.
— *Gardner, Floyd, "Charge-Pump Phase-Locked Loops", IEEE Transaction Communications, Vol. COM–28, pp. 1849 – 1858, Nov. 1980.*

filter buffer and voltage-to-current converter (V/I)

The filter-buffer amplifier is a unity gain amplifier used to buffer the voltage present at the FILTER pin with minimal leakage current. The output of the filter buffer drives a voltage-current (V/I) converter which produces equal currents, proportional to the filter voltage, for use in the voltage-controlled oscillator (VCO). The current level or constant of proportionality is set by the external resistor connected to ground connected at the VCOGAN pin. This resistor sets the VCO gain which is critical to loop gain and damping. The filter voltage range over which the current level tracks the voltage determines the pull-in range of the VCO.

voltage-controlled oscillator (VCO)

The voltage-controlled oscillator (VCO) is an emitter-coupled astable multivibrator. The frequency is set by internal circuit parameters, the currents from the filter buffer, and an internal VCO timing capacitor. Symmetrical circuit design helps ensure symmetry of the VCO output, which has a nominal frequency of 32 MHz. The VCO output is buffered and sent to the divider (for 4 Mbps) and multiplexer circuit.

divider and multiplexer

The multiplexer selects the source of the recovered clock which may be either the direct output of the VCO (a nominally 32 MHz signal) or the divided version of the VCO output (nominally an 8 MHz signal) for 16 or 4 Mbps operation. The output clock of the VCO is fed both to a "divide by 4" circuit and to a multiplexer. The divider is enabled when SPSW (pin 7) is high. The recovered clock is passed to both frequency and phase detectors, the clock of the data latch, and is buffered at the RCLK pin and passed on to the TMS380C16 COMMprocessor for processing of the received data.

energy detect

The energy detect circuit provides a timing delay of the $\overline{\text{REDY}}$ signal. Whenever the FRAQ pin changes state, it indicates to the energy detect circuit that a change of lock mode has occurred and that time must be allowed before data recovered by the TMS38053 can be considered valid. The energy detect timing capacitor is, therefore, discharged shortly after a low or high going transition of FRAQ, which results in the $\overline{\text{REDY}}$ signal being deasserted.

The time taken for the TMS38053 to acquire phase-lock will depend on the transition density of the incoming data, so the delay of the energy detect circuit must also change. Each rising transition of data results in a current pulse of fixed duration being injected into the energy timing capacitor. The charge time of the capacitor will therefore be dependent on incoming data transition density, $\overline{\text{REDY}}$ is then re-asserted after the capacitor reaches an internally set threshold voltage.

A small discharge current is always present on the energy timing capacitor. When the incoming data transition density falls below a certain threshold, the current pulses may not be sufficient to overcome this discharge current and $\overline{\text{REDY}}$ may, therefore, not be asserted.

test mode

The TMS38053 features a test mode for board-level testing with the components in the circuits. This facilitates testing by bed-of-nails testers. This test mode is enabled by pulling the ENABLE pin to a low level. The media-driver outputs (DROUTA and DROUTB) are not affected by this function. When the ENABLE pin is high, the TMS38053 operates normally. When the ENABLE pin is low, the circuit will continue to operate except that pins PHOUTA, PHOUTB, RCVR, $\overline{\text{WFLT}}$, and RCLK, are driven to the high-impedance state, and pin $\overline{\text{REDY}}$ is driven to the high state.

external passive circuitry

Figure 5 shows an arrangement of external components for a typical 16-Mbps or 4-Mbps Token Ring Interface. The selection of component values is dependent on the objective of the design. The design needs to take into account the importance of layout and component selection (values and tolerances).

ISU1 and ISU2 contain both the transformers for coupling data from the TMS38053 to the ring and the protection circuitry against large voltage excursions. The low frequency gain is set by the sum of the two equalization resistors, R1 + R2, connected from pin EQUALA to pin EQUALB in the emitter circuit of the differential input stage. High-frequency gain is set by resistor R1 because R2 is bypassed by the equalization capacitor C1. The frequency at which equalization becomes effective is determined by the values of R1 and C1.

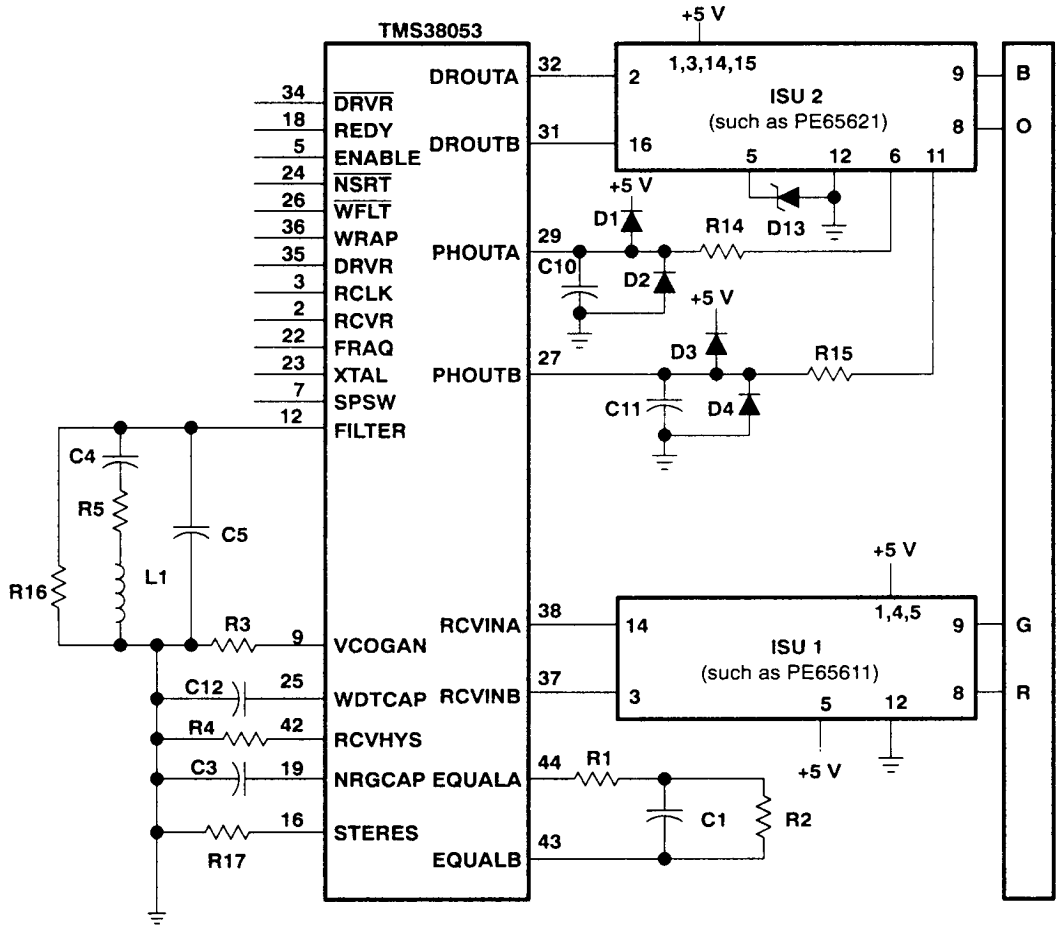

Figure 5. Typical Token-Ring Interface Circuit for 16 or 4 Mbps

Table 1. Typical Components for Figure 5

SYMBOL(S)	FUNCTION
C1	Equalizer capacitor
C3	Energy detect capacitor
C4	PLL filter capacitor
C5	PLL filter capacitor
C10, C11	Phantom drive isolation capacitor
C12	Watchdog timer capacitor
D1-D4	Phantom surge suppression diodes
D13	Driver surge suppression Zener diode
L1	Compensation inductor
R1	Equalizer resistor
R2	Equalizer resistor
R3	VCO Gain resistor
R4	Receiver hysteresis resistor
R5	PLL filter resistor
R14, R15	Phantom drive resistor
R16	Pattern jitter resistor
R17	Static timing error resistor
ISU 1	Isolation/shaping unit (such as Pulse Engineering's PE65611)
ISU 2	Isolation/shaping unit (such as Pulse Engineering's PE65621)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range (see Note 1) . . . . . – 0.5 V to 7 V
Output voltage range: Driver outputs . . . . . – 0.5 V to 8 V
All other outputs (see Note 2) . . . . . – 0.5 V to 7 V
Power dissipation (see Note 3) . . . . . 1.25 W
Storage temperature range . . . . . – 65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Inputs may be taken to more negative voltages if the current is limited to 20 mA.
2. These outputs may not be taken more than 0.5 V above the V_{CC} pins.
3. Maximum power dissipation per package.

recommended operating conditions‡

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	2			V
V_{IL}	Low-level input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW			0.7	V
Receiver input bias voltage (see Note 5)			V_{SB} – 1		V_{SB} + 1	V
I_{OH}	High-level output current	RCVR, RCLK, $\overline{WFLT}$, $\overline{REDY}$			– 0.1	mA
I_{OL}	Low-level output current	$\overline{REDY}$, RCVR, $\overline{WFLT}$, RCLK,			1	mA
I_{CC}	Supply current	V_{CC} = 5.25 V		180	230	mA
T_A	Operating free-air temperature (see Note 4)		0		60	°C

‡ "Recommended Operating Conditions" indicate the conditions that must be met to ensure that the device will function as intended and meet the detailed electrical specifications. Unless otherwise noted, all electrical specifications apply for all recommended operating conditions. Voltages are measured with respect to the device ground pins. Currents into the device are considered to be positive.

NOTES: 4. Devices are tested in an environment in excess of 60°C to guarantee operation at 60°C. Case temperature should be maintained at or below 89°C.
5. V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as $V_{SB} = (V_{SBA} + V_{SBB})/2$, (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins will be approximately $V_{CC}/2$.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

TTL input

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 2.7 V			20	µA
I_{IL}	Low-level input current	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 0.4 V			– 0.4	mA
I_I	Input current at maximum input voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW	V_I = 7 V			100	µA
V_{IK}	Input clamp voltage	$\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$, SPSW DRVR, $\overline{DRVR}$	I_I = – 12 mA			– 1.5	V

TTL output (RCVR, RCLK, $\overline{REDY}$, and $\overline{WFLT}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 0.1 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.45	V
I_{OZH}	Off-state output current with high-level voltage applied	V_O = 2.7 V			± 100	µA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0.4 V			± 100	µA

receiver input (RCVINA and RCVINB)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rising input threshold voltage, V_{T+}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, (see Notes 5, 6, and 7)			35	mV
Falling input threshold voltage, V_{T-}	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, (see Notes 5, 6, and 7)	– 35†			mV
Asymmetry threshold voltage, (V_{T+} + V_{T-})	$V_{IC} = V_{SB}$, R4 = 2.49 kΩ, R_{tst} = 330 Ω, (see Notes 5, 6, and 7)	– 20†		20	mV
Rising input common mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330 Ω, R4 = 2.49 kΩ, (see Notes 5, 6, and 7)	– 30†		30	mV
Falling input common mode rejection [V_{T+} (@V_{SB} + 0.5 V) – V_{T+} (@V_{SB} – 0.5 V)]	R_{tst} = 330, R4 = 2.49 kΩ, (see Notes 5, 6, and 7)	– 30†		30	mV
Receiver input current	R_{tst} = 330 Ω, both inputs at V_{SB} (see Note 5)			± 25	μA
	R_{tst} = 330 Ω, Input under test at V_{SB} + 1.0 V Other input at V_{SB} – 1.0 V (see Note 5)	300		700	μA
	R_{tst} = 330 Ω, Input under test at V_{SB} – 1.0 V Other input at V_{SB} + 1.0 V (see Note 5)	–300		–700	μA
Equalizer bias current (EQUALA and EQUALB pins)	RCVINA and RCVINB open, EQUALA and EQUALB at 3 V	1.125		1.875	mA

† The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this data sheet for threshold voltages only.

NOTES: 5. V_{SB} is the self-bias voltage of the input pair RCVINA and RCVINB. It is defined as V_{SB} = (V_{SBA} +V_{SBB}) /2, (where V_{SBA} is the self-bias voltage of RCVINA; V_{SBB} is the self-bias voltage of RCVINB). The self-bias voltage of both pins will be approximately V_{CC}/2.
6. R_{tst} is a resistor connected between pins 43 and 44; it replaces R1, R2, and C1 (Figure 5).
7. V_{IC} is the common mode voltage applied to RCVINA and RCVINB.

transmitter

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current, on	DROUTA, DROUTB	$V_O = V_{CC}$, (see Note 8)	20		35	mA
Output current, off	DROUTA, DROUTB	V_O = 8 V, (see Note 8)			100	μA
Output current, off	DROUTA, DROUTB	$\overline{WRAP}$, = V_{IL}, V_O = 8 V			100	μA
I_{IH} High-level input current	DRVR, $\overline{DRVR}$	Input under test at 2.7 V. Other input at 0.40 V	100		700	μA
I_{IL} Low-level input current	DRVR, $\overline{DRVR}$	Input under test at 0.4 V. Other input at 2.70 V	–100		–700	μA

NOTE 8: Output not under test is loaded with 75 Ω to V_{CC}.

phantom driver (PHOUTA and PHOUTB)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	4.1			V
		I_{OH} = – 2 mA	3.8			V
I_{OS}	Short circuit output current	V_O = 0 V, $\overline{NSRT}$ = V_{IL}	– 4		– 20	mA
I_{OH}	High-level output current	$V_O = V_{CC}$, $\overline{NSRT}$ = V_{IH}			± 100	μA
I_{OZH}	Off-state output current with high-level voltage applied	$V_O = V_{CC}$, ENABLE = V_{IL}			± 100	μA
I_{OZL}	Off-state output current with low-level voltage applied	V_O = 0 V, ENABLE = V_{IL}			± 100	μA

wire fault ($\overline{WFLT}$) (see Notes 9 and 10)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phantom-normal condition	2.9 kΩ < R_{L1} < 5.5 kΩ, 2.9 kΩ < R_{L2} < 5.5 kΩ	2.4			V
Phantom-open condition	R_{L1} > 9.9 kΩ, and 2.9 kΩ > R_{L2} < 5.5 kΩ, or R_{L2} > 9.9 kΩ, and 2.9 kΩ < R_{L1} < 5.5 kΩ			0.45	V
Phantom-short condition	R_{L1} < 0.1 kΩ, and 2.9 kΩ < R_{L2} < 5.5 kΩ, or R_{L2} < 0.1 kΩ, and 2.9 kΩ < R_{L1} < 5.5 kΩ			0.45	V

NOTES: 9. The wire-fault logic will recognize a load condition corresponding to greater than 9.9 kΩ to ground as an open-circuit fault, but will not recognize a load condition less than 5.5 kΩ to ground as an open. The wire-fault logic will recognize a load condition corresponding to less than 100 Ω to ground as a short-circuit fault, but will not recognize a load condition corresponding to greater than 2.9 kΩ to ground as a short. Figure 6 illustrates this with R_{L1} connected from PHOUTA to ground and R_{L2} connected from PHOUTB to ground.

10. R_{L1} is connected from pin 27 to ground; R_{L2} is connected from pin 29 to ground.

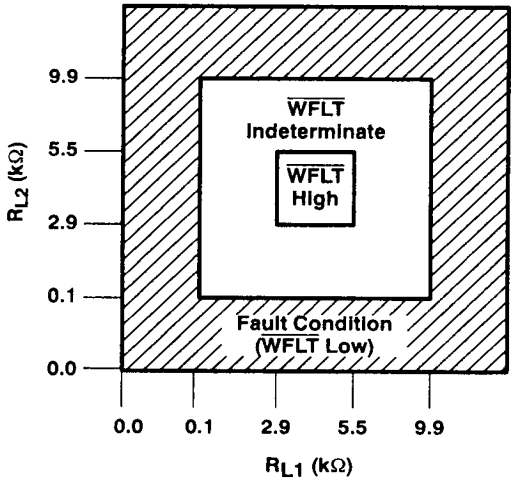

Figure 6. Wire-Fault Pin Test

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} Supply current	V_{CC} = 5.25 V (see Figure 7)		180	230	mA

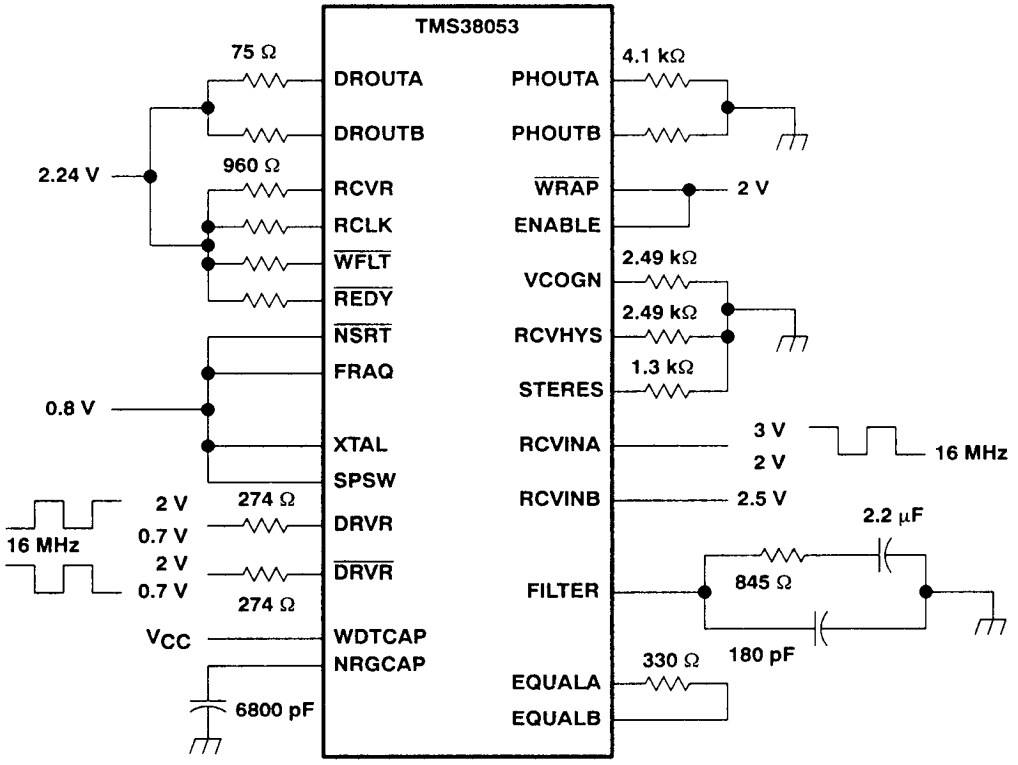

Figure 7. I_{CC} Test Circuit

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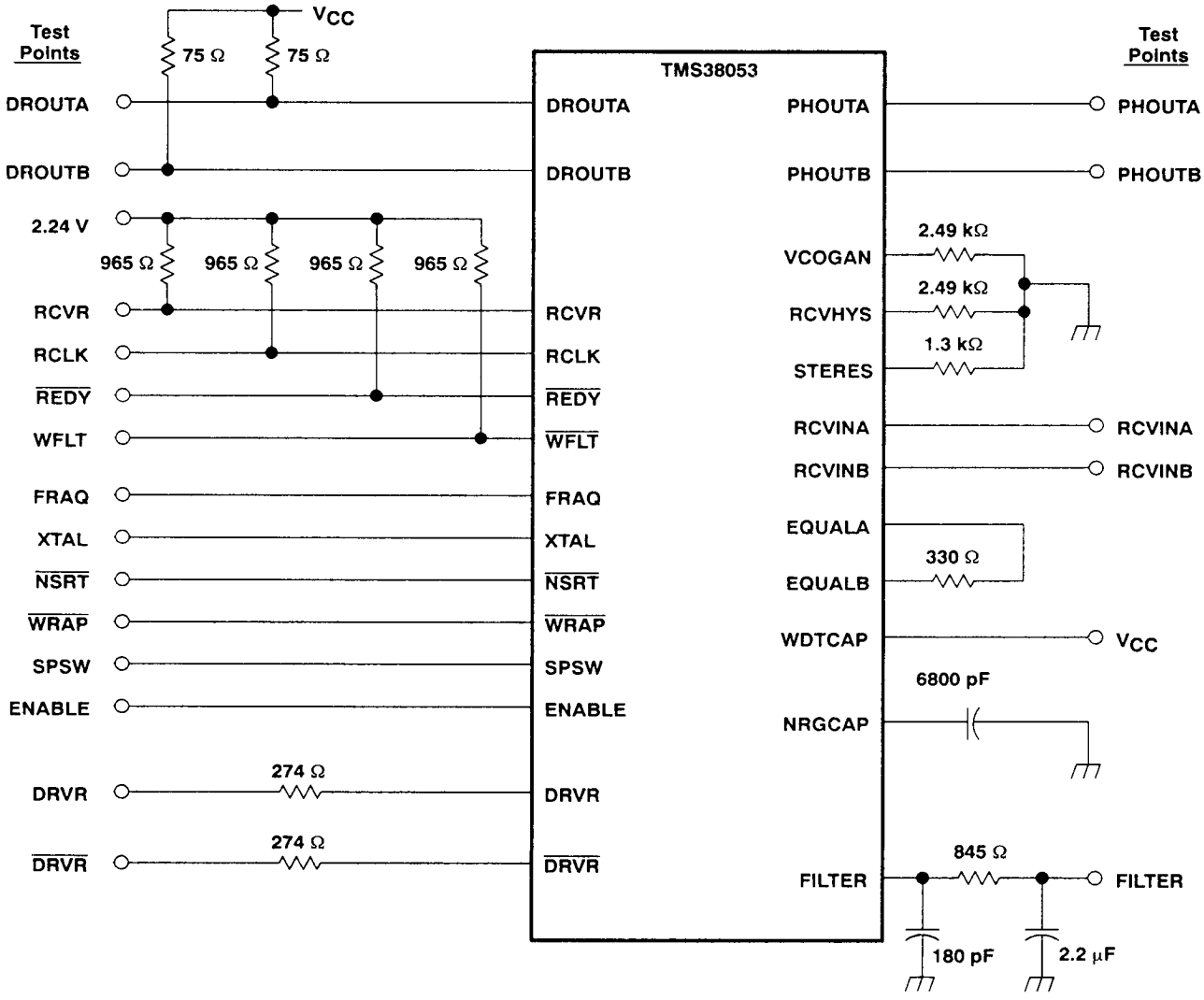

Figure 8. AC Test Circuit for TMS38053

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

transmitter (see Figures 8 and 9)

NO.	PARAMETER		TEST CONDITIONS	MIN TYP MAX	UNIT
1	$t_{sk(DRVR)}$	Delay from DRVR edge (1.5 V) to following $\overline{DRVR}$ edge (1.5 V)		(see Note 11)	
2	$t_{d(DROUTA)H}$	Delay from DRVR falling edge (1.5 V) to DROUTA rising edge (midpoint)		(see Note 11)	
3	$t_{d(DROUTA)L}$	Delay from DRVR rising edge (1.5 V) to DROUTA falling edge (midpoint)		(see Note 11)	
4	$t_{d(DROUTB)H}$	Delay from DRVR falling edge (1.5V) to DROUTB falling edge (midpoint)		(see Note 11)	
5	$t_{d(DROUTB)L}$	Delay from DRVR rising edge (1.5 V) to DROUTB rising edge (midpoint)		(see Note 11)	
6	DROUTA/DROUTB Skew	$t_{d(DROUTA)H} - t_{d(DROUTB)L}$	$t_{sk(DRVR)} = -1$ ns	± 3	ns
		$t_{d(DROUTA)L} - t_{d(DROUTB)H}$	$t_{sk(DRVR)} = +1$ ns	± 3	
7	DROUTA/DROUTB Assymetry	$\frac{t_{d(DROUTA)L} + t_{d(DROUTB)H}}{2} - \frac{t_{d(DROUTA)H} + t_{d(DROUTB)L}}{2}$	$t_{sk(DRVR)} = -1$ ns	± 2	ns
			$t_{sk(DRVR)} = +1$ ns	± 2	

NOTE 11: This parameter is not tested to a minimum or a maximum but is measured and used as a component required for parameters 6 and 7.

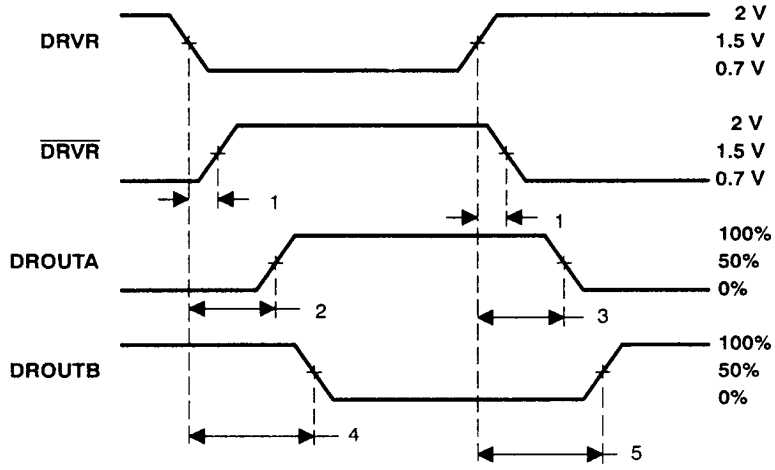

Figure 9. Skew and Asymmetry from DRVR and $\overline{DRVR}$ to DROUTA and DROUTB

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

RCLK and RCVR timing (see Figures 8 and 10)

NO.	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
8	$t_{w(RCLK)L}$	Pulse duration, RCLK low	4 Mbps, $t_{per(RCLK)}$ = 115.0 ns (see Note 12)	46			ns
			16 Mbps, $t_{per(RCLK)}$ = 30 ns (see Note 12)	10			
9	$t_{w(RCLK)H}$	Pulse duration, RCLK high	4 Mbps, $t_{per(RCLK)}$ = 115.0 ns (see Note 12)	35			ns
			16 Mbps, $t_{per(RCLK)}$ = 30 ns (see Note 12)	8			
10	$t_{su(RCVR)}$	Setup time, RCVR valid to RCLK rising edge (1.5-V point)	$t_{per(RCLK)}$ = 31.25 ns	10			ns
11	$t_{h(RCVR)}$	Hold time, RCVR valid after RCLK rising edge (1.5-V point)	$t_{per(RCLK)}$ = 31.25 ns	2			ns
12	$t_{per(RCLK)}$	Period of RCLK (see Note 13)	4 Mbps		125		ns
			16 Mbps		31.25		

NOTES: 12. The pulse duration high and low of RCLK is tested at a frequency in excess of nominal to ensure correct operation during brief periods where lock is lost.

13. This parameter is not tested. The typical value shown is that for the recovered clock from an IEEE 802.5 Token Ring.

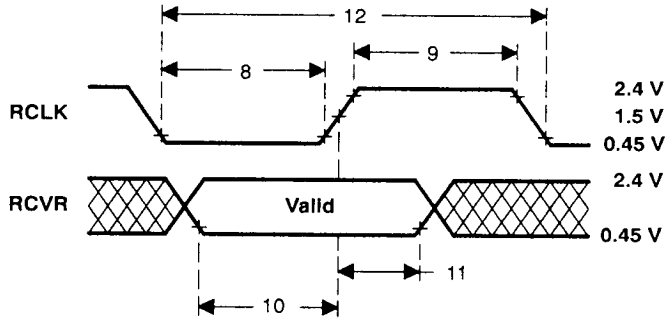

Figure 10. RCLK and RCVR Timing Diagram

loop parameters (see Figures 8 and 11)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Filter voltage low	f = 29.6 MHz (see Note 14)	1.9			V
Filter voltage high	f = 34.8 MHz (see Note 14)			3.1	V
VCO gain (G_O)	f1 = 28.6 MHz, f2 = 36.4 MHz (see Note 15)	11.90		16.10	MHz / V
Phase detector gain (G_d)	$I_{(FILTER)1}$ = +60 μA, $I_{(FILTER)2}$ = – 60 μA, f = 32 MHz (see Note 16)	6.16		8.33	μA / ns

NOTES:14. The frequency f is applied to the XTAL input pin, with FRAQ high, as shown in Figure 11. The voltage at the FILTER pin is measured after lock is achieved.

15. A frequency of f1 is applied to the XTAL with FRAQ high. After lock is achieved, the voltage at the FILTER pin is measured (V1). This is then repeated using f2 and measuring V2. VCO gain is calculated as (f2-f1)/(V2-V1). The result is in Hz / V (see "External Filter" section).

16. The circuit of Figure 8 is used to measure phase detector gain with $I_{(FILTER)}$ injected at the filter test point. Figure 12 shows the relevant timing. With the TMS38053 in phase lock, the propagation delay (t_p) between RCVINA positive transition and RCLK negative transition is measured. A value t_{p1} is seen when $I_{(FILTER)} = I_{(FILTER)1}$, and a value of t_{p2} is seen when $I_{(FILTER)} = I_{(FILTER)2}$. The phase detector gain is then calculated as $(I_{(FILTER)2} - I_{(FILTER)1}) \div (t_{p1} - t_{p2})$. The result is in μA/ns (see "External Filter" section).

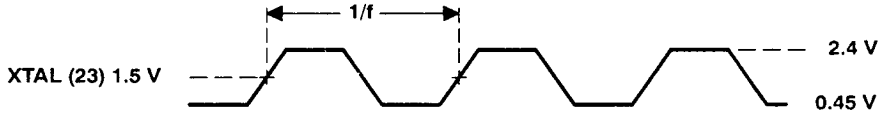

Figure 11. VCO Gain and Filter Voltage Test Timing

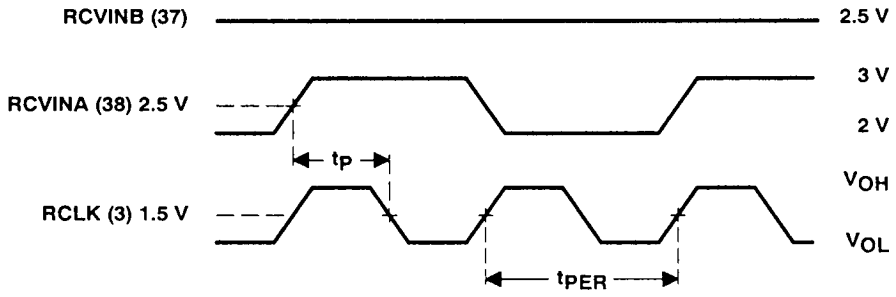

Figure 12. Phase Detector Gain Test Timing

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data recovery timing (see Figures 8 and 13, and Note 17)

NO.	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
13	t_{se} Static timing error from voltage midpoint of RCVINA edge to midpoint to RCVINA pulse	4 Mbps, f = 8 MHz			± 15	ns
		16 Mbps, f = 32 MHz			± 2.8	

NOTE 17: The TMS38053 is phase-locked to a RCVINA waveform as shown in Figure 13, with RCVINB biased to 2.5 V. The RCVR output pin is monitored for proper data being latched. Then for one pulse, shorten the time at which RCVINA's negative transition occurs. Check RCVR if the short pulse was latched. Re-stabilize the VCO with normal pulses. Input another short pulse. Continue this routine, while gradually shortening the pulse, until the data is not latched. The time between this negative transition and the midpoint of the original pulse's up-time is t_{se}. Repeat this procedure using all of the RCVINA waveforms shown.

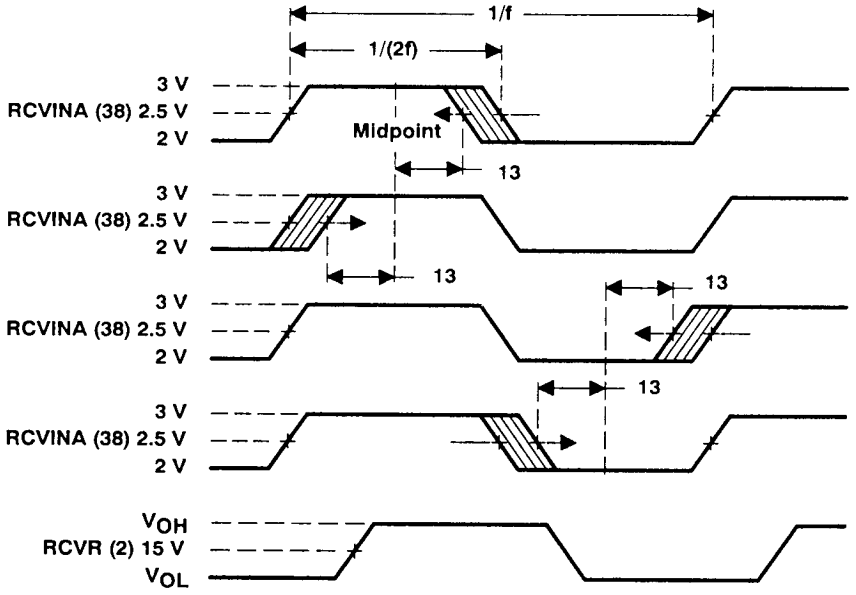

Figure 13. TMS38053 Phase-Locked to RCVINA

energy detect ($\overline{\text{REDY}}$) (see Figure 8 and Note 18)

NO.	PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
14	$t_{DL1(REDY)}$	Delay time, FRAQ transition to $\overline{\text{REDY}}$ low again	Data transition density = 100% (see Figure 14)	5			µs
			Data transition density = 33% (see Figure 14)	30		180	
15	$t_{DH2(REDY)}$	Delay time, data loss to $\overline{\text{REDY}}$ high	Data transition density changes 100% to 2.5% (see Figure 15)	20		100	µs

NOTE 18: The transition density of the incoming data is the percentage of transitions of the incoming data as compared with the maximum possible number of transitions. For a string of Manchester-encoded 0 data, 100% transition density is, therefore, a 16-MHz signal at a 16-Mbps data transmission rate.

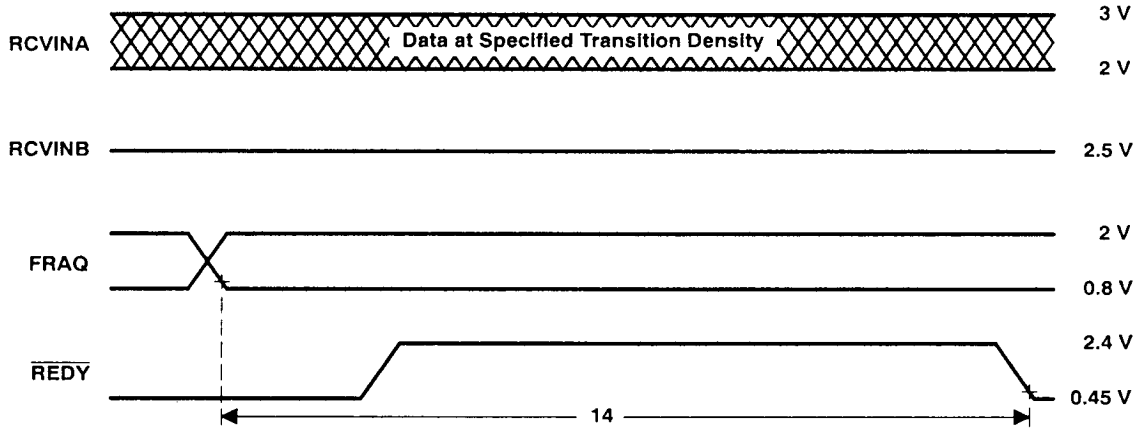

Figure 14. Timing Waveforms for Energy Detect, FRAQ to $\overline{\text{REDY}}$ Timing

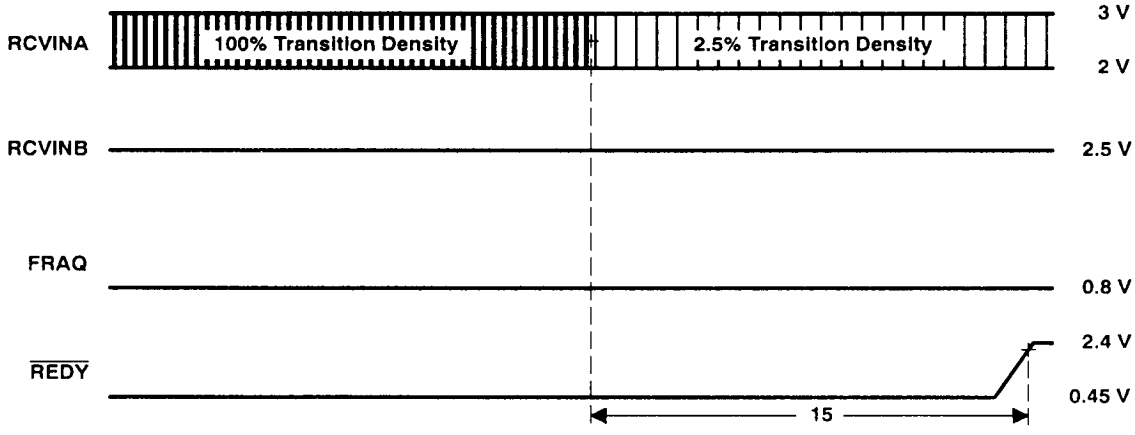

Figure 15. Timing Waveforms for Energy Detect to Energy Loss Timing

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watchdog timer(see Figure 16, and Notes 10, 19, 20, 21)

NO.	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
16	$t_{d(WDT)H}$ Watchdog timer expiration time	C_{wdt} = 1.5 μF, RL1 = RL2 = 2.9 kΩ	21		50	ms

NOTES: 10. R_{L1} is connected from pin 27 to ground; R_{L2} is connected from pin 29 to ground.

19. To enable the phantom driver signals, $\overline{NRST}$ must be toggled high with a minimum 20 ms period (50-Hz repetition rate). Phantom driver signals are assured to be disabled if $\overline{NRST}$ does not toggle for 50 ms. The TMS380C16 software assures a minimum 20-ms period toggling rate for the insertion condition.
20. Pulse duration high of $\overline{NSRT}$ is not critical, but it is recommended that it be at least 125 ns.
21. C_{wdt} is the capacitor connected from WDTCAP (pin 25) to GND.

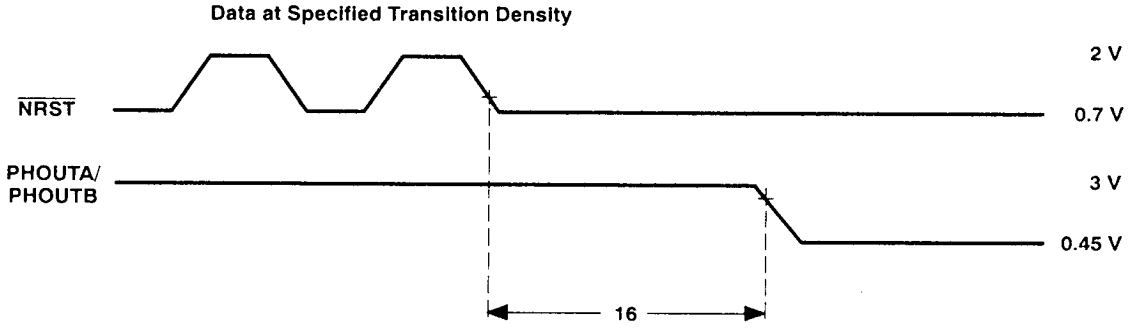
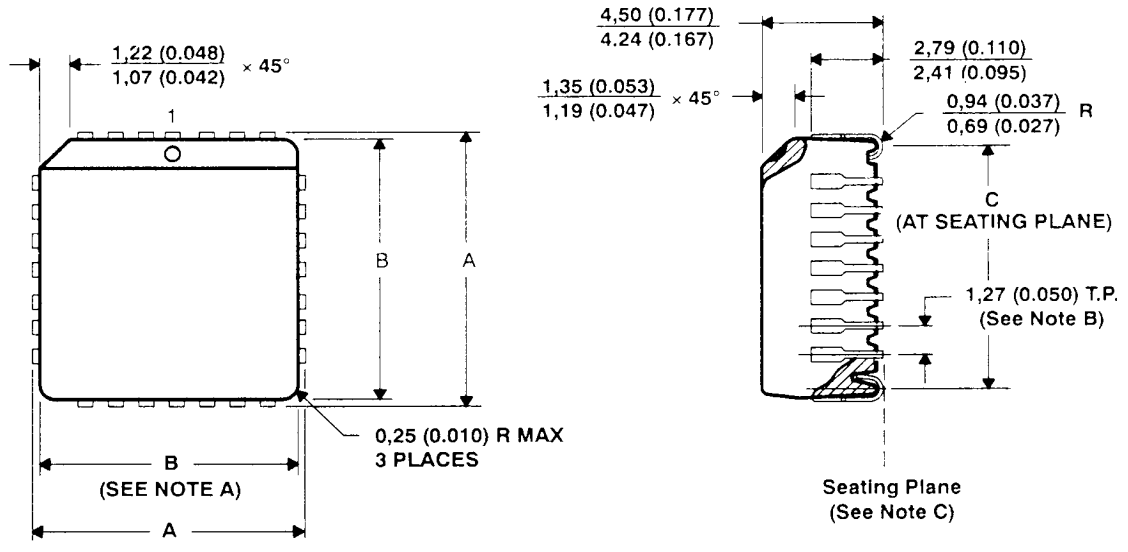


Figure 16. Watchdog Timer Expiration Time Wave Forms

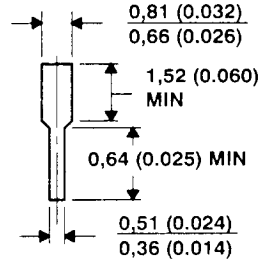
MECHANICAL DATA

plastic-leaded chip carrier package (FN suffix)

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.



JEDEC OUTLINE	NO OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
MO-047AA	20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
MO-047AB	28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
MO-047AC	44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15.49 (0.610)	16,00 (0.630)
MO-047AE	68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
MO-047AF	84	30,10 (1.185)	30,35 (1.195)	29,41 (0.150)	21,41 (1.158)	27,69 (0.090)	28,70 (1.130)



LEAD DETAIL

All dimensions and notes for the specified JEDEC outline apply

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).