PC133 144pin Unbuffered SDRAM SODIMM
SPD Specification(Intel Gerber 1.2ver. base)

Rev. 0.0

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• Revision History

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• SPD Spec List

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M464S0424DT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 4MX64
•Composition : 4MX16 *4
•Used component part # : K4S641632D-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	9Bh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S0424ET2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 4MX64
•Composition : 4MX16 *4
•Used component part # : K4S641632E-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	9Bh	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	4	34h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	E	45h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	E-die (6th Gen.)	45h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S0824DT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8MX64
•Composition : 4MX16 *8
•Used component part # : K4S641632D-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	9Ch	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	D	44h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	D-die (5th Gen.)	44h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S0824ET2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8MX64
•Composition : 4MX16 *8
•Used component part # : K4S641632E-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	8	08h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 32MB	08h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	9Ch	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	8	38h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	E	45h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	E-die (6th Gen.)	45h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S0924BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8Mx64
•Composition : 8Mx16 *4
•Used component part # : K4S281632B-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	A4h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	9	39h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S0924CT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 8Mx64
•Composition : 8Mx16 *4
•Used component part # : K4S281632C-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	A4h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	9	39h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S1724BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64
•Composition : 8MX16 *8
•Used component part # : K4S281632B-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	A5h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S1724CT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64
•Composition : 8MX16 *8
•Used component part # : K4S281632C-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 4K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 64MB	10h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	A5h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S1654AT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64
•Composition : 16MX16 *4
•Used component part # : K4S561632A-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 8K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	B7h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S1654BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 16MX64
•Composition : 16MX16 *4
•Used component part # : K4S561632B-TL75/TC75
•# of rows in module : 1 row
•# of banks in component : 4 banks
•Feature : 1,000 mil height & double sided
•Refresh : 8K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	B7h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	8Dh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S3254AT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 32MX64
•Composition : 16MX16 *8
•Used component part # : K4S561632A-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 8K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	B8h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	..... Manufacturer part # (Module depth)	2	32h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	A	41h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	A-die (2nd Gen.)	41h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.
6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.

M464S3254BT2-L75/C75(Intel SPD 1.2B ver. based)

•Organization : 32MX64
•Composition : 16MX16 *8
•Used component part # : K4S561632B-TL75/TC75
•# of rows in module : 2 rows
•# of banks in component : 4 banks
•Feature : 1,250 mil height & double sided
•Refresh : 8K/64ms
•**Contents** :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	2 Rows of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	Intel 1.2B	12h	
63	Checksum for bytes 0 ~ 62	-	B8h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	4	34h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	3	33h	
80	..... Manufacturer part # (Module depth)	2	32h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5	35h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	B	42h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L | C	4Ch | 43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)	42h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	-	64h	6
127	Reserved	Detailed PC100 Information	CDh	6
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
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