Freescale Semiconductor
Data Sheet: Technical Data

DSP56374
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DSP56374 Data Sheet

1 Overview

The DSP56374 is a high-density CMOS device with 3.3 V inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

For software or simulation models (for example, IBIS files), contact sales or go to www.freescale.com.

The DSP56374 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56374 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Semiconductor, Inc. Symphony™ DSP family, as shown in Figure 1. Significant architectural enhancements include a barrel shifter, 24-bit addressing, and direct memory access

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(DMA). The DSP56374 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock.

Data Sheet Conventions

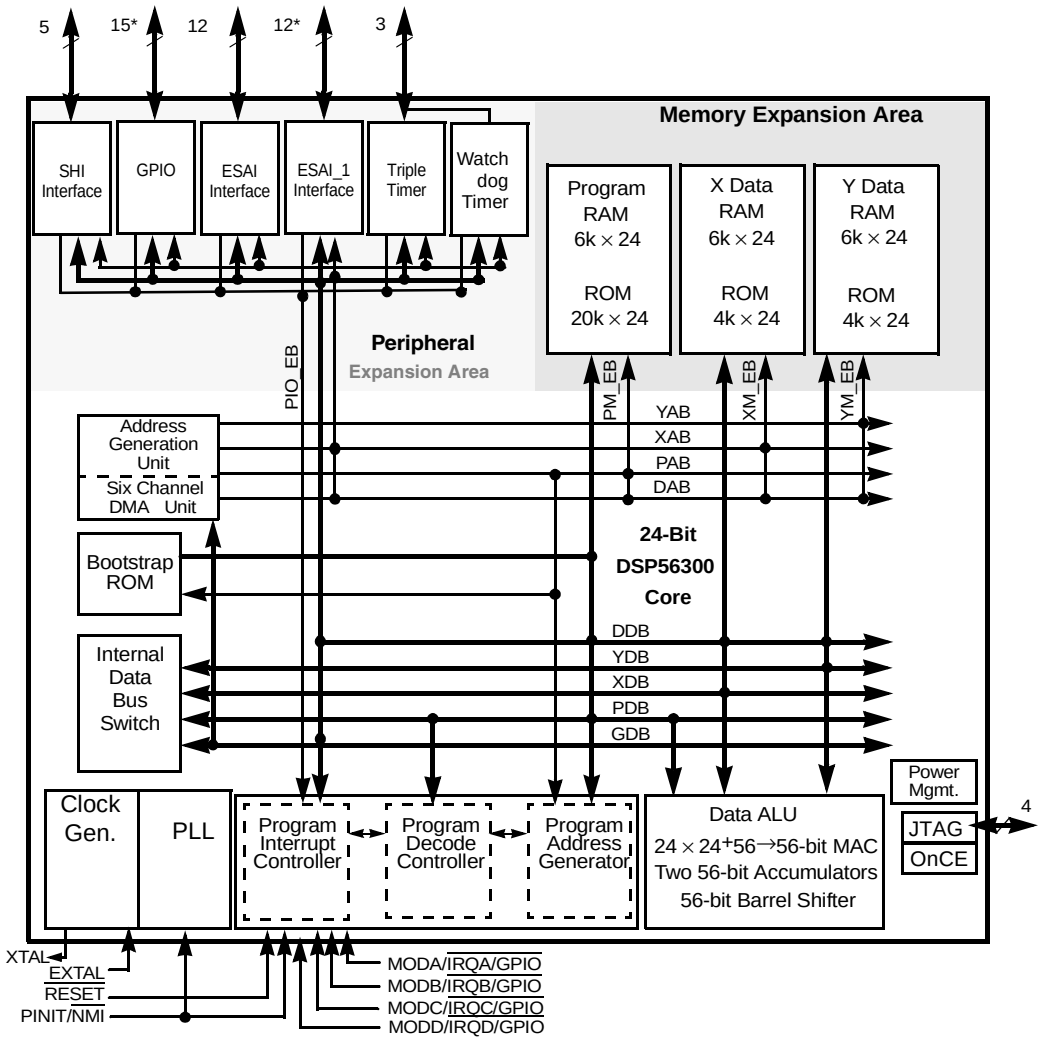
This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/ Symbol	Logic State	Signal State	Voltage*
PIN	True	Asserted	V_{IL} / V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
PIN	True	Asserted	V_{IH} / V_{OH}
PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



* ESAI_1 and dedicated GPIO pins are not available in the 52-pin package.

Figure 1. DSP56374 Block Diagram

2 Features

2.1 DSP56300 Modular Chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at an internal logic supply (QVDDL) of 1.25 V
- Object Code Compatible with the 56K core
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter;16 bit arithmetic support
- Program Control with position independent code support

- Six-channel DMA controller
- Provides a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31), PLL feedback multiplier (2 or 4), Output divide factor (1, 2, or 4) and a power-saving clock divider (2^i: i = 0 to 7) to reduce clock noise
- Internal address tracing support and OnCE for Hardware/Software debugging
- JTAG port, supporting boundary scan, compliant to IEEE 1149.1
- Very low-power CMOS design, fully static design with operating frequencies down to DC
- STOP and WAIT low-power standby modes

2.2 On-chip Memory Configuration

- 6Kx24 Bit Y-Data RAM and 4Kx24 Bit Y-Data ROM
- 6Kx24 Bit X-Data RAM and 4Kx24 Bit X-Data ROM
- 20Kx24 Bit Program and Bootstrap ROM including a PROM patching mechanism
- 6Kx24 Bit Program RAM.
- Various memory switches are available. See memory table below.

Table 1. DSP56374 Memory Switch Configurations

Bit Settings			Memory Sizes (24-bit words)					
MSW1	MSW0	MS	Prog RAM	X Data RAM	Y Data RAM	Prog ROM	X Data ROM	Y Data ROM
X	X	0	6K	6K	6K	20K	4K	4K
0	0	1	2K	10K	6K	20K	4K	4K
0	1	1	4K	8K	6K	20K	4K	4K
1	0	1	8K	4K	6K	20K	4K	4K
1	1	1	10K	4K	4K	20K	4K	4K

2.3 Peripheral Modules

- Enhanced Serial Audio Interface (ESAI): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I^2S, Sony, AC97, network, and other programmable protocols.
- Enhanced Serial Audio Interface I (ESAI_1): up to 4 receiver pins and up to 6 transmitter pins, master or slave. I^2S, Sony, AC97, network and other programmable protocols. *Note: Available in the 80-pin package only.*
- Serial Host Interface (SHI): SPI and I^2C protocols, 10-word receive FIFO, support for 8, 16, and 24-bit words. Three noise reduction filter modes.
- Triple Timer module (TEC)
- Most pins of unused peripherals may be programmed as GPIO pins. Up to 47 pins can be configured as GPIO on the 80 pin package and 20 pins on the 52 pin package.

- Hardware Watchdog Timer

2.4 Packages

80-pin and 52-pin plastic LQFP packages.

3 Documentation

Table 2 lists the documents that provide a complete description of the DSP56374 and are required to design properly with the part. Documentation is available from a local Freescale Semiconductor, Inc. (formerly Motorola) distributor, semiconductor sales office, Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 2. DSP56374 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56374 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56374UM/D
DSP56374 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56374
DSP56374 Product Brief	Brief description of the chip	DSP56374PB/D

4 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 3.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 3. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals[1]	Detailed Description
Power (V_{DD})		11	Table 15
Ground (GND)		9	Table 5
Scan Pins		1	Table 6
Clock and PLL		3	Table 7
Interrupt and mode control	Port H[2]	5	Table 8
SHI	Port H[2]	5	Table 9
ESAI	Port C[4]	12	Table 10
ESAI_1	Port E[5]	12	Table 11

Table 3. DSP56374 Functional Signal Groupings (continued)

Functional Group		Number of Signals[1]	Detailed Description
Dedicated GPIO	Port G[3]	15	Table 12
Timer		3	Table 13
JTAG/OnCE Port		4	Table 14

Note:
1 Pins are not 5 V. tolerant unless noted.
2 Port H signals are the GPIO port signals which are multiplexed with the MOD and $\overline{\text{HREQ}}$ signals.
3 Port G signals are the dedicated GPIO port signals.
4 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
5 Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.

4.1 Power

Table 4. Power Inputs

Power Name	Description
PLLA_VDD (1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND. PLLA_VDD requires a filter as shown in Figure 1 and Figure 2 below. See the DSP56374 technical data sheet for additional details.
PLLP_VDD(1)	PLL Power— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_VDD (1)	PLL Power— The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_VDD (4)	Core Power—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
IO_VDD (80-pin 4) (52-pin 3)	SHI, ESAI, ESAI_1, WDT and Timer I/O Power —The voltage (3.3 V) should be well-regulated, and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, WDT and Timer I/O. The user must provide adequate external decoupling capacitors.

4.2 Ground

Table 5. Grounds

Ground Name	Description
PLLA_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLA_VDD and PLLA_GND.

Table 5. Grounds (continued)

Ground Name	Description
PLLP_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLP_VDD and PLLP_GND.
PLLD_GND(1)	PLL Ground—The PLL ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors between PLLD_VDD and PLLD_GND.
CORE_GND(4)	Core Ground—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND(2)	SHI, ESAI, ESAI_1, WDT and Timer I/O Ground—IO_GND is the ground for the SHI, ESAI, ESAI_1, WDT and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

4.3 SCAN

Table 6. SCAN Signals

Signal Name	Type	State During Reset	Signal Description
SCAN	Input	Input	SCAN—Manufacturing test pin. This pin must be connected to ground.

4.4 Clock and PLL

Table 7. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	External Clock / Crystal Input—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
XTAL	Output	Chip Driven	Crystal Output—Connects the internal Crystal Oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.
PINIT/$\overline{\text{NMI}}$	Input	Input	PLL Initial/Nonmaskable Interrupt—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de-assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to the internal system clock. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is de-asserted, these inputs are hardware interrupt request lines.

Table 8. Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	MODA Input	Mode Select A/External Interrupt Request A—MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is de-asserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH0	Input, output, or disconnected		Port H0—When the MODA/IRQA is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODB/IRQB	Input	MODB Input	Mode Select B/External Interrupt Request B—MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH1	Input, output, or disconnected		Port H1—When the MODB/IRQB is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODC/IRQC	Input	MODC Input	Mode Select C/External Interrupt Request C—MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 8. Interrupt and Mode Control (continued)

Signal Name	Type	State during Reset	Signal Description
PH2	Input, output, or disconnected		Port H2—When the MODC/IRQC is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
MODD/$\overline{\text{IRQD}}$	Input	MODD Input	Mode Select D/External Interrupt Request D—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. This pin can also be programmed as GPIO. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is de-asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.
PH3	Input, output, or disconnected		Port H3—When the MODD/IRQD is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected.
RESET	Input	Input	Reset—$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is de-asserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.6 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 9. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	SPI Serial Clock—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		I^2C Serial Clock—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through an external pull-up resistor according to the I^2C specifications. This signal is tri-stated during hardware, software, and individual reset. This pin has an internal pull up resistor. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	SPI Master-In-Slave-Out—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is de-asserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		I^2C Data and Acknowledge—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 9. Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
MOSI	Input or output	Tri-stated	SPI Master-Out-Slave-In—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		I^2C Slave Address 0—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for I^2C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^2C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This pin has an internal pull up resistor. This input is 5 V tolerant.
SS	Input	Ignored Input	SPI Slave Select—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept de-asserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is de-asserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		I^2C Slave Address 2—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for the I^2C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^2C master mode. This pin has an internal pull up resistor. This input is 5 V tolerant.
HREQ	Input or Output	Tri-stated	Host Request—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and de-asserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This pin can also be programmed as GPIO.
PH4	Input, output, or disconnected		Port H4—When $\overline{HREQ}$ is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.

4.7 Enhanced Serial Audio Interface

Table 10. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected		Port C2—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.
HCKT	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected		Port C5—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This pin has an internal pull up resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR	Input or output	GPIO disconnected	Frame Sync for Receiver—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected		Port C1—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
FST	Input or output	GPIO disconnected	Frame Sync for Transmitter—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		Port C4—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	Receiver Serial Clock—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		Port C0—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	Transmitter Serial Clock—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		Port C3—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5	Output	GPIO disconnected	Serial Data Output 5—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		Serial Data Input 0—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		Port C6—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	Serial Data Output 4—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		Serial Data Input 1—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		Port C7—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		Port C8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 10. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		Serial Data Input 3—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		Port C9—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1	Output	GPIO disconnected	Serial Data Output 1—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		Port C10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	Serial Data Output 0—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		Port C11—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.8 Enhanced Serial Audio Interface_1

Table 11. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	High Frequency Clock for Receiver—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		Port E2—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT_1	Input or output	GPIO disconnected	High Frequency Clock for Transmitter—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		Port E5—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	Frame Sync for Receiver_1—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected		Port E1—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
FST_1	Input or output	GPIO disconnected	Frame Sync for Transmitter_1—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).
PE4	Input, output, or disconnected		Port E4—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	Receiver Serial Clock_1—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected		Port E0—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SCKT_1	Input or output	GPIO disconnected	Transmitter Serial Clock_1—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected		Port E3—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO5_1	Output	GPIO disconnected	Serial Data Output 5_1—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		Serial Data Input 0_1—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		Port E6—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant
SDO4_1	Output	GPIO disconnected	Serial Data Output 4_1—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		Serial Data Input 1_1—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		Port E7—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		Port E8—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2_1	Output	GPIO disconnected	Serial Data Output 2—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		Serial Data Input 3—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		Port E9—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO1_1	Output	GPIO disconnected	Serial Data Output 1—SDO1_1 is used to transmit data from the TX1 serial transmit shift register.
PE10	Input, output, or disconnected		Port E10—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1	Output	GPIO disconnected	Serial Data Output 0—SDO0_1 is used to transmit data from the TX0 serial transmit shift register.
PE11	Input, output, or disconnected		Port E11—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

4.9 Dedicated GPIO-Port G

Table 12. Dedicated GPIO-Port G Signals

Signal Name	Type	State During Reset	Signal Description
PG0	Input, output, or disconnected	GPIO disconnected	Port G0—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG1	Input, output, or disconnected	GPIO disconnected	Port G1—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG2	Input, output, or disconnected	GPIO disconnected	Port G2—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG3	Input, output, or disconnected	GPIO disconnected	Port G3—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG4	Input, output, or disconnected	GPIO disconnected	Port G4—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG5	Input, output, or disconnected	GPIO disconnected	Port G5—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG6	Input, output, or disconnected	GPIO disconnected	Port G6—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG7	Input, output, or disconnected	GPIO disconnected	Port G7—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG8	Input, output, or disconnected	GPIO disconnected	Port G8—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

Table 12. Dedicated GPIO-Port G Signals (continued)

Signal Name	Type	State During Reset	Signal Description
PG9	Input, output, or disconnected	GPIO disconnected	Port G9—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG10	Input, output, or disconnected	GPIO disconnected	Port G10—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG11	Input, output, or disconnected	GPIO disconnected	Port G11—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG12	Input, output, or disconnected	GPIO disconnected	Port G12—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG13	Input, output, or disconnected	GPIO disconnected	Port G13—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant
PG14	Input, output, or disconnected	GPIO disconnected	Port G14—This signal is individually programmable as input, output, or internally disconnected. Internal Pull down resistor. This input is 5 V tolerant

4.10 Timer

Table 13. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	Timer 0 Schmitt-Trigger Input/Output—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input. Internal Pull down resistor. This input is 5 V tolerant
TIO1	Input or Output	Watchdog Timer Output	Timer 1 Schmitt-Trigger Input/Output—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input.
WDT	Output		WDT—When this pin is configured as a hardware watchdog timer pin, this signal is asserted low when the hardware watchdog timer counts down to zero. Internal Pull down resistor. This input is 5 V tolerant
TIO2	Input or Output	PLOCK Output	Timer 2 Schmitt-Trigger Input/Output—When timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer control/status register (TCSR2). If TIO2 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input .

Table 13. Timer Signal (continued)

Signal Name	Type	State during Reset	Signal Description
PLOCK	Output		PLOCK—When this pin is configured as a PLL lock pin, this signal is asserted high when the on-chip PLL enabled and locked and de-asserted when the PLL enabled and unlocked. This pin is also asserted high when the PLL is disabled. Internal Pull down resistor. This input is 5 V tolerant

4.11 JTAG/OnCE Interface

Table 14. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	Test Clock—TCK is a test clock input signal used to synchronize the JTAG test logic. Internal Pull up resistor. This input is 5 V tolerant.
TDI	Input	Input	Test Data Input—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	Test Data Output—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	Test Mode Select—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK. Internal Pull up resistor. This input is 5 V tolerant.

5 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

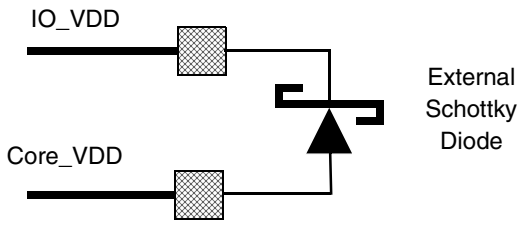
Table 15. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	−0.3 to + 1.6	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	−0.3 to + 4.0	V
Maximum CORE_VDD power supply ramp time[4]	Tr	10	ms
All "5.0V tolerant" input voltages	V_{IN}	GND − 0.3 to 6V	V
Current drain per pin excluding V_{DD} and GND(Except for pads listed below)	I	12	mA
SCK_SCL	I_{SCK}	16	mA
TDO	I_{JTAG}	24	ma
Operating temperature range[3]	T_J	80 LQFP = 105 52 LQFP = 110	°C
Storage temperature	T_{STG}	−55 to +125	°C
ESD protected voltage (Human Body Model)		2000	V
ESD protected voltage (Machine Model)		200	V

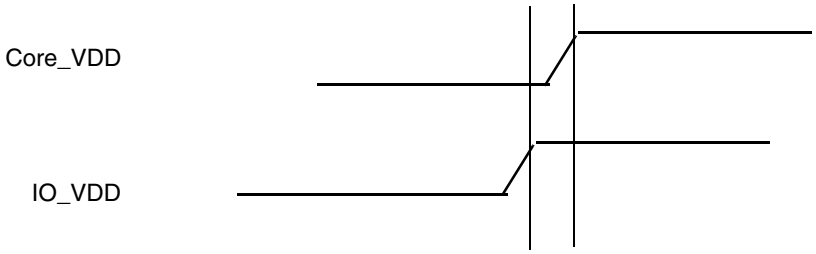
Note:
1 GND = 0 V, T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), CL = 50pF
2 Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3 Operating temperature qualified for automotive applications. $T_J = T_A + \theta_{JA}$ x Power. Variables used were Core Current = 100 mA, I/O Current = 60 mA, Core Voltage = 1.3 V, I/O Voltage = 3.46 V, T_A = 85°C
4 If the power supply ramp to full supply time is longer than 10 ms, the POR circuitry will not operate correctly, causing erroneous operation.

6 Power Requirements

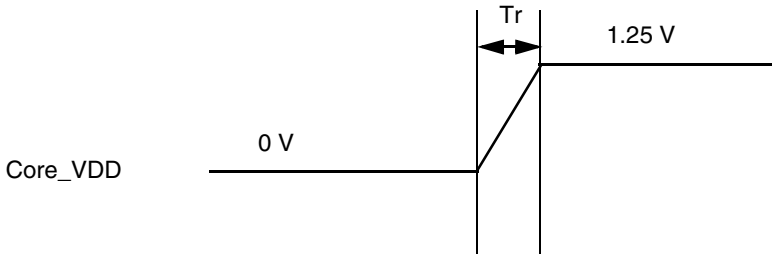
To prevent high current conditions due to possible improper sequencing of the power supplies, the connection shown below is recommended to be made between the DSP56374 IO_VDD and Core_VDD power pins.



To prevent a high current condition upon power up, the IO_VDD must be applied ahead of the Core_VDD as shown below if the external Schottky is not used.



For correct operation of the internal power on reset logic, the Core_VDD ramp rate (Tr) to full supply must be less than 10 ms. This is shown below.



7 Thermal Characteristics

Table 16. Thermal Characteristics

Characteristic	Symbol	LQFP Values	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	$R_{\theta JA}$ or θ_{JA}	68 (52 LQFP) 50 (80 LQFP)	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	17 (52 LQFP) 11 (80 LQFP)	°C/W

Note:
1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

8 DC Electrical Characteristics

Table 17. DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (Core_VDD) • PLL (PLLD_VDD)	V_{DD}	1.2	1.25	1.3	V
Supply voltages • I/O (IO_VDD) • PLL (PLLP_VDD) • PLL (PLLA_VDD)	V_{DDIO}	3.14	3.3	3.46	V
Input high voltage • All pins	V_{IH}	2.0	—	V_{IO_VDD}+2V	V
Note: All 3.3-V supplies must rise prior to the rise of the 1.25-V supplies to avoid a high current condition and possible system damage.					
Input low voltage • All pins	V_{IL}	–0.3	—	0.8	V
Input leakage current	I_{IN}	—	—	± 84	µA
Clock pin Input Capacitance (EXTAL)	C_{IN}		4.7		pF
High impedance (off-state) input current (@ 3.46V)	I_{TSI}	–10	—	84	µA
Output high voltage • I_{OH} = -5 mA • XTAL Pin I_{OH} = -10mA	V_{OH}	2.4	—	—	V
Output low voltage • I_{OL} = 5 mA • XTAL Pin I_{OL} = 10 mA	V_{OL}	—	—	0.4	V
Internal supply current[1] (core only) at internal clock of 150 MHz • In Normal mode	I_{CCI}	—	65	100	mA
• In Wait mode	I_{CCW}	—	16	—	mA
• In Stop mode[2]	I_{CCS}	—	1.2	—	mA
Input capacitance	C_{IN}	—	—	10	pF

Note:

[1] The Current Consumption section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.25V, V_{DD_IO} = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.30V, $V_{IO\_VDD)}$ = 3.46V at T_J = 115°C.

[2] In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

9 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56374 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 1.0 V and 1.8 V, respectively.

10 Internal Clocks

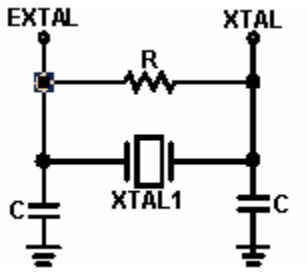
Table 18. INTERNAL CLOCKS[1]

No.	Characteristics	Symbol	Min	Typ	Max	Unit	Condition
1	Comparison Frequency	Fref	5	—	20	MHz	Fref = FIN/NR
2	Input Clock Frequency	FIN	Fref*NR				NR is input divider value
3	Output clock Frequency (with PLL enabled)[2,3]	FOUT Tc	75 13.3	(Ef × MF x FM)/ (PDF × DF x OD)	150	MHz ns	FOUT=FVCO/NO where NO is output divider value
4	Output clock Frequency (with PLL disabled)[2,3]	FOUT	—	Ef	150	MHz	—
5	Duty Cycle	—	40	50	60	%	FVCO=300MHz~600MHz

Note:
1 See users manual for definition.
2 DF = Division Factor
Ef = External Frequency
Mf = Multiplication Factor
PDF = Predivision Factor
FM= Frequency Multiplier
OD = Output Divider
Tc = Internal Clock Period
3 Maximum frequency will vary depending on the ordered part number.

11 External Clock Operation

The DSP56374 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; an example is shown below.



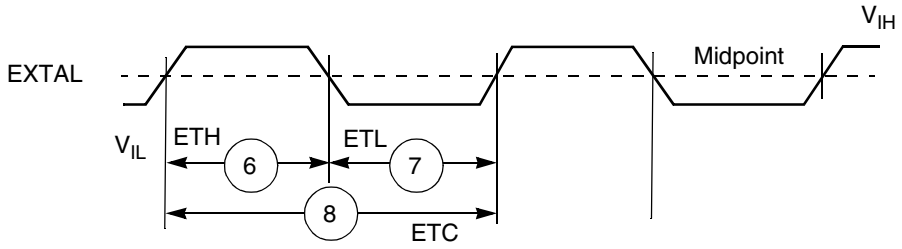
Suggested component values:

f_{osc} = 24.576 MHz
R = 1 M ±10%
C (EXTAL)= 18 pF
C (XTAL) = 47 pF

Calculations are for a 12 - 49 MHz crystal with the following parameters:

- shunt capacitance (C_0) of 10 pF - 12 pF
- series resistance 40 Ohm
- drive level of 10 μW

If the DSP56374 system clock is an externally supplied square wave voltage source, it is connected to EXTAL (Figure 2.). When the external square wave source connects to EXTAL, the XTAL pin is not used.



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 2. External Clock Timing

Table 19. Clock Operation

No.	Characteristics	Symbol	Min	Max	Units
6	EXTAL input high [1] (40% to 60% duty cycle)	Eth	3.33	50	ns
7	EXTAL input low[2] (40% to 60% duty cycle)	Etl	3.33	50	ns
8	EXTAL cycle time • With PLL disabled • With PLL enabled	Etc	6.67 50	inf 200	ns
9	Instruction cycle time= I_{CYC} = T_C[3] • With PLL disabled • With PLL enabled	Icyc	6.67 6.67	inf 13.33	ns

Table 19. Clock Operation (continued)

No.	Characteristics	Symbol	Min	Max	Units

Note:

[1] Measured at 50% of the input transition.

[2] The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

[3] A valid clock signal must be applied to the EXTAL pin within 3 ms of the DSP56374 being powered up.

12 Reset, Stop, Mode Select, and Interrupt Timing

Table 20. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4]				
	• Power on, external clock generator, PLL disabled	$2 \times T_C$	13.4	—	ns
	• Power on, external clock generator, PLL enabled	$2 \times T_C$	13.4	—	ns
13	Syn reset deassert delay time				
	• Minimum	$2 \times T_C$	13.4	—	ns
	• Maximum (PLL enabled)	$(2 \times T_C) + T_{LOCK}$	5.0	—	ms
14	Mode select setup time		10.0	—	ns
15	Mode select hold time		10.0	—	ns
16	Minimum edge-triggered interrupt request assertion width	$2 \times T_C$	13.4	—	ns
17	Minimum edge-triggered interrupt request deassertion width	$2 \times T_C$	13.4	—	ns
18	Delay from interrupt trigger to interrupt code execution	$10 \times T_C + 5$	72	—	ns
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[1, 2, 3]				
	• PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9 + (128 \times T_C)$	854	—	µs
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$25 \times T_C$	165	—	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	$9 + (128 \times T_C) + T_{LOCK}$	5.7		ms
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	$(25 \times T_C) + T_{LOCK}$	5		ms
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution[1]	$10 \times T_C + 3.0$		69.0	ns

Table 20. Reset, Stop, Mode Select, and Interrupt Timing (continued)

No.	Characteristics	Expression	Min	Max	Unit
21	Interrupt Requests Rate[1]				
	• ESAI, ESAI_1, SHI, Timer	12 x T_C	—	80.0	ns
	• DMA	8 x T_C	—	53.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	8 x T_C	—	53.0	ns
	• $\overline{IRQ}$ (level trigger)	12 x T_C	—	80.0	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, SHI	6 x T_C	—	40.0	ns
	• Data write to ESAI, ESAI_1, SHI	7 x T_C	—	46.7	ns
	• Timer	2 x T_C	—	13.4	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	3 x T_C	—	20.0	ns

Note:

[1] When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

[2] For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.

For PLL enable, (if bet 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.

[3] Periodically sampled and not 100% tested.

[4] $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other “required $\overline{RESET}$ duration” conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

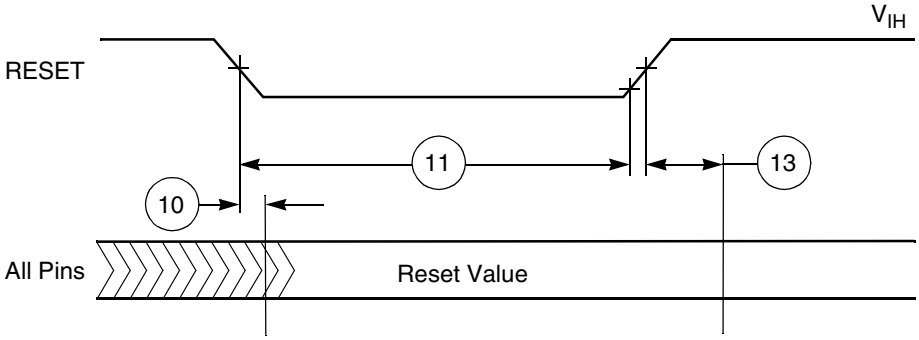


Figure 3. Reset Timing

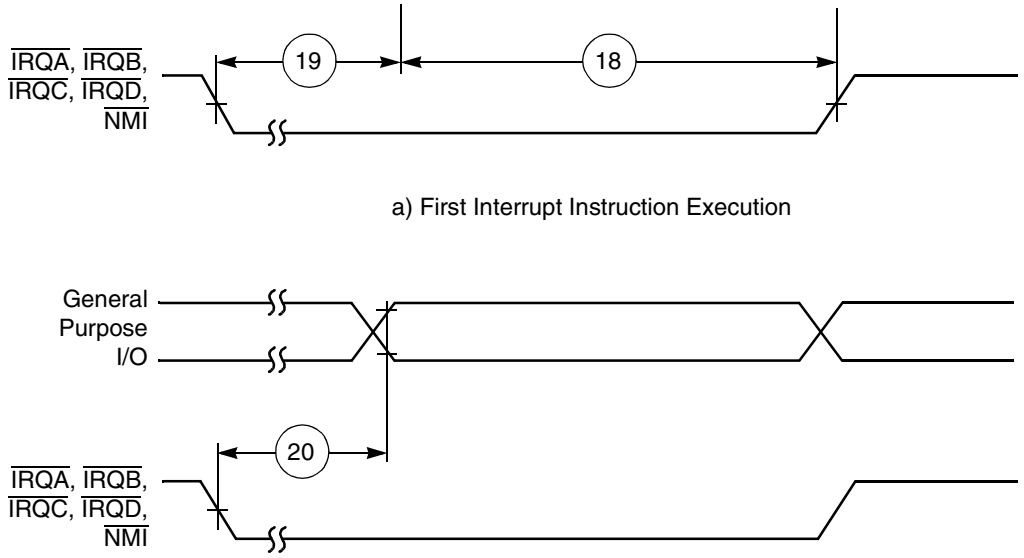


Figure 4. External Fast Interrupt Timing

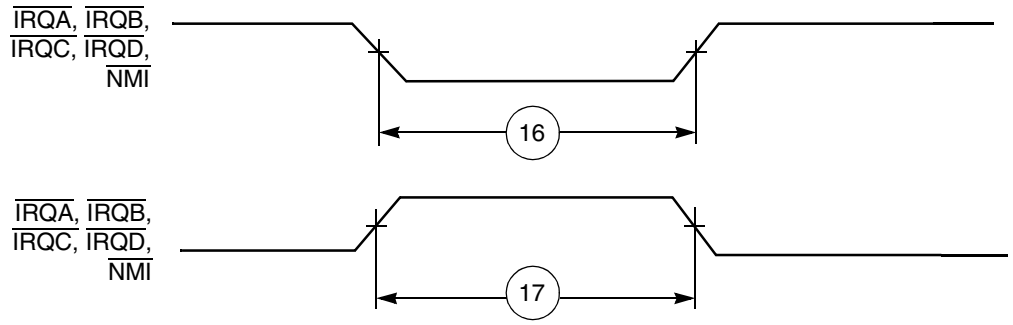


Figure 5. External Interrupt Timing (Negative Edge-Triggered)

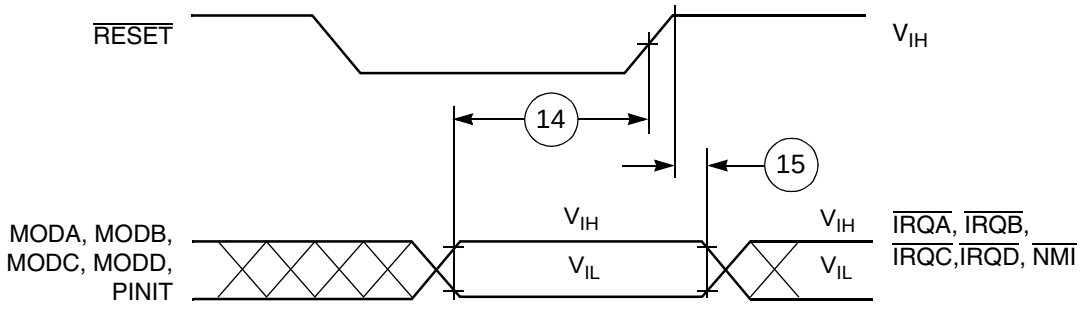


Figure 6. Recovery from Stop State Using IRQA Interrupt Service

13 Serial Host Interface SPI Protocol Timing

Table 21. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master/Slave	Bypassed	10.0 x T_C + 9	76.0	—	ns
			Very Narrow	10.0 x T_C + 9	76.0	—	ns
			Narrow	10.0 x T_C + 133	200.0	—	ns
			Wide	10.0 x T_C + 333	400.0	—	ns
XX	Tolerable Spike width on data or clock in.	—	Bypassed	—	—	0	ns
			Very Narrow	—	—	10	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
24	Serial clock high period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
25	Serial clock low period	Master	Bypassed	—	38.0	—	ns
			Very Narrow	—	38.0	—	ns
			Narrow	—	100.0	—	ns
			Wide	—	200.0	—	ns
		Slave	Bypassed	2.0 x T_C + 19.6	33.0	—	ns
			Very Narrow	2.0 x T_C + 19.6	33.0	—	ns
			Narrow	2.0 x T_C + 86.6	100.0	—	ns
			Wide	2.0 x T_C + 186.6	200.0	—	ns
26	Serial clock rise/fall time	Master	—	—	—	—	ns
		Slave	—	—	—	5	ns
				—			

Table 21. Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	2.0 x T_C + 12.6	26	—	ns
			Very Narrow	2.0 x T_C + 2.6	16	—	ns
			Narrow	2.0 x T_C – 37.4[5]	0	—	ns
			Wide	2.0 x T_C – 87.4[5]	0	—	ns
	CPHA = 1	Slave	Bypassed	—	10	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	—	12	—	ns
			Very Narrow	—	22	—	ns
			Narrow	—	100	—	ns
			Wide	—	200	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master /Slave	Bypassed	—	0	—	ns
			Very Narrow	—	0	—	ns
			Narrow	—	0	—	ns
			Wide	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master /Slave	Bypassed	3.0 x T_C	20	—	ns
			Very Narrow	3.0 x T_C + 23.2	43.2	—	ns
			Narrow	3.0 x T_C + 53.2	73.2	—	ns
			Wide	3.0 x T_C + 80	100.0	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master /Slave	Bypassed	3.0 x T_C + 26.1	—	46.2	ns
			Very Narrow	3.0 x T_C + 90.4	—	110.4	ns
			Narrow	3.0 x T_C + 116.4	—	136.4	ns
			Wide	3.0 x T_C + 203.4	—	223.4	ns
34	SCK edge to data out not valid (data out hold time)	Master /Slave	Bypassed	2.0 x T_C	13.4	—	ns
			Very Narrow	2.0 x T_C + 1.6	15	—	ns
			Narrow	2.0 x T_C + 41.6	55	—	ns
			Wide	2.0 x T_C + 91.6	105	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	—	12.0	ns

Table 21. Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1,3,4]	Mode	Filter Mode	Expression	Min	Max	Unit
36	SCK edge following the first SCK sampling edge to $\overline{\text{HREQ}}$ output deassertion	Slave	Bypassed	3.0 x T_C + 30	50	—	ns
			Very Narrow	3.0 x T_C + 40	60	—	ns
			Narrow	3.0 x T_C + 80	100	—	ns
			Wide	3.0 x T_C + 120	150	—	ns
37	Last SCK sampling edge to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 1)	Slave	Bypassed	4.0 x T_C	57.0	—	ns
			Very Narrow	4.0 x T_C	67.0	—	ns
			Narrow	4.0 x T_C	107.0	—	ns
			Wide	4.0 x T_C	157.0	—	ns
38	$\overline{\text{SS}}$ deassertion to $\overline{\text{HREQ}}$ output not deasserted (CPHA = 0)	Slave	—	3.0 x T_C + 30	50.0	—	ns
39	$\overline{\text{SS}}$ deassertion pulse width (CPHA = 0)	Slave	—	2.0 x T_C	13.4	—	ns
40	$\overline{\text{HREQ}}$ in assertion to first SCK edge	Master	Bypassed	0.5 x T_{SPICC} + 3.0 x T_C + 5	63	—	ns
			Very Narrow	0.5 x T_{SPICC} + 3.0 x T_C + 5	63	—	ns
			Narrow	0.5 x T_{SPICC} + 3.0 x T_C + 5	125	—	ns
			Wide	0.5 x T_{SPICC} + 3.0 x T_C + 5	225	—	ns
41	$\overline{\text{HREQ}}$ in deassertion to last SCK sampling edge ($\overline{\text{HREQ}}$ in set-up time) (CPHA = 1)	Master	—	—	0	—	ns
42	First SCK edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	Master	—	—	0	—	ns
43	$\overline{\text{HREQ}}$ assertion width	Master	—	3.0 x T_C	20	—	ns

Note:
1 V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2 Periodically sampled, not 100% tested
3 All times assume noise free inputs.
4 All times assume internal clock frequency of 150 MHz.
5 Equation applies when the result is positive T_C.

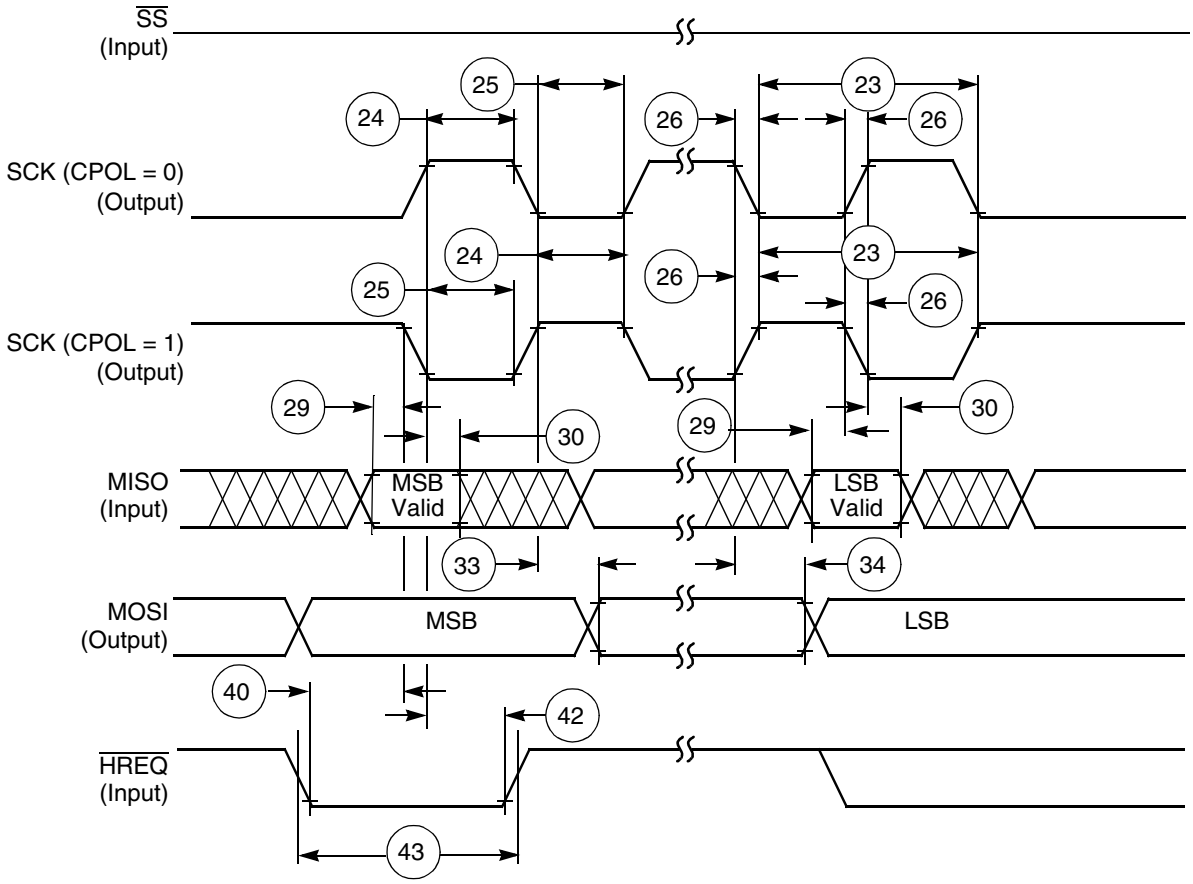


Figure 7. SPI Master Timing (CPHA = 0)

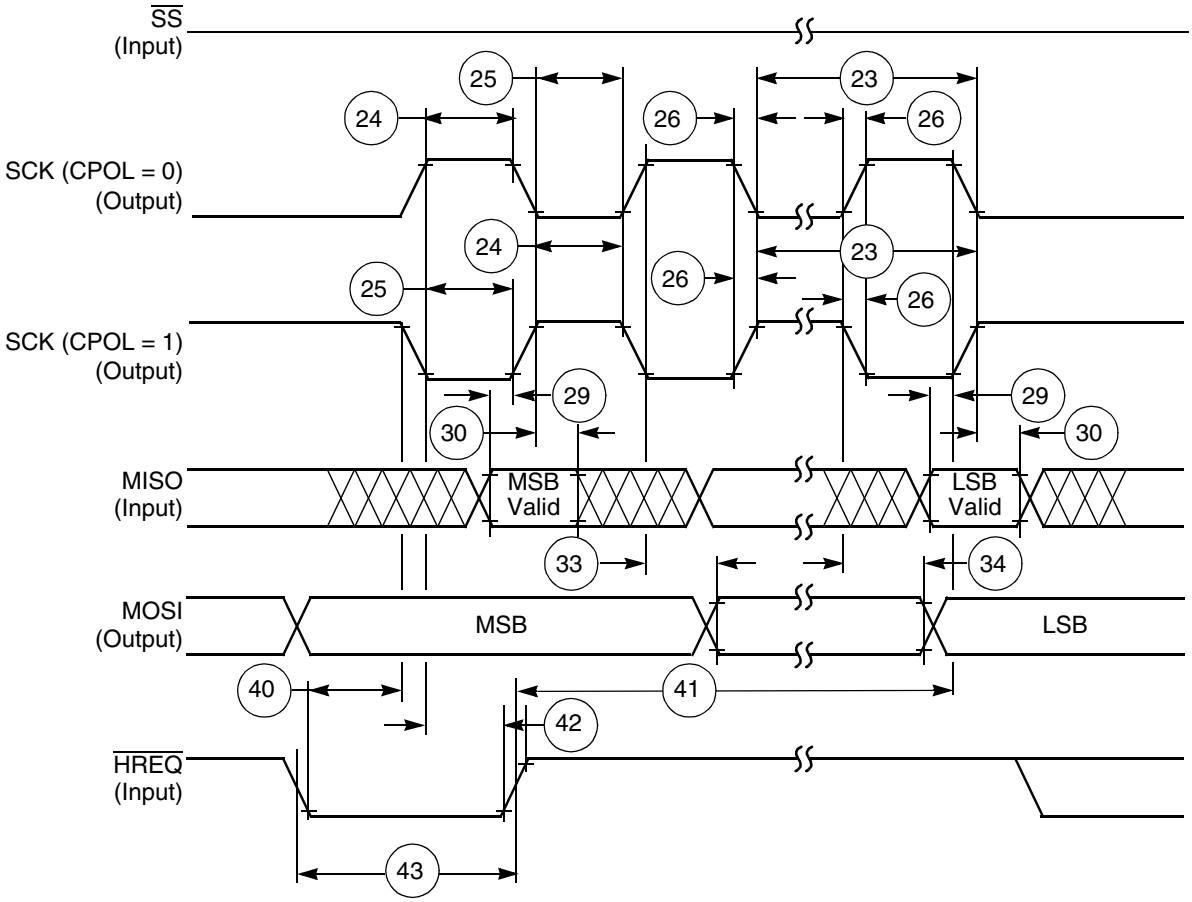


Figure 8. SPI Master Timing (CPHA = 1)

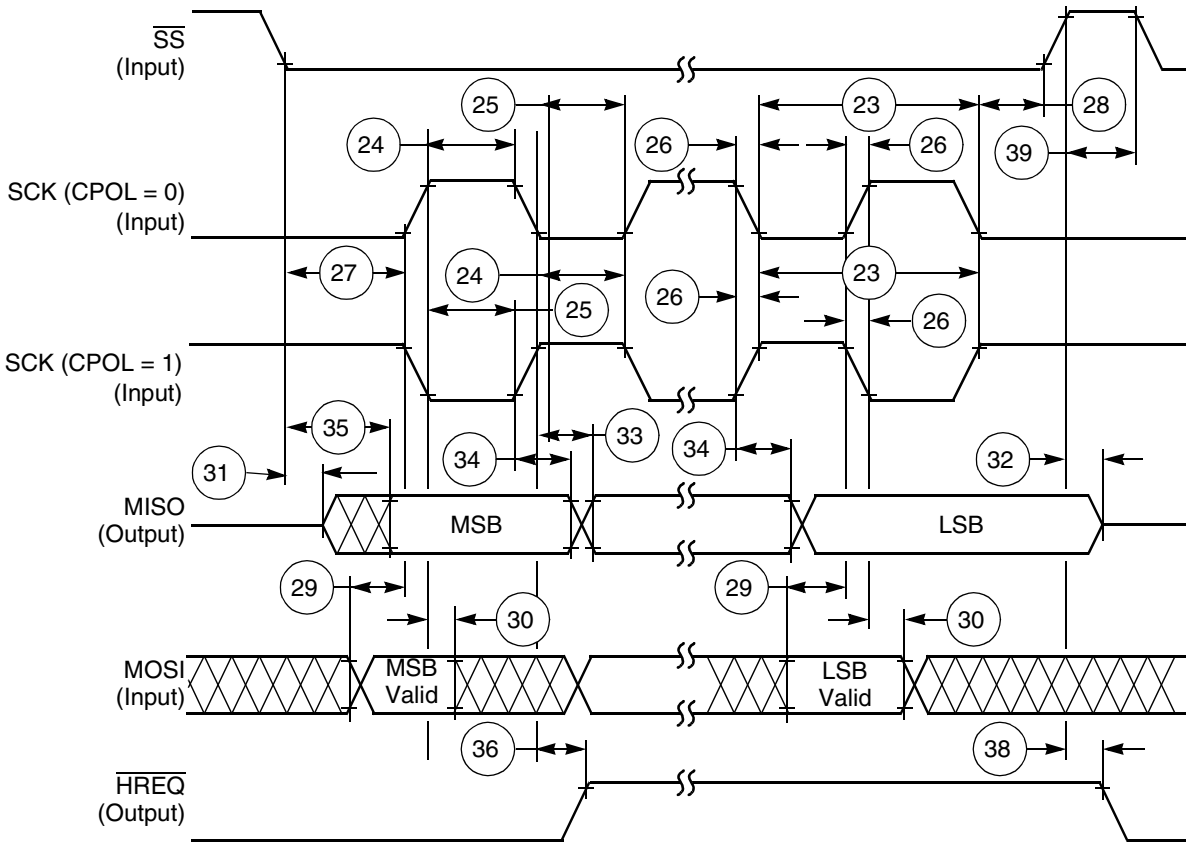


Figure 9. SPI Slave Timing (CPHA = 0)

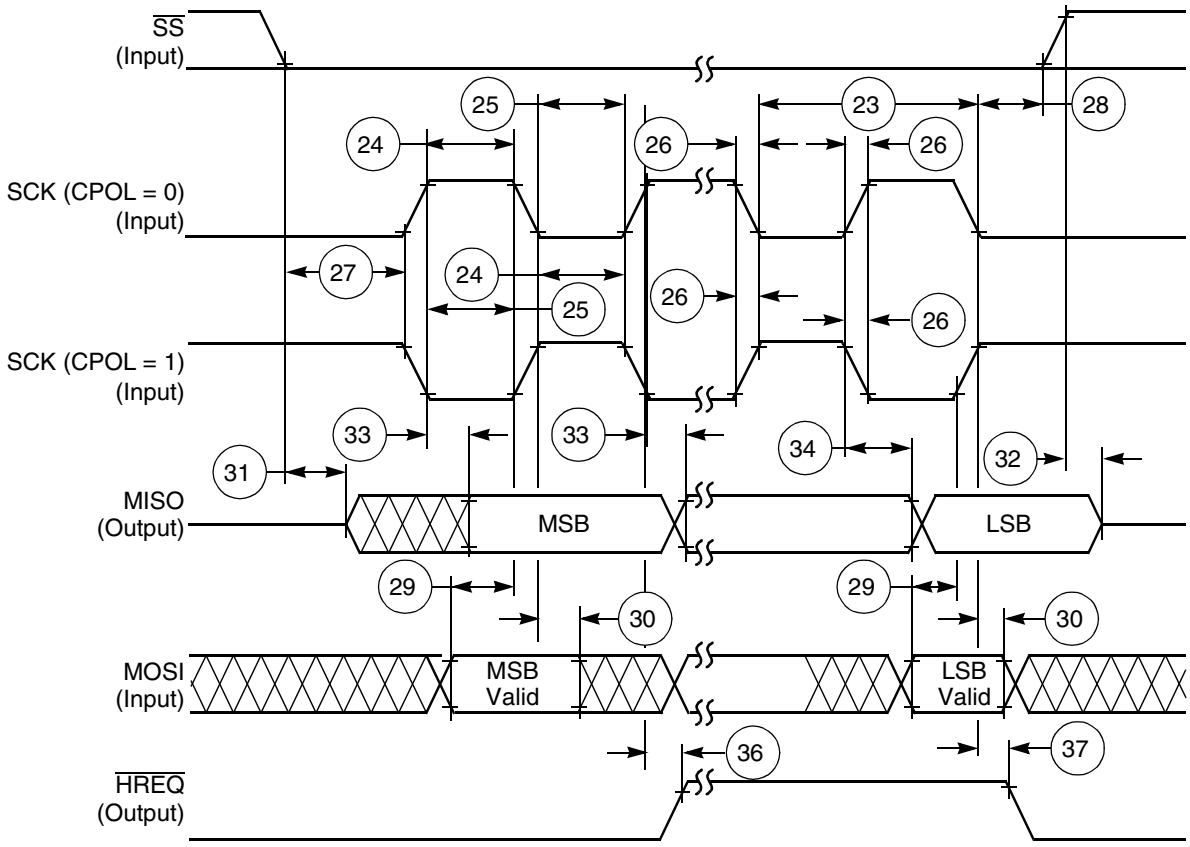


Figure 10. SPI Slave Timing (CPHA = 1)

14 Serial Host Interface (SHI) I2C Protocol Timing

Table 22. SHI I2C Protocol Timing

Standard I2C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
XX	Tolerable Spike Width on SCL or SDA	—					
	Filters Bypassed		—	0	—	0	ns
	Very Narrow Filters enabled		—	10	—	10	ns
	Narrow Filters enabled		—	50	—	50	ns
	Wide Fileters enabled.		—	100	—	100	ns
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs

Table 22. SHI I²C Protocol Timing (continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time	T_R	—	5.0	—	5.0	ns
51	SCL and SDA fall time	T_F	—	5.0	—	5.0	ns
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency	F_{OSC}					
	• Filters bypassed		10.6	—	28.5	—	MHz
	• Very Narrrow filters enabled		10.6	—	28.5	—	MHz
	• Narrow filters enabled		11.8	—	39.7	—	MHz
	• Wide filters enabled		13.1	—	61.0	—	MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{HREQ}$ output deassertion[2]	$T_{NG;RQO}$					
	• Filters bypassed	$4 \times T_C + 30$	—	57.0	—	57.0	ns
	• Very Narrow filters enabled	$4 \times T_C + 50$	—	77.0	—	67.0	ns
	• Narrow filters enabled	$4 \times T_C + 130$	—	157.0	—	157.0	ns
	• Wide filters enabled	$4 \times T_C + 230$	—	257.0	—	257.0	ns
59	Last SCL edge to $\overline{HREQ}$ output not deasserted[2]	$T_{AS;RQO}$					
	• Filters bypassed	$2 \times T_C + 30$	44	—	44	—	ns
	• Very Narrow filters enabled	$2 \times T_C + 40$	54	—	54	—	ns
	• Narrow filters enabled	$2 \times T_C + 80$	94	—	94	—	ns
	• Wide filters enabled	$2 \times T_C + 130$	144	—	144	—	ns
60	$\overline{HREQ}$ in assertion to first SCL edge	$T_{AS;RQI}$					
	• Filters bypassed		4327	—	927	—	ns
	• Very Narrow filters enabled		4317	—	917	—	ns
	• Narrow filters enabled		4282	—	877	—	ns
	• Wide filters enabled		4227	—	827	—	ns
61	First SCL edge to $\overline{HREQ}$ is not asserted ($\overline{HREQ}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Table 22. SHI I²C Protocol Timing (continued)

Standard I²C							
No.	Characteristics[1,2,3,4,5]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	

Note:
1. V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2. Pull-up resistor: R_P (min) = 1.5 kOhm
3. Capacitive load: C_b (max) = 50 pF
4. All times assume noise free inputs
5. All times assume internal clock frequency of 150MHz

15 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \quad \textit{Eqn. 1}$$

where

— HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I²C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \text{ (if HDM[7:0] = \$02 and HRS = 1)} \quad \textit{Eqn. 2}$$

to

$$4096 \times T_C \text{ (if HDM[7:0] = \$FF and HRS = 0)} \quad \textit{Eqn. 3}$$

The programmed serial clock cycle (T_{I^2CCP}) should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 23.

Table 23. SCL Serial Clock Cycle (T_{SCL}) Generated as Master

Nominal	$T_{I^2CCP} + 3 \times T_C + 45ns + T_R$

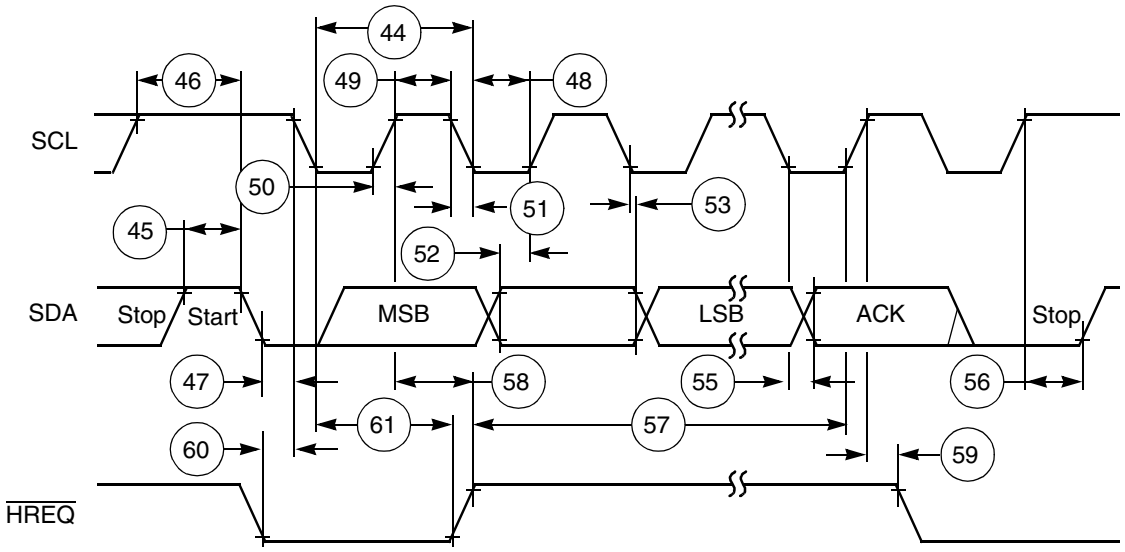


Figure 11. I²C Timing

16 Enhanced Serial Audio Interface Timing

Table 24. Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	26.4 26.4	— —	x ck i ck	ns
63	Clock high period • For internal clock • For external clock	t_{SSICCH}	 $2 \times T_C - 0.5$ $2 \times T_C$	 12.8 13.4	 — —		ns
64	Clock low period • For internal clock • For external clock	t_{SSICCL}	 $2 \times T_C$ $2 \times T_C$	 13.4 13.4	 — —		ns
65	SCKR edge to FSR out (bl) high	—	—	— —	17.0 7.0	x ck i ck a	ns
66	SCKR edge to FSR out (bl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
67	SCKR edge to FSR out (wr) high[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
68	SCKR edge to FSR out (wr) low[6]	—	—	— —	19.0 9.0	x ck i ck a	ns
69	SCKR edge to FSR out (wl) high	—	—	— —	16.0 6.0	x ck i ck a	ns

Table 24. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
70	SCKR edge to FSR out (wl) low	—	—	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR edge	—	—	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR edge [6]	—	—	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR edge	—	—	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR edge	—	—	2.5 8.5	— —	x ck i ck a	ns
76	Flags input setup before SCKR edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT edge to FST out (bl) high	—	—	— —	18.0 8.0	x ck i ck	ns
79	SCKT edge to FST out (bl) low	—	—	— —	20.0 10.0	x ck i ck	ns
80	SCKT edge to FST out (wr) high[6]	—	—	— —	20.0 10.0	x ck i ck	ns
81	SCKT edge to FST out (wr) low[6]	—	—	— —	22.0 12.0	x ck i ck	ns
82	SCKT edge to FST out (wl) high	—	—	— —	19.0 9.0	x ck i ck	ns
83	SCKT edge to FST out (wl) low	—	—	— —	20.0 10.0	x ck i ck	ns
84	SCKT edge to data out enable from high impedance	—	—	— —	22.0 17.0	x ck i ck	ns
85	SCKT edge to transmitter #0 drive enable assertion	—	—	— —	17.0 11.0	x ck i ck	ns
86	SCKT edge to data out valid	—	—	— —	18.0 13.0	x ck i ck	ns
87	SCKT edge to data out high impedance[7]	—	—	— —	21.0 16.0	x ck i ck	ns

Table 24. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
88	SCKT edge to transmitter #0 drive enable deassertion[7]	—	—	— —	14.0 9.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT edge[6]	—	—	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT edge	—	—	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT edge	—	—	4.0 5.0	— —	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	—	—	—	21.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	14.0	—	ns
94	Flag output valid after SCKT rising edge	—	—	— —	14.0 9.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	13.4	—		ns
96	HCKT input edge to SCKT output	—	—	—	18.0		ns
97	HCKR input edge to SCKR output	—	—	—	18.0		ns

Note:

1 V_{CORE_VDD} = 1.25 ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

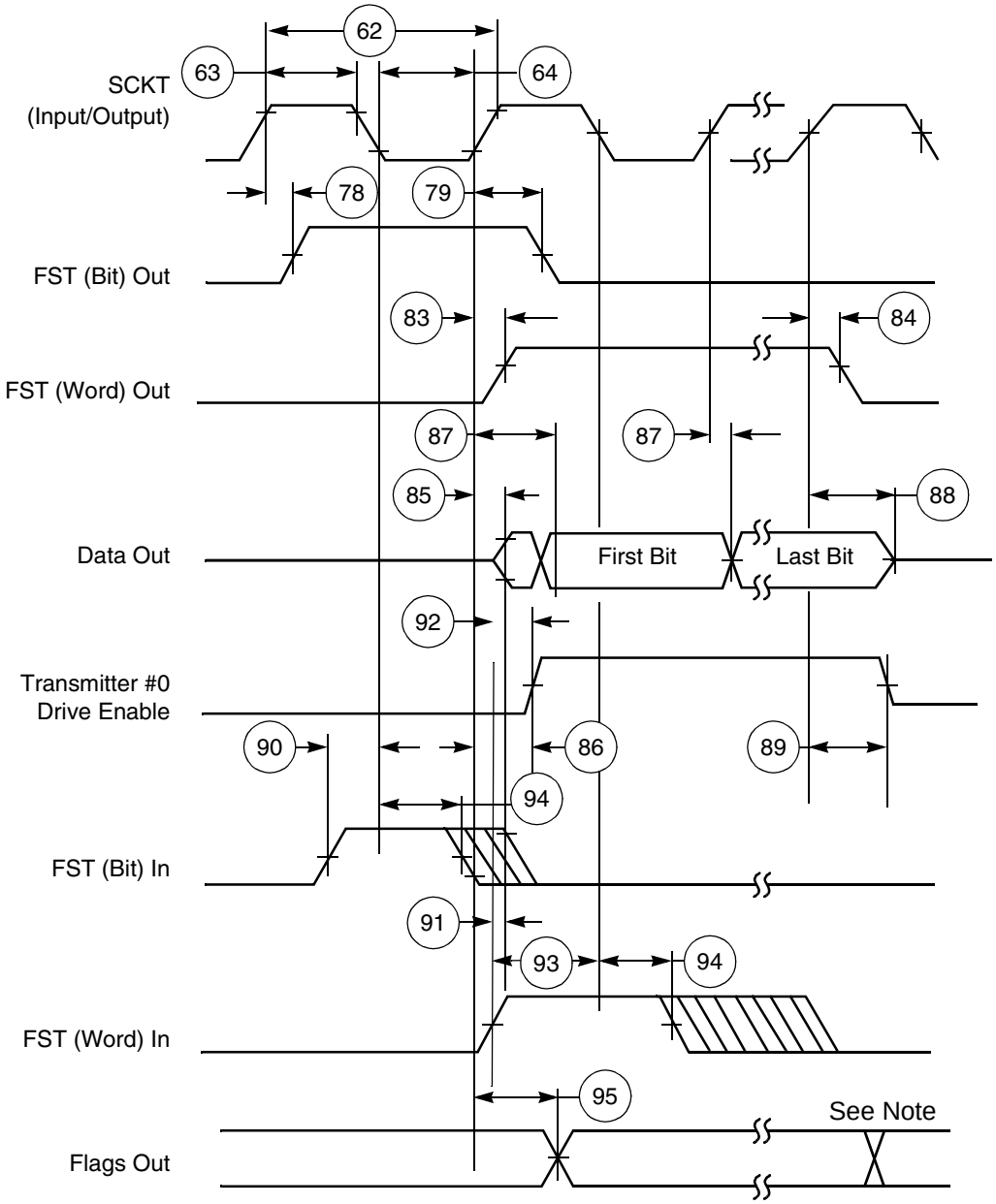
4 SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.

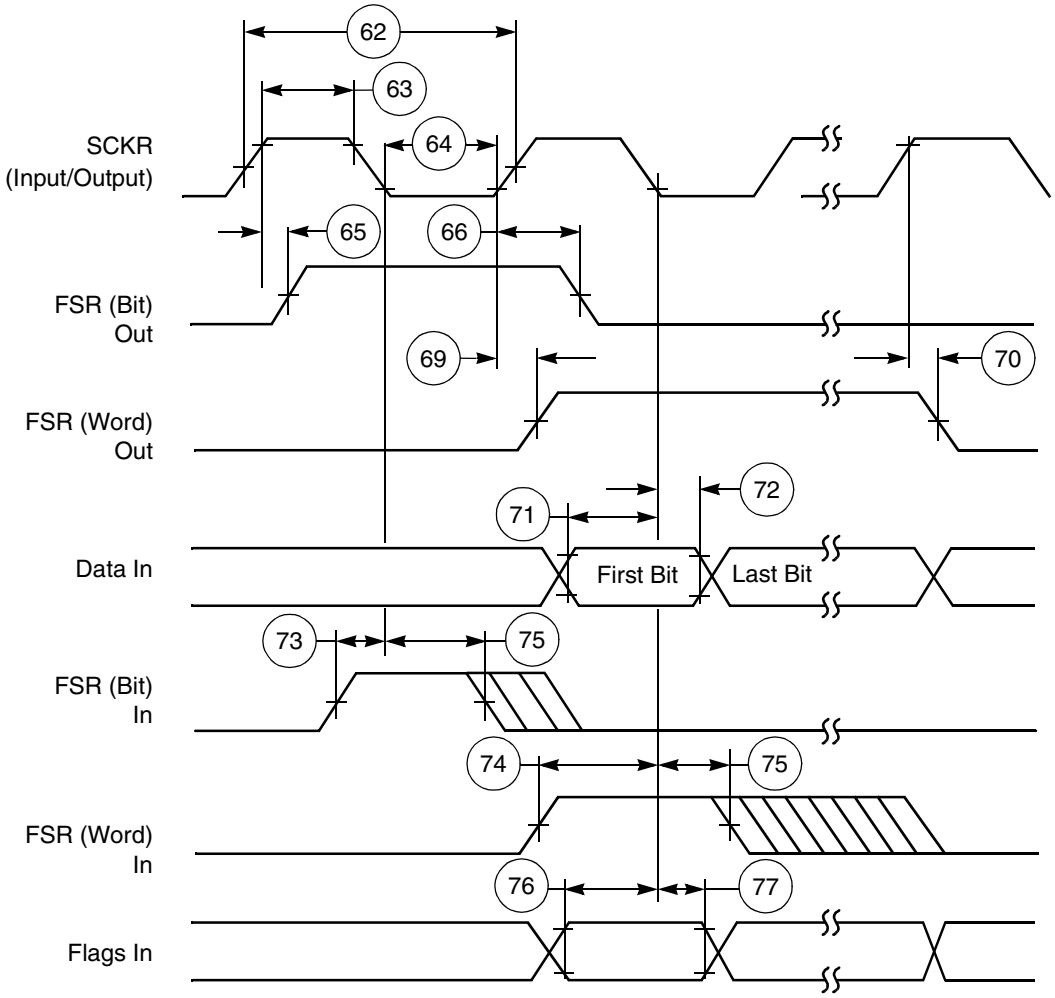
7 Periodically sampled and not 100% tested.

8 ESAI_1 specs match those of ESAI.



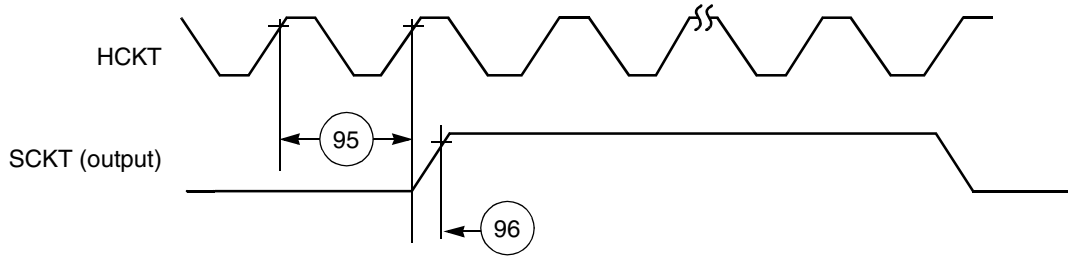
Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period. Figure 12 is drawn assuming positive polarity bit clock (TCKP=0) and positive frame sync polarity (TFSP=0).

Figure 12. ESAI Transmitter Timing



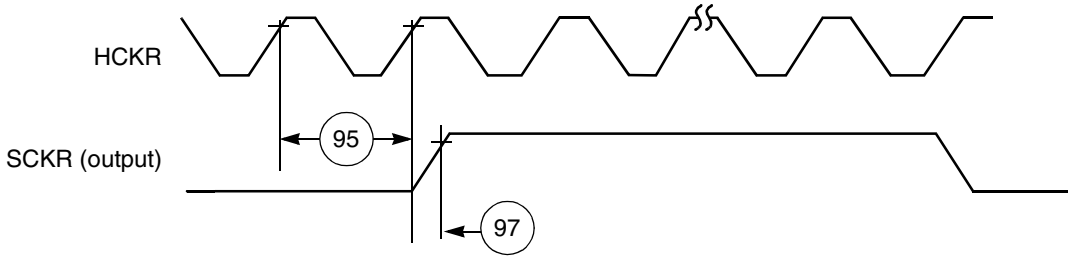
Note: Figure 13 is drawn assuming positive polarity bit clock (RCKP=0) and positive frame sync polarity (RFSP=0).

Figure 13. ESAI Receiver Timing



Note: Figure 14 is drawn assuming positive polarity high frequency clock (THCKP=0) and positive bit clock polarity (TCKP=0).

Figure 14. ESAI HCKT Timing



Note: Figure 15 is drawn assuming positive polarity high frequency clock (RHCKP=0) and positive bit clock polarity (RCKP=0).

Figure 15. ESAI HCKR Timing

17 Timer Timing

Table 25. Timer Timing

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
98	TIO Low	$2 \times T_C + 2.0$	15.4	—	ns
99	TIO High	$2 \times T_C + 2.0$	15.4	—	ns
Note: V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF					

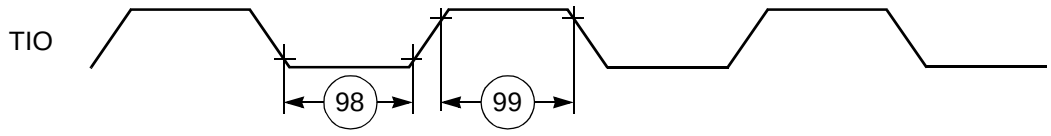


Figure 16. TIO Timer Event Input Restrictions

18 GPIO Timing

Table 26. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
100	EXTAL edge to GPIO out valid (GPIO out delay time)[2]		—	7	ns
101	EXTAL edge to GPIO out not valid (GPIO out hold time)[2]		—	7	ns
102	GPIO In valid to EXTAL edge (GPIO in set-up time)[2]		2	—	ns
103	EXTAL edge to GPIO in not valid (GPIO in hold time)[2]		0	—	ns
104	Minimum GPIO pulse high width	$T_C + 13$	19.7	—	ns
105	Minimum GPIO pulse low width	$T_C + 13$	19.7	—	ns
106	GPIO out rise time	—	—	13.0	ns
107	GPIO out fall time	—	—	13.0	ns

Note:
1 V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2 PLL Disabled, EXTAL driven by a square wave.

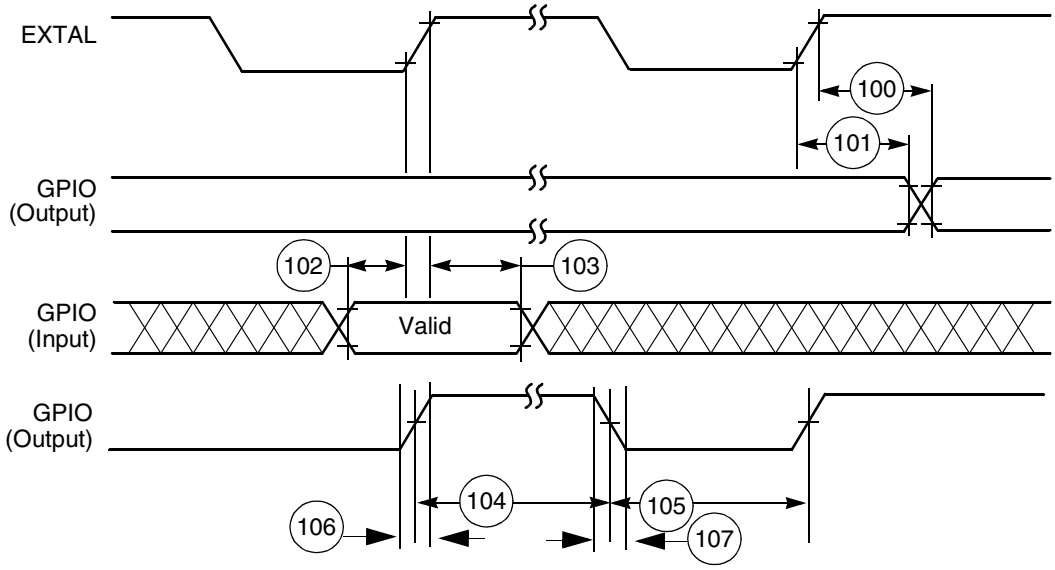


Figure 17. GPIO Timing

19 JTAG Timing

Table 27. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
108	TCK frequency of operation (1/($T_C \times 3$); maximum 10 MHz)	—	10.0	MHz

Table 27. JTAG Timing (continued)

No.	Characteristics	All frequencies		Unit
		Min	Max	
109	TCK cycle time in Crystal mode	100.0	—	ns
110	TCK clock pulse width measured at 1.65 V	50.0	—	ns
111	TCK rise and fall times	—	3.0	ns
112	Boundary scan input data setup time	15.0	—	ns
113	Boundary scan input data hold time	24.0	—	ns
114	TCK low to output data valid	—	40.0	ns
115	TCK low to output high impedance	—	40.0	ns
116	TMS, TDI data setup time	5.0	—	ns
117	TMS, TDI data hold time	25.0	—	ns
118	TCK low to TDO data valid	—	44.0	ns
119	TCK low to TDO high impedance	—	44.0	ns

Note:
1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = -40°C to 110°C (52 LQFP) / -40°C to 105°C (80 LQFP), C_L = 50 pF
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

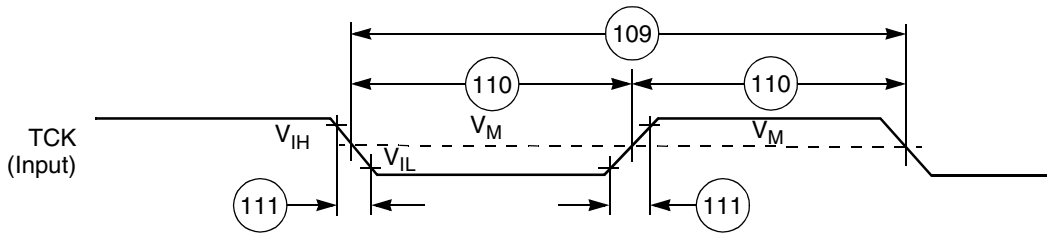


Figure 18. Test Clock Input Timing Diagram

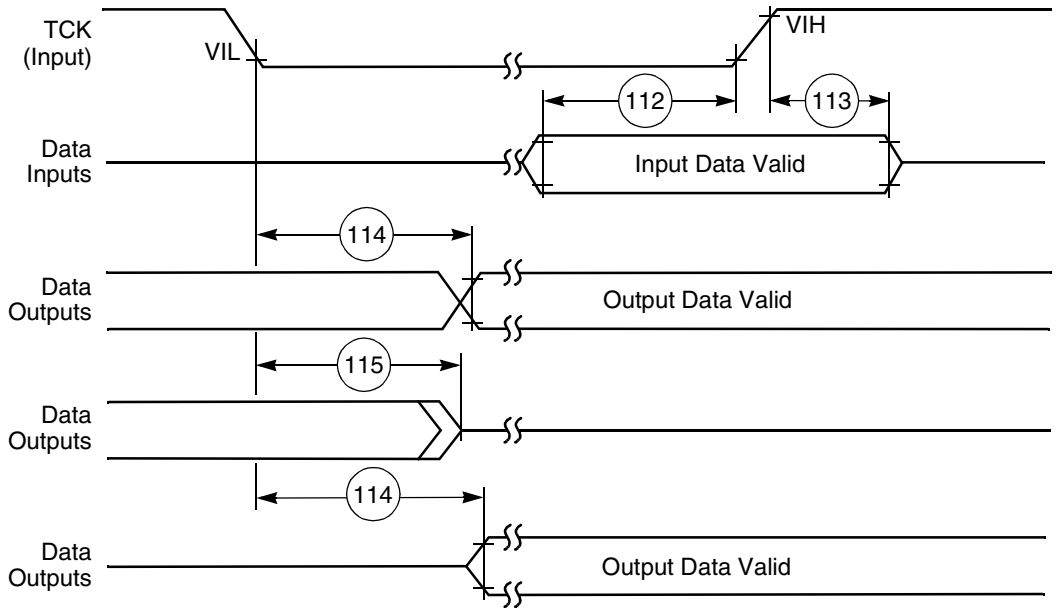


Figure 19. Debugger Port Timing Diagram

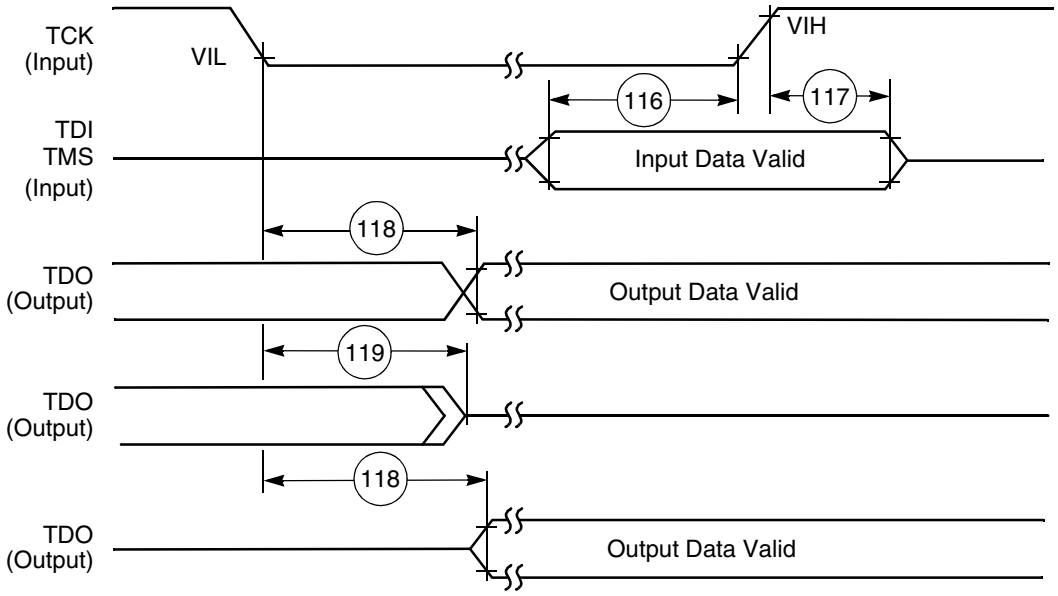


Figure 20. Test Access Port Timing Diagram

20 Watchdog Timer Timing

Table 28. Watchdog Timer Timing

No.	Characteristics	Expression	Min	Max	Unit
120	Delay from time-out to fall of TIO1	$2 \times T_C$	13.4	—	ns
121	Delay from timer clear to rise of TIO1	2 x Tc	13.4	—	ns

Appendix A
Package Information

A.1 DSP56374 Pinout

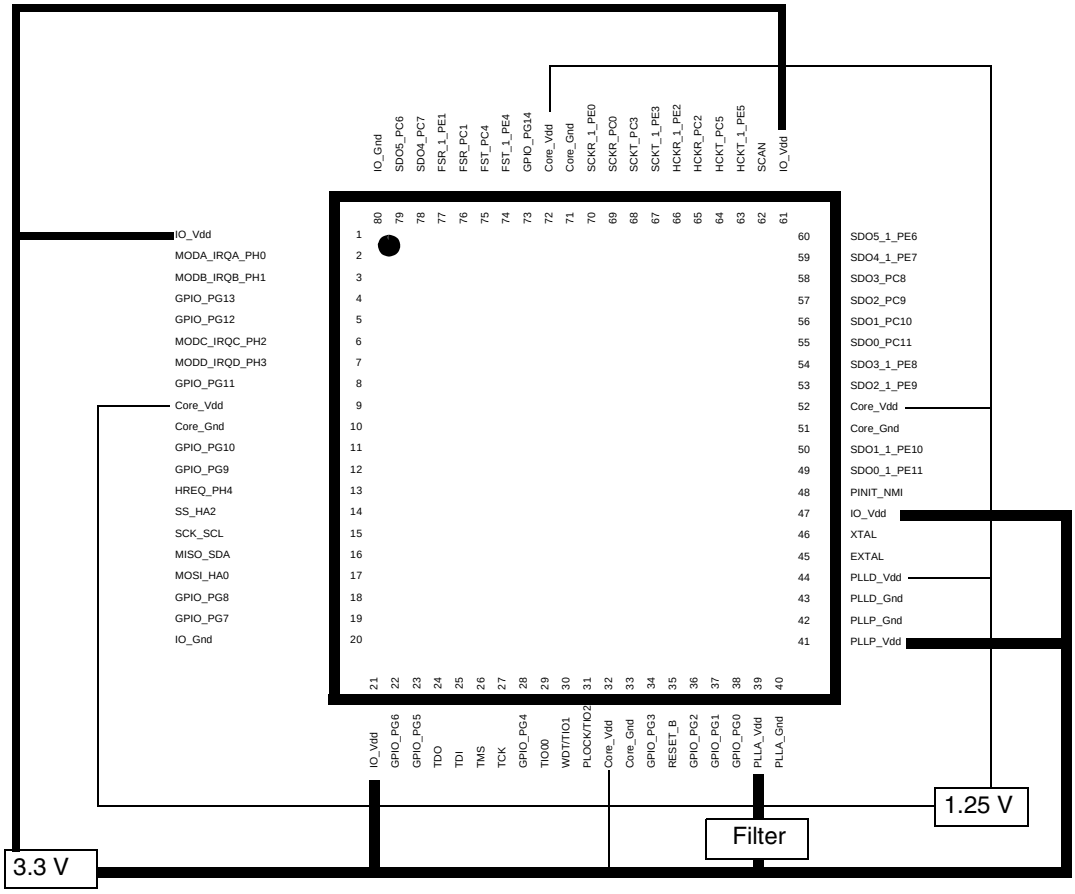


Figure A-1. 80-Pin Vdd Connections

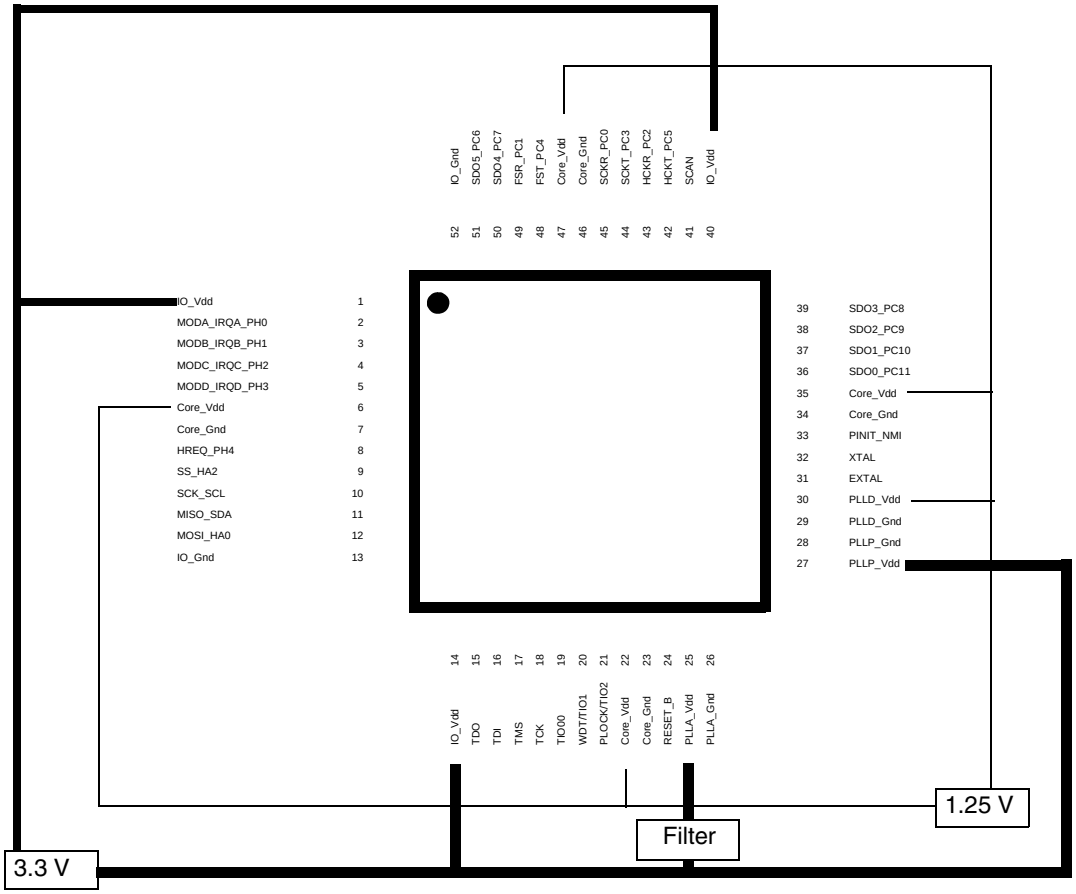
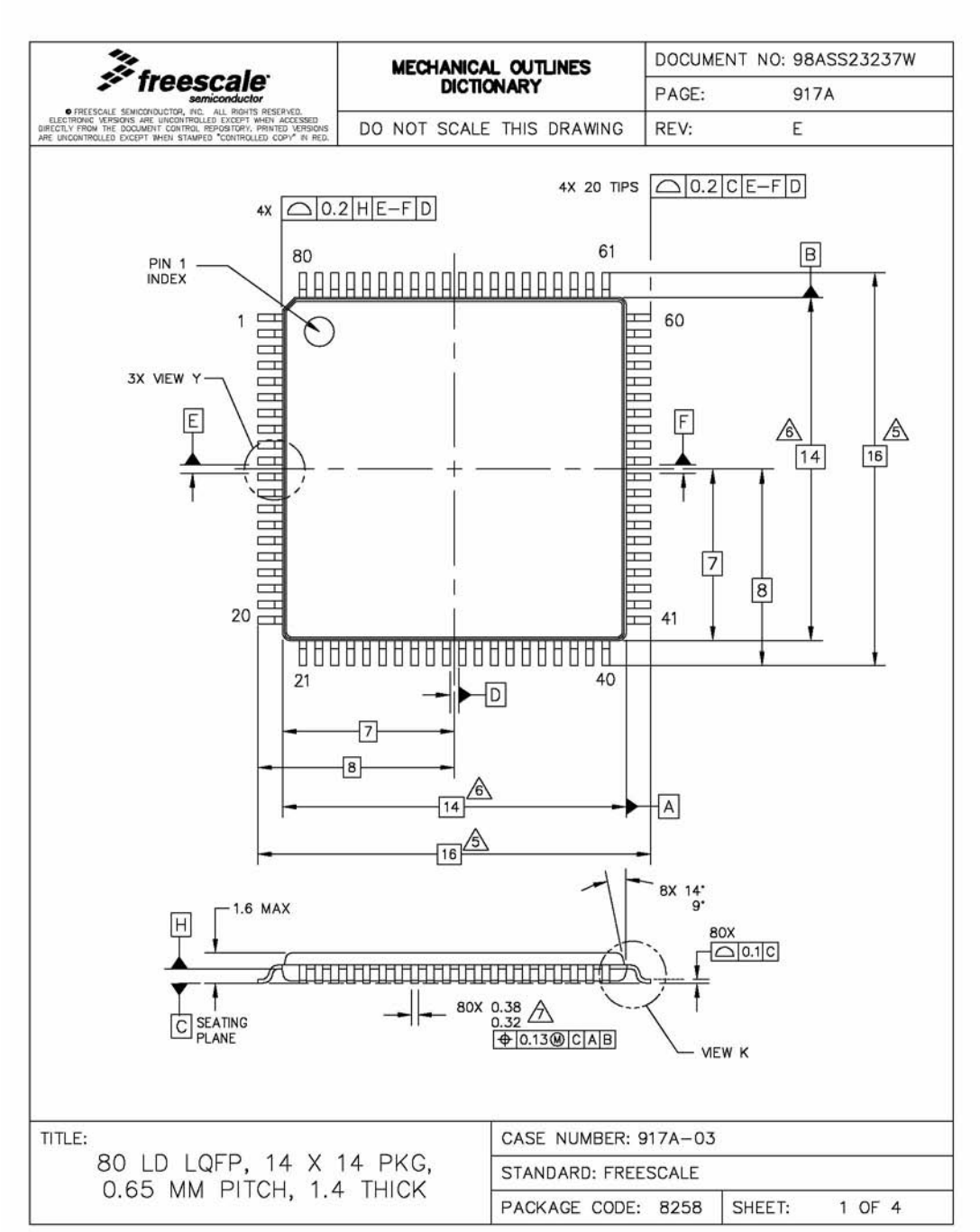
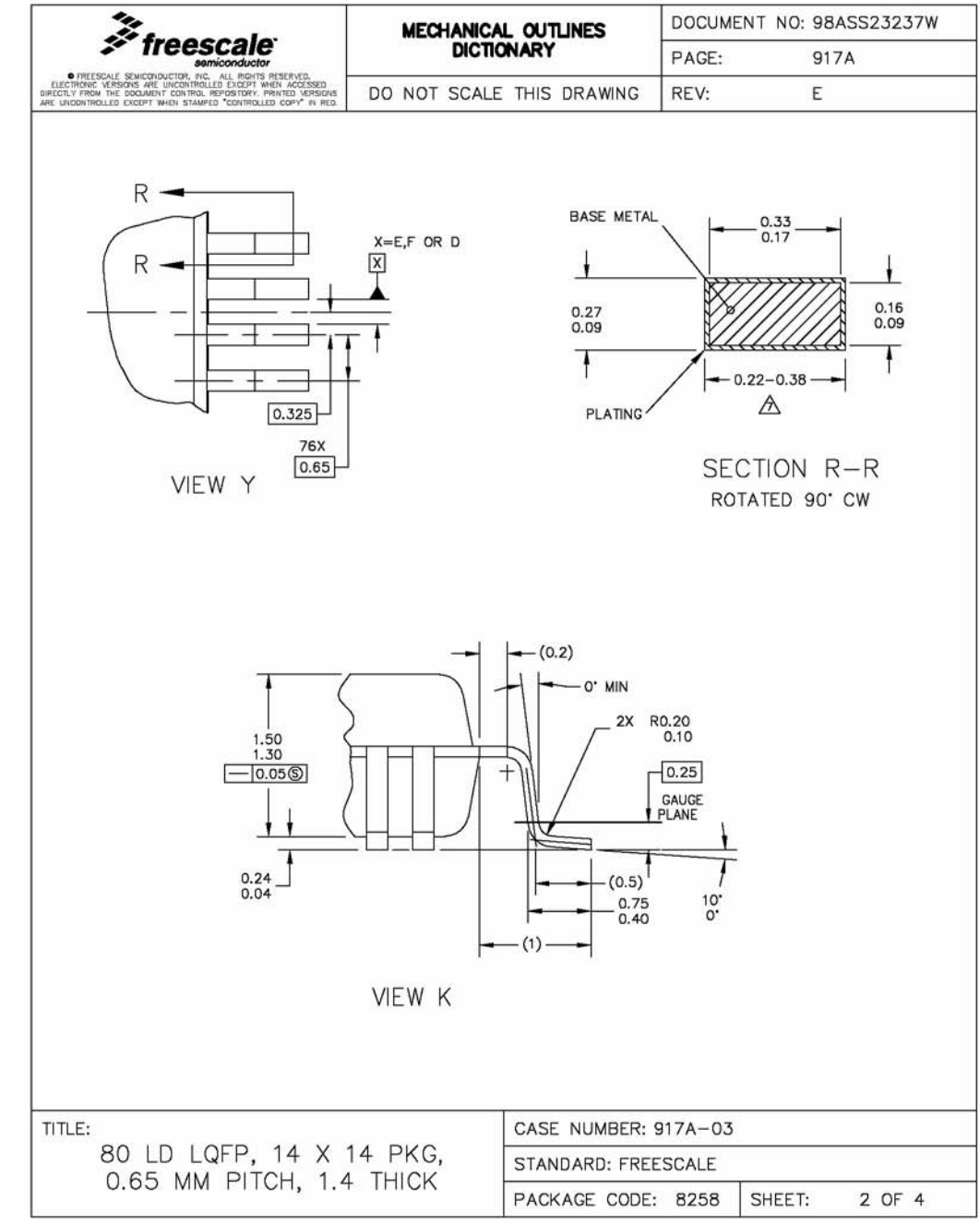


Figure A-2. 52-pin Vdd Connections

A.2 Package Information

A.2.1 80-Pin Package

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0.65
VIEW Y
BASE METAL
0.33
0.17
0.27
0.09
0.16
0.09
0.22–0.38
PLATING
7
SECTION R–R
ROTATED 90° CW
(0.2)
0° MIN
2X R0.20
0.10
1.50
1.30
0.05 S
0.25
GAUGE
PLANE
0.24
0.04
(0.5)
0.75
0.40
10°
0°
(1)
VIEW K
TITLE:
80 LD LQFP, 14 X 14 PKG,
0.65 MM PITCH, 1.4 THICK
CASE NUMBER: 917A–03
STANDARD: FREESCALE
PACKAGE CODE: 8258
SHEET: 2 OF 4

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3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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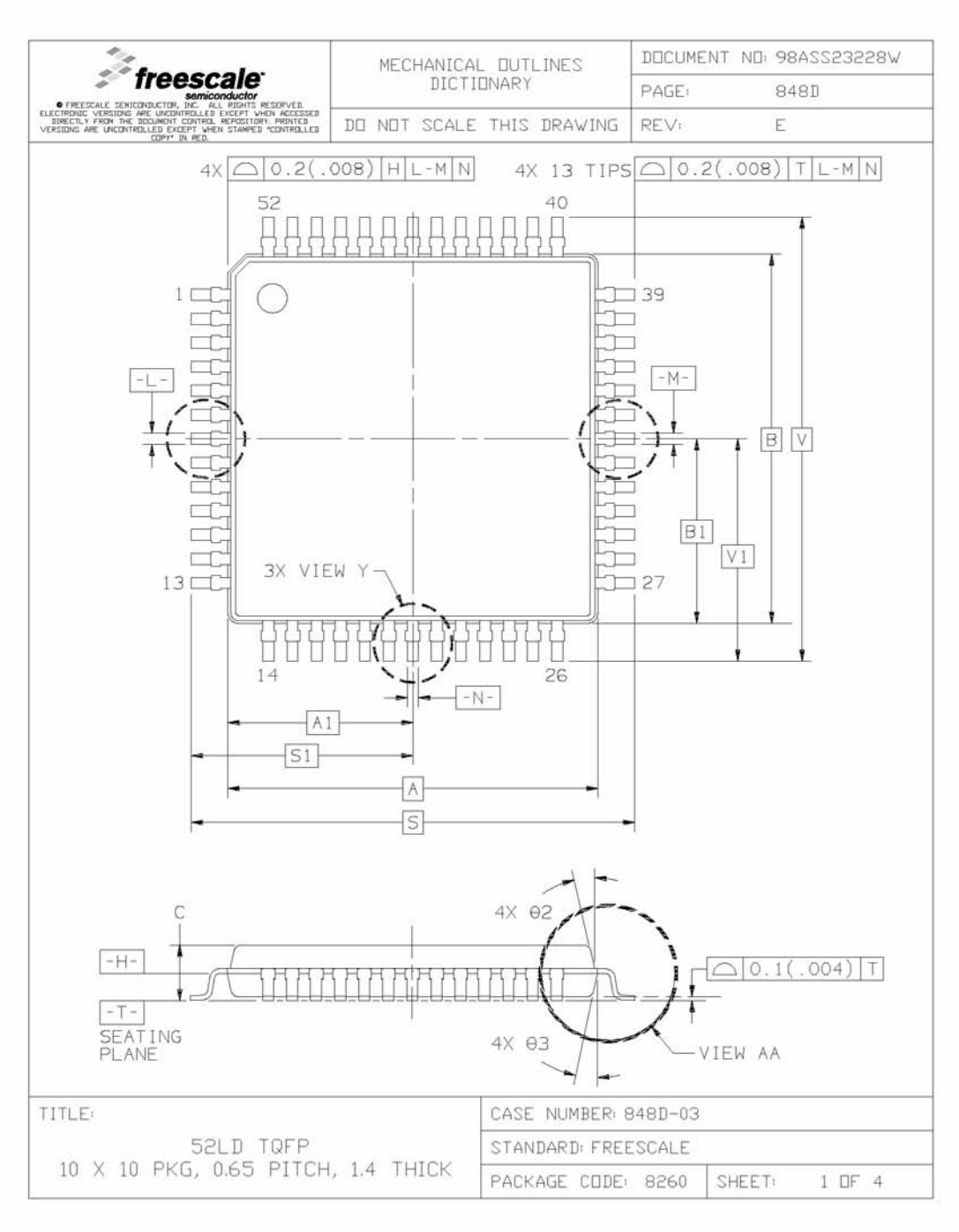
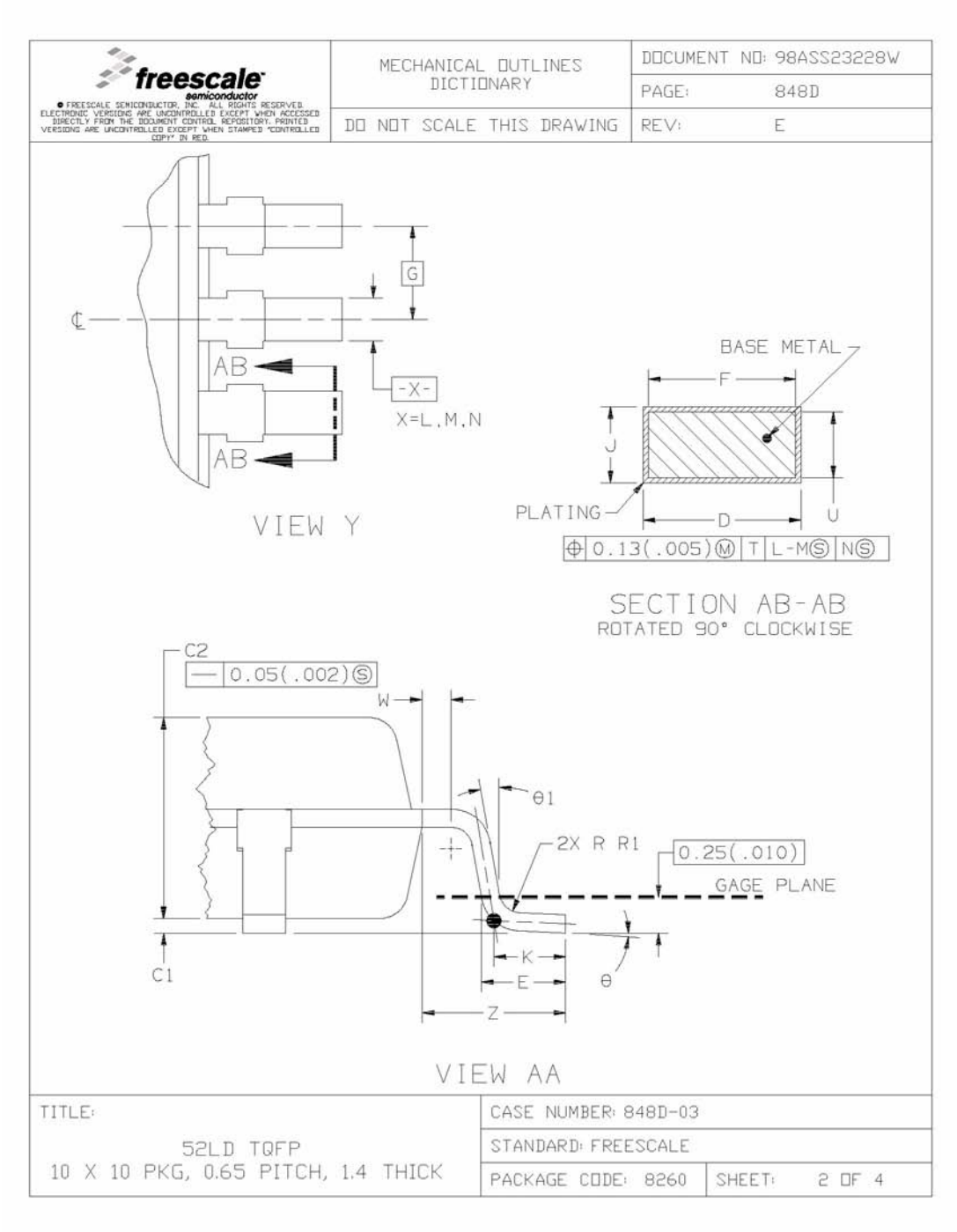
A.2.2 52-Pin Package

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D
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SECTION AB-AB
ROTATED 90° CLOCKWISE
C2
0.05(.002) S
W
θ1
2X R R1
0.25(.010)
GAGE PLANE
K
E
θ
C1
Z
VIEW AA
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52LD TQFP
10 X 10 PKG, 0.65 PITCH, 1.4 THICK
CASE NUMBER: 848D-03
STANDARD: FREESCALE
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4. DATUMS [-L-], [-M-] AND [-N-] TO BE DETERMINED AT DATUM PLANE [-H-].
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE [-T-].
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25(.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [-H-].
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46(.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07(.003).

	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC						
A1	5.00 BSC		0.197 BSC						
B	10.00 BSC		0.394 BSC						
B1	5.00 BSC		0.197 BSC						
C	---	1.70	---	0.067					
C1	0.05	0.20	0.002	0.008					
C2	1.30	1.50	0.051	0.059					
D	0.20	0.40	0.008	0.016					
E	0.45	0.75	0.018	0.030					
F	0.22	0.35	0.009	0.014					
G	0.65 BSC		0.026 BSC						
J	0.07	0.20	0.003	0.008					
K	0.50 REF		0.020 REF						
R1	0.08	0.20	0.003	0.008					
S	12.00 BSC		0.472 BSC						
S1	6.00 BSC		0.236 BSC						
U	0.09	0.16	0.004	0.006					
V	12.00 BSC		0.472 BSC						
V1	6.00 BSC		0.236 BSC						
W	0.20 REF		0.008 REF						
Z	1.00 REF		0.039 REF						
θ	0°	7°	0°	7°					
θ1	0°	---	0°	---					
θ2	12° REF		12° REF						
θ3	12° REF		12° REF						

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	STANDARD: FREESCALE	
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