SIEMENS

Picture-in-Picture Processor — SDA 9088

Preliminary Data — **MOS IC**

Features

- Input interface compatible to the data format of the Digital Multistandard Decoder (DMSD)SDA 9050/51 if Y, U, V output is used
- Decimation of the Y, U, V data for pictures sizes 1/9 and 1/16
- Intermediate storage of the inset picture (on-chip-memory)
- Readout of the data in the parent window, framing, generation of a SELECT signal
- Interpolation of the chrominance data rate to the luminance data rate
- RGB- or Y-, U-, V-signal generation
- D/A conversion
- Generation of an internal parent clock for an analog system environment from the sandcastle pulse by means of PLL

Type	Ordering Code	Package
SDA 9088	Q67100-H8630	P-DIP-28
SDA 9088-2	Q67100-H5043	P-DIP-28

Functional Description

The SDA 9088 Picture in Picture (PIP) processor combines two asynchronous picture sources so that a small moving picture (the inset picture) can be superimposed in a moving picture of normal size (the parent picture). The functions of the PIP are as follows **(see block diagram).**

The components of the video signal of the inset source must reach the SDA 9088 in digitized form **(figure 1).** Amplitude resolution of the signal components is 5 bit at a sampling rate of 13.5 MHz for the luminance signal and 3.375 MHz for the chrominance signals.

The PIP handles picture reduction (decimation with horizontally and vertically acting filters), intermediate data storage in an integrated image memory (167.904 bits) as well as the output of the decimated picture.

The picture can be set 1/9 or 1/16 of its original size. In order to indicate the border between parent picture and inset picture the inset picture can be surrounded with a frame. Different signal sources can be identified by using different framing colors. The four corners of the parent picture are possible positions for the inset picture. The inset picture can also be inserted as a still picture, independently of the parent picture.

The output signals of the PIP are analog. Either RGB or Y, U, V signals can be output, whereby a 6-bit, broadband conversion is obtained in all components. If Y, U, V are selected, the inset picture signals must be clamped externally before switching between inset and parent channels. The sandcastle pulse of the parent channel can be used to control the clamping circuit. Clamping for RGB output signal is performed in an RGB processor (e.g. TDA 4580).

Only a few additional devices are required for a complete picture-in-picture system. **Application circuits 1 and 2** illustrate two possibilities for use of the PIP device. It can be operated both in systems with analog or digital signal processing or in any combinatioof the two.

If the CVBS input signal is to be decoded using an analog color decoder for the PIP, the analog/digital interface for the inset picture (ADIIP, SDA 9087) performs the conversion of the Y, U, V components into digital signals as well as the generation of the inset clocks BLNI and LL3I.

The PIP processes both 50 Hz/625 and 60 Hz/525 line signals. The field frequency can be 50 Hz or 60 Hz. For systems with Siemens TV feature box a field frequency of 100 Hz or 120 Hz is also possible by doubling the clock frequency LL3P (LL1.5P). Frame reproduction with 50 Hz or 60 Hz can also be set via the I^2C bus. Adaptation to the number of lines occurs automatically. If the field frequencies in the parent and inset channels are different, artifacts may result in the picture.

An unfavourable phase, varying with time, of the sync signals and clock of the parent channel may produce jumps in the position of the inset picture on the TV screen by a line or a pixel (ragged vertical borders). Similar condition for the sync signals of the inset channel may lead to slight instability within the inset picture.

Synchronization with the parent channel is performed via the horizontal and vertical sync signals HPS/SAND and VSP plus the LL3P clock (13.5 MHz) or in the case of standard conversion via the LL1.5P clock (27 MHz).

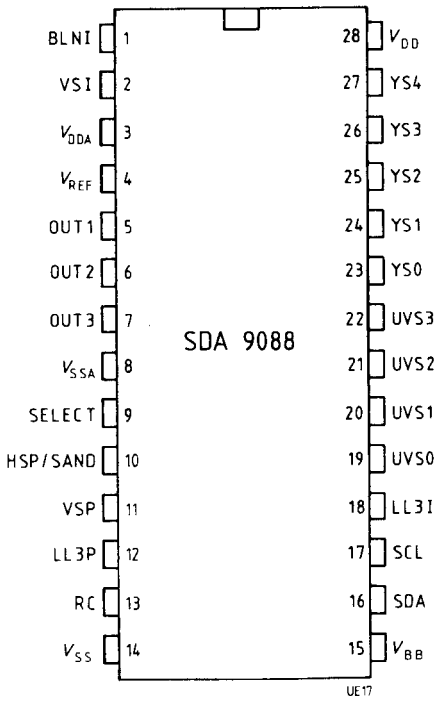
For an analog parent channel the LL3P clock can be generated from the sandcastle pulse (SAND) by an internal PLL.

The horizontal and vertical sync signals BLNI and VSI plus the LL3I clock (13.5 MHz) are used for synchronization with the inset source.

The interface between inset and parent channel is done by the on-chip memory. The memory write access is controlled by the inset clock and the read access controlled by the parent clock.

The SELECT output signal inserts the inset picture into the parent picture driving an external analog switch, e.g. the TDA 4580. All operation modes of the PIP can be controlled via the I^2C bus. Five registers can be used.

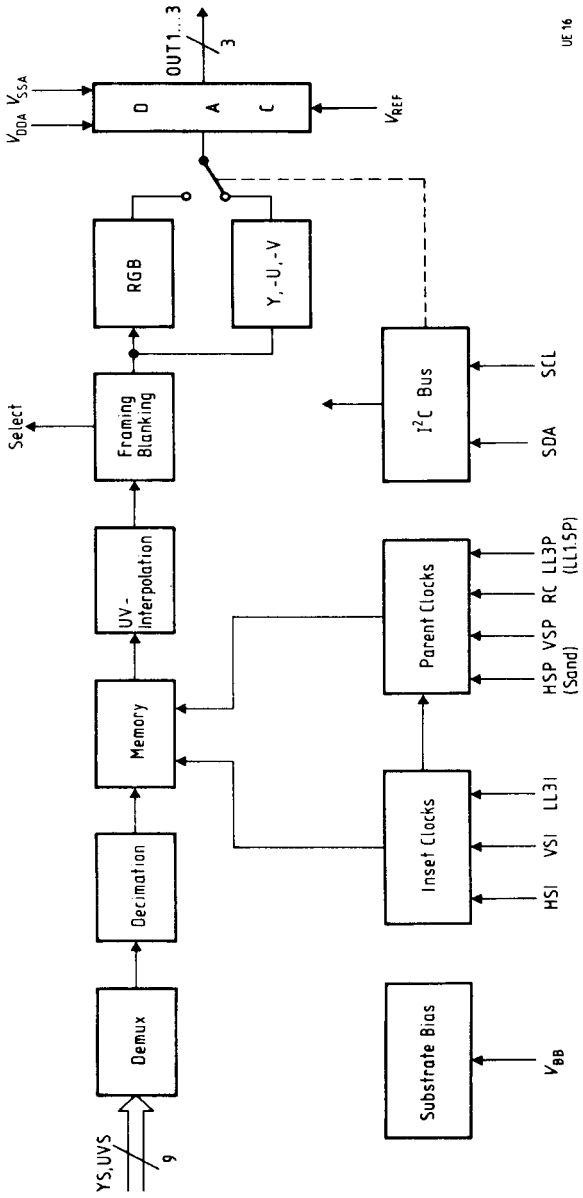
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No	Symbol	Function	Definition
1	BLNI	Blanking inset	Inset lines synchronization
2	VSI	Vertical synchron inset	Inset field synchronization
3	V_{DDA}	Analog supply	V_{DD} power supply for D/A converter and PLL
4	V_{REF}	Reference voltage generation	Current mirror for OUT1-OUT3
5-7	OUT1-OUT3	Analog R, G, B, Y, UV-outputs	Analog RGB-, YUV outputs
8	V_{SSA}	Analog ground	Ground for D/A converter and PLL
9	SELECT	SELECT	Valid signals at OUT1-OUT3
10	HSP/SAND	Horizontal synchron/ Sandcastle parent	Parent line synchronization
11	VSP	Vertical synchron parent	Parent field synchronization
12	LL3P	Line locked clock parent	Parent system clock
13	RC	RC	RC network for PLL loop to V_{SSA}
14	V_{SS}	Digital ground	Ground
15	V_{BB}	Substrate bias	V_{BB} smoothing
16	SDA	Serial data	I²C data
17	SCL	Serial clock	I²C clock
18	LL3I	Line locked clock inset	Inset system clock
19-27	UV0-UV3, Y0-Y4	UV, Y data	Digital YUV input data
28	V_{DD}	Digital supply	V_{DD} delay

Block Diagram



Circuit Description

The DMSD compatible data are transferred under the control of LL3I, BLNI and VSI on pins YS0-YS4 and UVS0-UVS3. The decimated data are stored automatically. Either R, G, B or Y, U, V analog signals are available at the outputs OUT1-OUT3. The validity of the signals is identified by SELECT = 1. In a digital system environment the input is controlled by LL3P, HSP and VSP. In an analog system environment a line frequency signal has to be applied to the pin called SAND. An internal PLL can then generate the internal output clock pulses. In this case an RC network must be connected to pin RC to act as part of a low-pass filter.

Inset Data Reduction

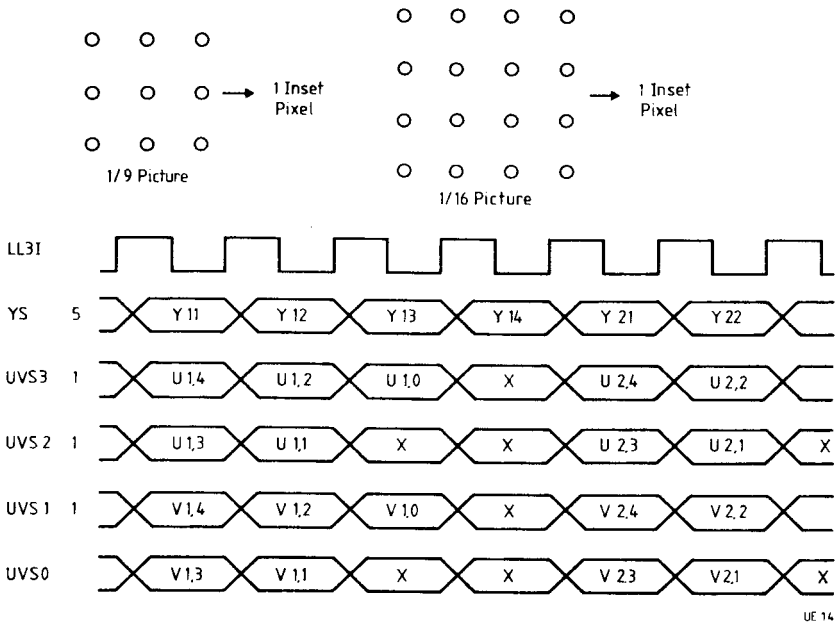
The data rate at the inputs YS0-YS4, UVS0-UVS3 is 13.5 MHz in multiplexed format (DMSD compatible), **see figure 1.**

In order to reduce the quantity of data which have to be stored and to prevent artifacts in the inset picture, nine pixels are processed into an inset pixel for a 1/9 picture and 16 pixels for 1/16 picture.

This is done by horizontal and vertical averaging of pixels:

Figure 1

Input Data Format



The pixel and line number of the inset picture depend on the standard of the inset channel and on the selected picture size:

Table 1

Inset Picture Size

Picture Size	TV Standard (Inset) (Frame Line Number)	Pixel Number P			Line Number L
		Y	U	V	
1/9	625	212	53	53	88
1/9	525	212	53	53	76
1/16	625	160	40	40	66
1/16	525	160	40	40	57

Intermediate Storage of Inset Picture

The PIP memory has a capacity of 167.904 bits large enough to store the data of the inset picture and to output data, which are synchronized with the parent channel. The memory organisation is 88 × 212 × 9 bits. Its size is oriented on the maximum pixel and line number required (1/9 picture, 625 lines).

Data are written in with the inset and read out with the parent clock frequency.

Table 2 shows the processed sections of the original picture stored in the memory.

To avoid strong 25-Hz flicker, only every second field of the inset source is processed.

Table 2

Processed Sections of Original Picture (BWL, BWP = Starting Point)

Picture Size	TV Standard (Inset) (Frame Line Number)	Pixel Number P		Section	
		TV Line (BWL)	Pixel (BWP)	Line Number	Pixel Number
1/9	625	36	13	264	636
1/9	525	26	13	228	636
1/16	625	36	17	264	640
1/16	525	26	17	228	640

Output of Data in Parent Window

The four corners of the parent picture are foreseen as positions for inserting the inset picture. To enable compatibility to different system configurations, readout from memory can be shifted horizontally in 63 steps by max. 252 LL3P cycles and vertically in 15 steps by max. 30 lines in the parent field setting the control bits RDH and RDV in control register 2 and 3.

The coordinates BRP, BRL of the normal location of all four insertion positions are given in **table 4** for RDH = RDV = 8.

The SELECT signal goes high during the display of the inset picture. Outside of the inset picture SELECT signal is low and the analog outputs OUT1-OUT3 provide the black level. The external wiring can produce a delay between the SELECT signal and the analog outputs. This delay can be compensated for by bits SD0-SD2 in register 2 via the I^2C bus.

A frame with one of eight colors can be inserted using control bits FRON, COL0-2. The width of the frame is fixed at three lines and six pixels. The size is shown in **table 3.**

Figure 2

Insertion Positions of Inset Picture

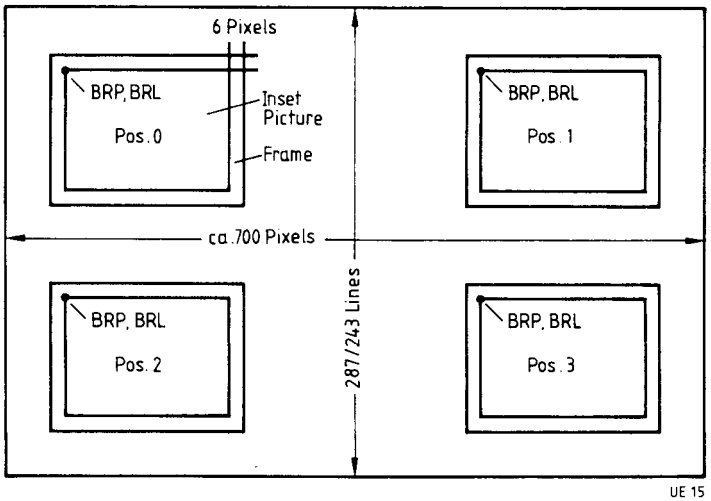


Table 3

Frame Size

Picture Size (with Frame)	TV Standard (Inset)	TV Standard (Parent)	POS	Horiz. Bar		Vert. Bar	
				Pixel Number	Line Number	Pixel Number	Line Number
1/9	625	X	0	224	3	6	94
1/9	625	X	1	224	3	6	94
1/9	525	X	0	224	3	6	82
1/9	525	X	1	224	3	6	82
1/16	625	X	0	172	3	6	72
1/16	625	X	1	172	3	6	72
1/16	525	X	0	172	3	6	63
1/16	525	X	1	172	3	6	63
1/9	X	625	2	224	3	6	94
1/9	X	625	3	224	3	6	94
1/9	X	525	2	224	3	6	94[1)]
1/9	X	525	3	224	3	6	94[1)]
1/16	X	625	2	172	3	6	72
1/16	X	625	3	172	3	6	72
1/16	X	525	2	172	3	6	63
	X	525	3	172	3	6	63

X = don't care

1) Clamping to minimal RDV if a 625-standard picture has to be inserted; the vertical position cannot be changed by software.

Table 4

Display of Inset Picture

Position	TV Standard (Parent) (Frame Line Number)	Picture Size	Location of Top Left Corner Point		
			TV Line (FL)		Pixel (FP)
			NINT	INT	
0	625	X	59	30	54
0	525	X	43	22	54
1	625	1/9	59	30	448
1	525	1/9	43	22	448
1	625	1/16	59	30	502
1	525	1/16	43	22	502
2	625	1/9	367	184	54
2	525	1/9	295	148	54
2	625	1/16	411	206	54
2	525	1/16	335	168	54
3	625	1/9	367	184	448
3	525	1/9	295	148	448
3	625	1/16	411	206	502
3	525	1/16	335	168	502

Pixel data related to positive HSP edge
Line data related to positive VSP edge

Interpolation of Chrominance Data Rate to Luminance Data Rate

To avoid chrominance artifacts after D/A conversion and for digital RGB conversion, the data rate of the chrominance signals is quadrupled in order to match the luminance data rate. This is done by repeating the chrominance data twice followed by low-pass filtering.

RGB, Y, U, V Outputs

A digital RGB matrix converts the Y, U, V data in R, G, B data. The outputs of the matrix are:

$$R = Y + 0.75\ V$$
$$G = Y - 0.375\ V - 0.1875\ U$$
$$B = Y + U$$

If not required a by-pass can be switched allowing the Y, U, V data to reach the D/A converters at the output of the RGB matrix, the chrominance signals U and V being inverted at the same time.

D/A Conversion

SDA 9088 includes three 6-bits D/A converters. Each D/A converter delivers a current through an external resistor that is to be connected between OUT1-OUT3 and V_{SS}. The resistor value determines the output voltages **(see application circuit).** The assignment of outputs OUT1-OUT3 to R, G, B and Y, U, V is shown in **table 5.**

Table 5

Assignment of Output Signals to OUT1-OUT3

Output	RGB	YUV
OUT1	R	– V
OUT2	G	Y
OUT3	B	– U

PLL

In an analog system environment (PLLL = 1) the internal PLL can be activated. Input LL3P is switched off in VCO mode. The internally generated output clock rate is:

$f_T = 864 \cdot f\,(SAND)$

I²C BUS

Organization of I²C Bus Registers

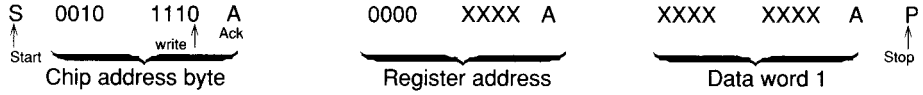
SDA 9088 has the device address

$$00101110 = 2E_H$$

Applying the supply voltage V_{DD} produces a power-up reset. The bus lines SDA and SCL are enabled. All bits in the registers except bit PLL (D3 in Register 0) are set to 0. Bit PLL is set to 1.

The I²C bus interface works as a slave receiver and only functions if the inset clock LL3I is available.

Write Operation



After writing a byte into any register, the register address is automatically incremented for the write access to the next register.

The following table shows the functions that can be set on the I²C bus and define the data bytes.

Table 6

I²C Bus Register

Function	SUB-Address	Data Byte							
		D7	D6	D5	D4	D3	D2	D1	D0
CONTROL 0	00	0	0	STILL	SIZE	PPLL	NINT	OUT	PON
CONTROL 1	01	0	0	0	0	COL2	COL1	COL0	FRON
CONTROL 2	02	0	SD2	SD1	SD0	RDV3	RDV2	RDV1	RDV0
CONTROL 3	03	POS1	POS0	RDH5	RDH4	RDH3	RDH2	RDH1	RDH0
CONTROL 4	04	CON0	CON1	CON2	CON3	HSPINT	SOP	PL27	HSP5

All bits which are not used have to be set to "0".

The bits are numbered in the reverse order to the data stream of the I²C bus.

Register 0 (Address 00_H)

Bit	Function	Name	Remarks
d0	0 = PIP OFF 1 = PIP ON	PON	If d0 = 0, no SELECT generated
d1	0 = Y, -U, -V 1 = RG	OUT	Output format
d2	0 = Field mode 1 = Frame mode	NINT	Reproduction mode
d3	0 = PLL inactive 1 = PLL active	PPLL	Parent clock generation. External clock has to be connected to LL3P is PPLL = 0.
d4	0 = 1/9 1 = 1/16	SIZE	Picture size
d5	0 = normal picture 1 = still picture	STILL	Still/moving picture
d6, d7	not assigned		

Register 1 (Address 01_H)

Bit	Function	Name	Remarks
d0	0 = without frame 1 = with frame	FRON	
d1-d3	frame colour d3 d2 d1 0 0 0 = blue 0 0 1 = violet 0 1 0 = green 0 1 1 = white 1 0 0 = red 1 0 1 = yellow 1 1 0 = orange 1 1 1 = cyan	COL0- COL2	
d4-d7	without function		

Register 2 (Address 02_H)

Bit	Function	Name	Remarks
d0-d3	Read delay vertical in BLNP period d3 d2 d1 d0 0 0 0 0 = 0 0 0 0 1 = 2 0 0 1 0 = 4 : 1 1 0 1 = 26 1 1 1 0 = 28 1 1 1 1 = 30	RDV0– RDV3	Increment in 2 BLNP period
d4-d6	SELECT delay in LL3P period d6 d5 d4 0 0 0 = 0 0 0 1 = 1 0 1 0 = 2 0 1 1 = 3 1 0 0 = 4 1 0 1 = 5 1 1 0 = 6 1 1 1 = 7	SD0- SD2	
d7	without function		

Register 3 (Address 03_H)

Bit	Function	Name	Remarks
d0-d5	Read delay horizontal d5 d4 d3 d2 d1 d0 0 0 0 0 0 0 = 0 0 0 0 0 0 1 = 4 0 0 0 0 1 0 = 2 : 1 1 1 1 0 1 = 244 1 1 1 1 1 0 = 248 1 1 1 1 1 1 = 252	RDH0– RDH5	Increment in 4 LL3P period
d6, d7	Insert picture location d7 d6 0 0 top left 0 1 top right 1 0 down left 1 1 down right	POS0- POS1	

Register 4 (Address 04_H)

Bit	Function	Name	Remarks
d0	0 = SANDCASTLE at HSP 1 = TTL level at HSP	HSP5	Level switch
d1	0 = 13.5 MHz PLL 1 = 27 MHz PLL	PL27	Switch off the VCO clock prescaler
d2	0 = SELECT PULLUP INTERN 1 = SELECT PULLUP EXTERN	SOP	Open drain for SELECT output
d2	0=HSP EXTERN 1=HSP INTERN	HSPINT	HSP from the PLL divider For PLL d3 =1 has to be set
d4-d7	Contrast DA converter	CON 0-3	Applying an external resistor between V_{REF} and V_{SS} the same output voltage is reached if R = 6.8kΩ and d7 ...d4 = 0000 are selected. d4 = LSB d7 = MSB

Absolute Maximum Ratings
T_A = 0 to 70 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 1	6	V
Voltages at V_{BB}*	V_{BB}			V
HSP/SAND	V_{IN}	– 1	10.5	V
All the rest	V_{IN}	– 1	6	V
Ambient temperature	T_A	– 20	70	°C
Storage temperature	T_{stg}	– 20	125	°C
Power dissipation	P_{tot}		1	W

*Note: the voltage V_{BB} is internally generated.

Operating Range
T_A = 25 °C

Supply voltage	V_{DD}	4.5	5.5	V
Ambient temperature	T_A	0	70	°C

Characteristics
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply voltage	V_{DD}/V_{DDA}	4.5	5	5.5	V	
Current consumption dig. analog	I_{DD}	13 5	40 10	70 20	mA mA	without load LL3I = 13.5 MHz LL3P = 27 MHz

Inputs
YS0-YS4, UVS0-UVS3,
LL3I, BLNI, VSI, LL3P, VSP

H-input voltage L-input voltage	V_{IH} V_{IL}	2.3 – 1.0		V_{DD} 0.8	V V	
Input capacitance	C_I			7	pH	
Input leakage current	I_L			10	µA	V_{IH} = 5.5 V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Select						
H-output voltage	V_{QH}	2.4		V_{DD}	V	$-I_{QH}$ = 0.2 mA SOP = 0
L-output voltage	V_{QL}	0		0.4	V	I_{QH} = 1.6 mA SOP = 0
H-output voltage	V_{QH}			V_{DD}	V	SOP = 1
L-output voltage	V_{QL}	0		0.1	V	I_{QL} = 1.6 mA SOP = 1
Load capacitance	C_L			50	pF	
Transition period	t_r, t_f			15	ns	
Input HSP / SAND						
H-input voltage	V_{IH}	2.3		V_{DD}	V	PPLL = 0 or HSP5 = 1
L-input voltage	V_{IL}	− 1.0		0.8	V	PPLL = 0 or HSP5 = 1
H-input voltage	V_{IH}	V_{DD}+2.5 5		10	V	PPLL = 1 and HSP5 = 0
L-input voltage	V_{IL}	0		V_{DD}+0.5 5	V	PPLL = 1 and HSP5 = 0
Input capacitance	C_I			7	pF	
Input leakage current	I_L	− 10		10	µA	$0 \le V \le V_{DD}$ + 0.5 V
Input current	I_{IH}			1	mA	V_{DD} + 2.5 ≤ V_I ≤ 11

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Input SCL, In/Output SDA							
L-input voltage	V_{IL}	– 1		1.5	V		
H-input voltage	V_{IH}	3		V_{DD}	V		
Input leakage current	I_L			10	µA		
Input capacitance	C_I			7	pF		
Input frequency	f_{SCL}			100	kHz		
Transition period	t_r, t_f			2	µs		
Max. capacitance at bus	C_{max}			400	pF		
Fall time	t_f			0.2	µs	from 3 V to 1 V	
SDA by replay message	V_{AL}	0		0.4	V	I_{AL}= 3 mA	
Output OUT1...3, RGB Mode*							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H	V_{QH}		1.07		Vpp	RGB-Mode	6
Output voltage L	V_{QL}	0			mV	RGB-Mode	6
Numerical range		0		63			
Resolution	$I_{Q\,quant}$		25		µA		
Load resistance	R_L		680		Ω		7
Output capacitance	C_Q			7	pF		7
Coupling capacitance	C_C		47		nF		7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range	$V_{Q\,max}$	V_{SSA}		2	V		
Differential non-linearity		– 0.5		0.5	LSB		
Maximum difference between the voltage levels of the RGB outputs at the same full modulation		– 3		3	%		

*The nominal color saturation is achieved in RGB mode by an amplitude ratio of 0.72/0.93/1for Y/U/V at the inputs.

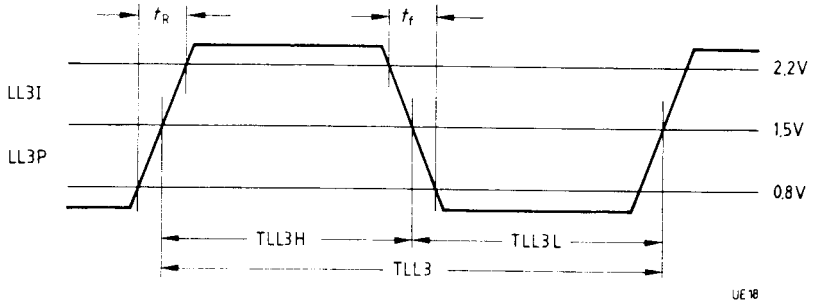
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output OUT1 (V) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H Output voltage L	V_{QH} V_{QL}		1.070		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	$I_{Q\,quant}$		25		µA		
Load capacitance	R_L		680		Ω		7
Output capacitance Coupling capacitance	C_Q C_C		 47	7	pF nF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		
Output OUT2 (V) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA		
Output voltage H Output voltage L	$V_{Q\,H}$ $V_{Q\,L}$		0.43 0		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	I_{Qquant}		25		µA		
Load capacitance	R_L		270		Ω		7
Output capacitance Coupling capacitance	C_Q C_C		 47	7	pF pF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		

Characteristics (cont'd)

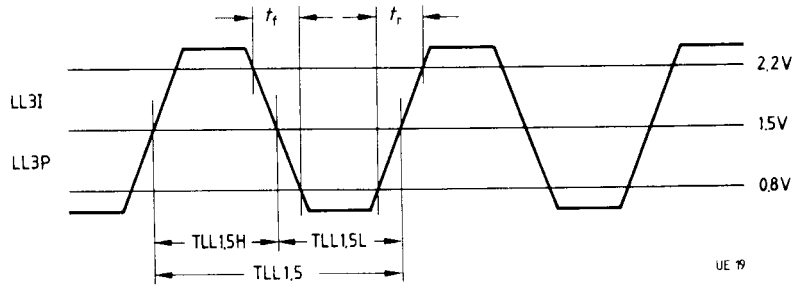
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output OUT3 (U) **YUV Mode**							
Output current	I_Q	0	– 1.57		mA	V_{DDA} = 5 V	
Output voltage H Output voltage L	V_{QH} V_{QL}		1.42 0		Vpp mV	YUV-Mode YUV-Mode	6 6
Numerical range		0		63			
Resolution	I_{Qquant}		25		µA		
Load capacitance	R_L		900		Ω		7
Output capacitance Coupling capacitance	C_Q C_C		 47	7	pF nF		7 7
Time constant	t_{const}			35	ns	BW = 4.5 MHz	7
Output voltage range		V_{SSA}		2	V		
Differential non-linearity Maximum difference between the voltage levels of the YUV outputs at the same full modulation.		– 0.5 – 3		0.5 3	LSB %		
Output RC							
Pulse current	I_P		0.8		mA		8
First external capacitance Second external capacitance	C_1 C_2		22 470		µF µF		
Resistance	R		4.7		kΩ		
Output capacitance	C_Q			7	pF		

Measuring Circuit 1



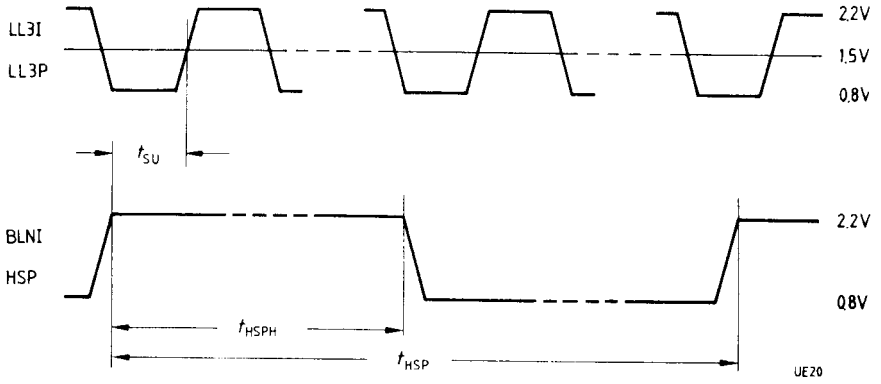
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LL3I, LL3P					
Period time	T_{LL3}	68	74	80	ns
Rise time	t_r			3	ns
Fall time	t_f			3	ns
Sampling ratio	T_{LL3H}/T_{LL3}	0.43		0.57	

Measuring Circuit 2



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
LL1.5P					
Period time	$T_{LL1.5}$	34	37	40	ns
Rise time	t_r			3	ns
Fall time	t_f			3	ns
Sampling ratio	$T_{LL1.5H}/T_{LL1.5}$	0.43		0.57	

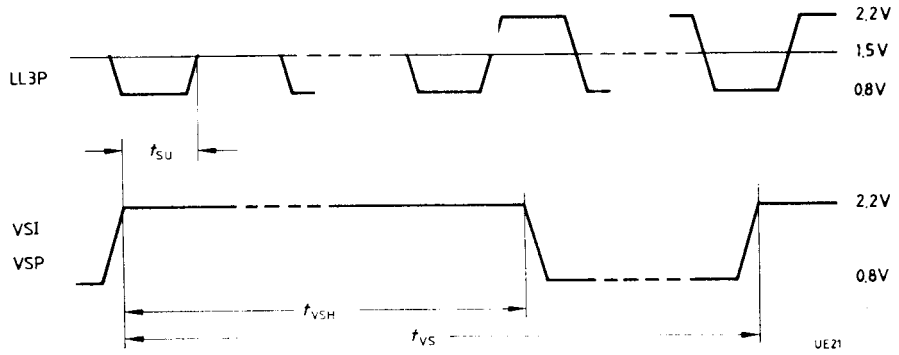
Measuring Circuit 3



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
BLNI					
Period time 625 lines	t_{BLN}	864	864	864	T_{LL3I}
Period time 525 lines	t_{BLN}	858	858	864	T_{LL3I}
High time	t_{BLNH}	1		857	T_{LL3I}
Set-up time	t_{SU}	12			ns
HSP					
Period time 625 lines	t_{HSP}	864	864	864	$T_{LL3P}/T_{LL1.5P}$*
Period time 525 lines	t_{HSP}	858	858	864	$T_{LL3P}/T_{LL1.5P}$*
High time	t_{HSP}	1		857	$T_{LL3P}/T_{LL1.5P}$*
Set-up time	t_{SU}	12			ns

*by standard conversion

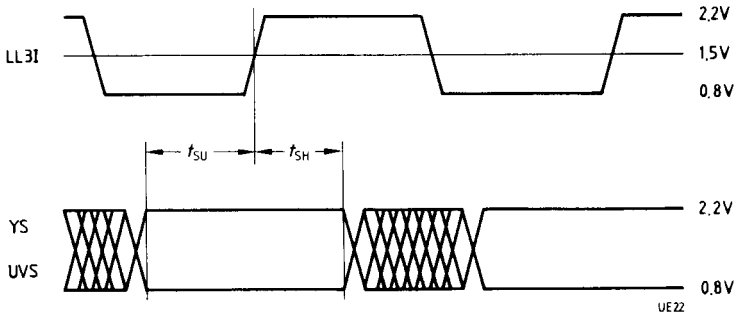
Measuring Circuit4



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
VSI					
Period time 625 lines	t_{VS}		312.5		T_{BLNI}
Period time 525 lines	t_{VS}		262.5		T_{BLNI}
High time	t_{VSH}	1			T_{LL3I}
Set-up time	t_{SU}	12			ns
VSP					
Period time 625 lines	t_{VS}		312.5/625*		T_{HSP}
Period time 525 lines	t_{VS}		262.5/525*		T_{HSP}
High time	t_{VSH}	1			T_{LL3P}
Set-up time	t_{SH}	12			ns

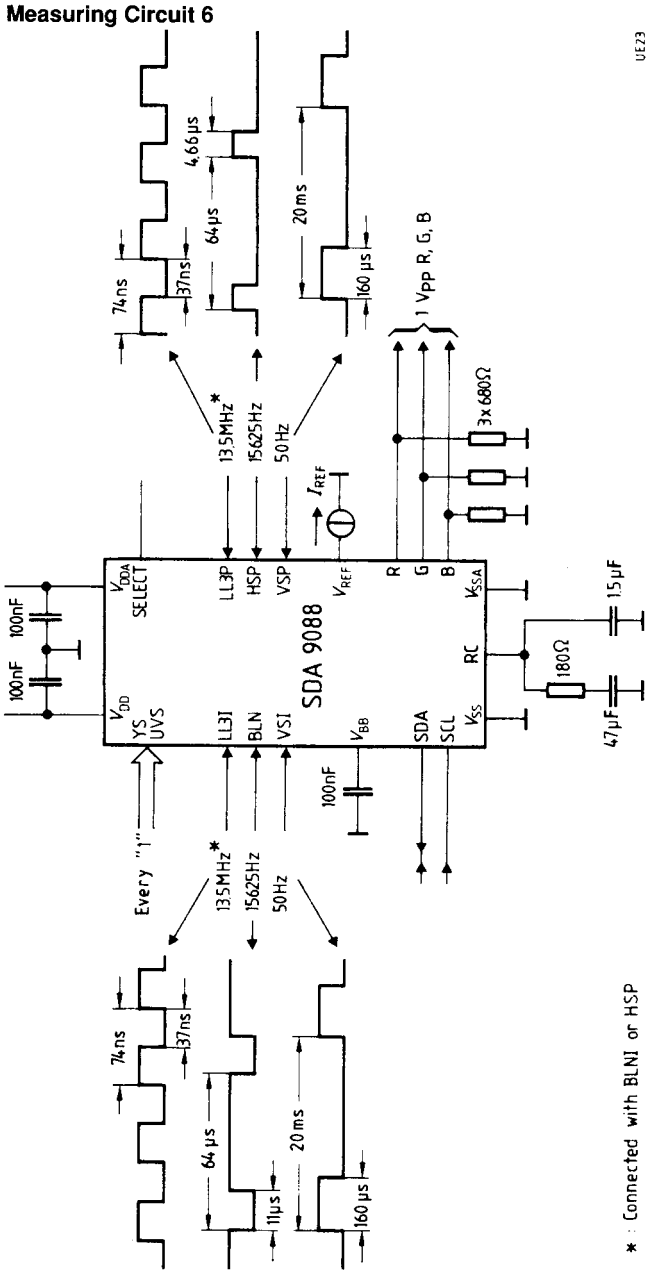
*by progressive scanning

Measuring Circuit 5

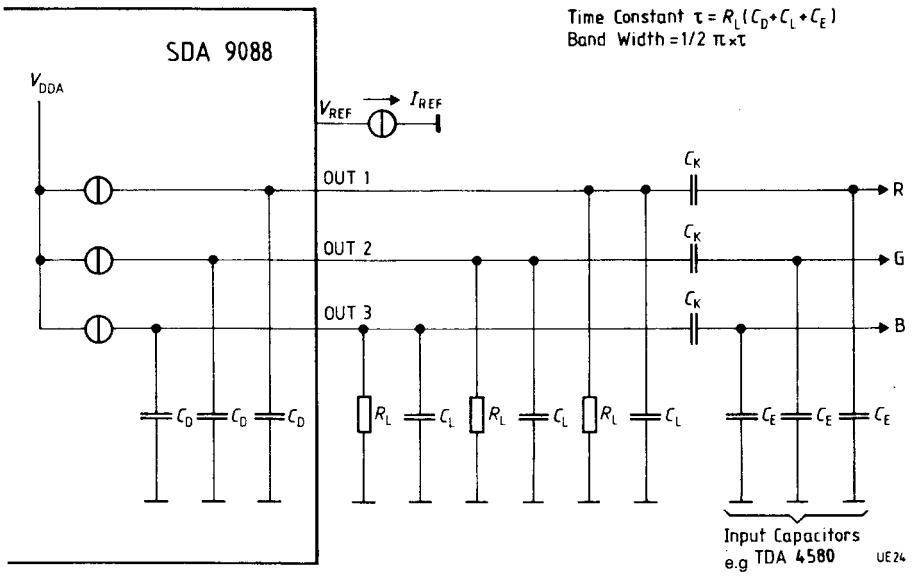


Parameter	Symbol	Limit Values		Unit
		min.	max.	
YS, UVS				
Set-up time	t_{SU}	12		ns
Hold time	t_{SH}	3		ns

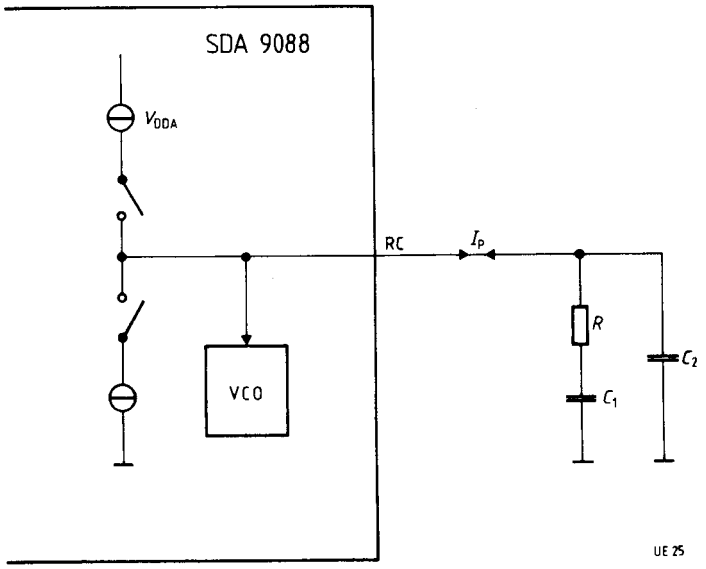
Measuring Circuit 6



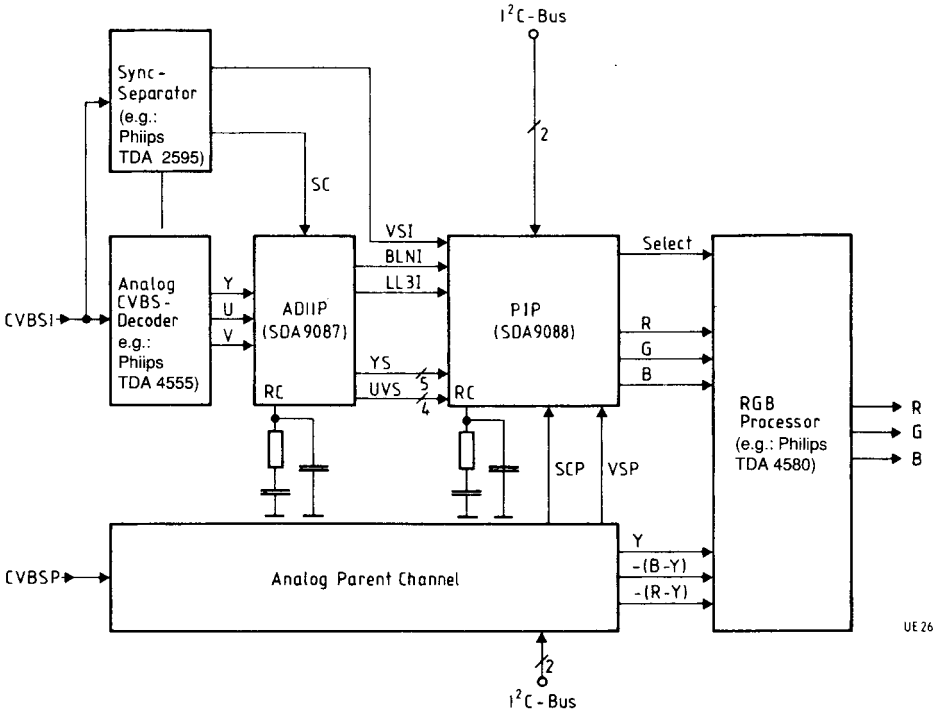
Measuring Circuit 7



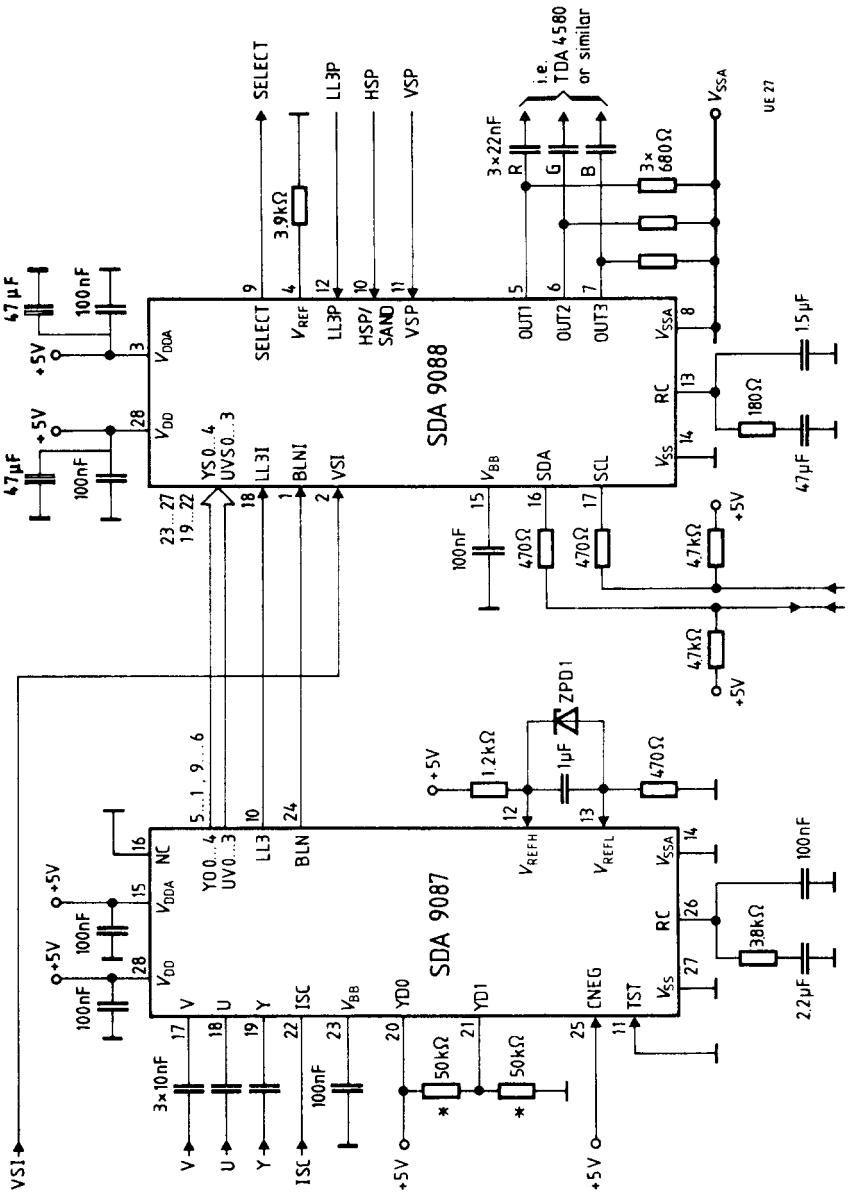
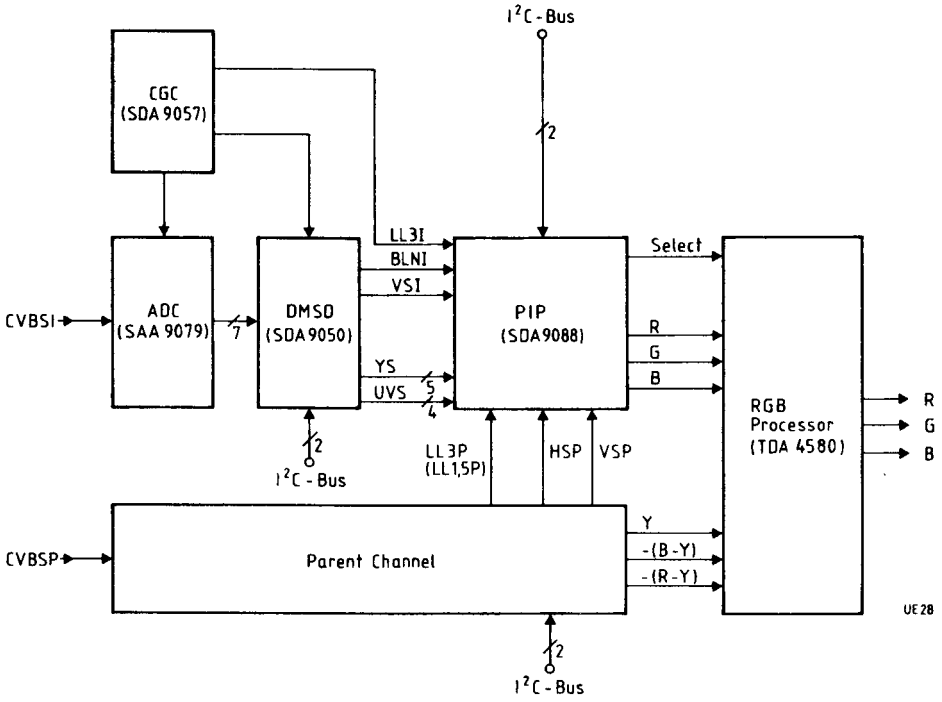
Measuring Circuit 8



Application Circuit 1a



Application Circuit 1b



Application Circuit 2