SC624

LED Light Management Unit

Charge Pump, 4 LEDs, Dual LDOs, and SemWire™ Interface

POWER MANAGEMENT

Features

- Input supply voltage range — 3.0V to 5.5V
- Charge pump modes — 1x, 1.5x and 2x
- Four programmable current sinks with 32 steps from 0.5mA to 25mA
- Two user-configurable 100mA low-noise LDO regulators
- Charge pump frequency — 250kHz
- SemWire™ single wire interface — up to 75kbit/s
- Backlight current accuracy ±1.5% typical
- Backlight current matching ±0.5% typical
- Programmable fade-in/fade-out for main backlight
- Automatic sleep mode (LEDs off) — I_Q = 100µA
- Low shutdown current — 0.1µA (typical)
- Ultra-thin package — 3mm x 3mm x 0.6mm
- Fully WEEE and RoHS compliant

Applications

- Cellular phone backlighting
- PDA backlighting
- Camera I/O and core power

Description

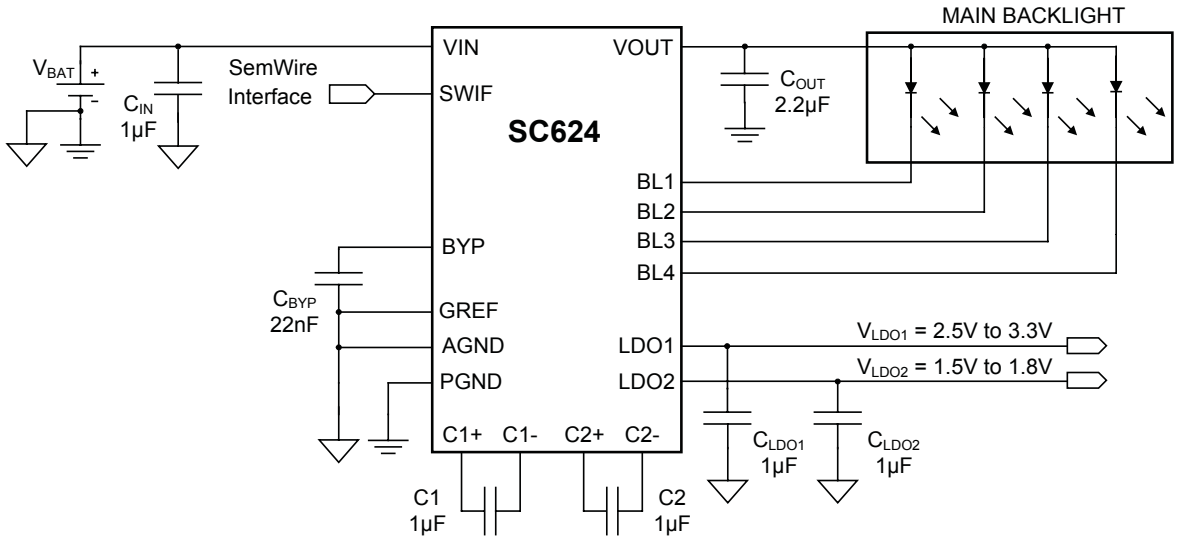
The SC624 is a high efficiency charge pump LED driver using Semtech's proprietary mAhXLife™ technology. Performance is optimized for use in single-cell Li-ion battery applications.

The charge pump provides backlight current in conjunction with four matched current sinks. The load and supply conditions determine whether the charge pump operates in 1x, 1.5x, or 2x mode. An optional fading feature that gradually adjusts the backlight current is provided to simplify control software. The SC624 also provides two low-dropout, low-noise linear regulators for powering a camera module or other peripheral circuits.

The SC624 uses the proprietary SemWire™ single wire interface. The interface controls all functions of the device, including backlight current and two LDO voltage outputs. The single wire implementation minimizes microcontroller and interface pin counts.

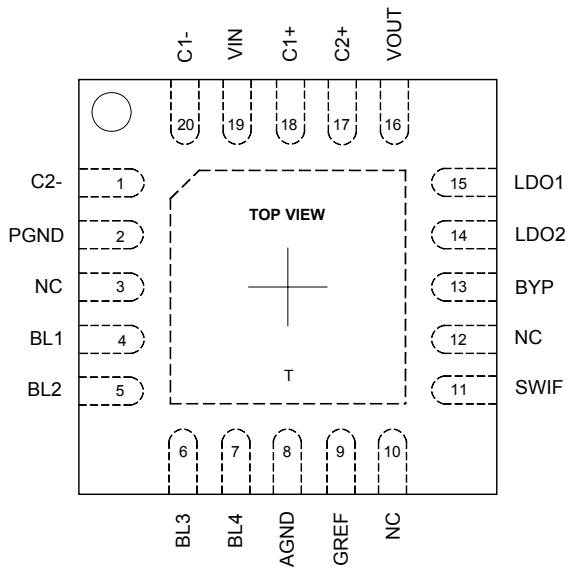
In sleep mode, the device reduces quiescent current to 100µA while continuing to monitor the serial interface. The two LDOs can be enabled when the device is in sleep mode. Total current reduces to 0.1µA in shutdown.

Typical Application Circuit



US Patents: 6,504,422; 6,794,926

Pin Configuration



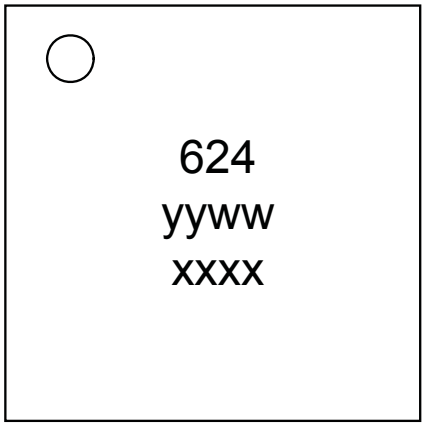
MLPQ-UT-20; 3x3, 20 LEAD
θ_{JA} = 35°C/W

Ordering Information

Device	Package
SC624ULTRT(1)(2)	MLPQ-UT-20 3×3
SC624EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



yyww = Date Code
xxxx = Semtech Lot No.

Absolute Maximum Ratings

VIN (V) ..... -0.3 to +6.0
VOUT (V) ..... -0.3 to +6.0
C1+, C2+ (V) ..... -0.3 to (V_{OUT} + 0.3)
Pin Voltage — All Other Pins (V) ..... -0.3 to (V_{IN} + 0.3)
VOUT Short Circuit Duration ..... Continuous
VLDO1, VLDO2 Short Circuit Duration ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \leq T_A \leq +85$
VIN (V) ..... $3.0 \leq V_{IN} \leq 5.5$
VOUT (V) ..... $2.5 \leq V_{OUT} \leq 5.25$
Voltage Difference between any two LEDs (V) ..... ≤ 1.2

Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) 35
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted, T_A = +25°C for Typ, -40°C to +85°C for Min and Max, $T_{J(MAX)}$ = 125°C, V_{IN} = 3.0V to 4.2V, C_{IN}= C_1= C_2= 2.2µF, C_{OUT} = 4.7µF (ESR = 0.03Ω), $\Delta V_F \leq 1.2V$[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Specifications						
Shutdown Current	$I_{Q(OFF)}$	Shutdown, V_{IN} = 4.2V		0.1	2	µA
Total Quiescent Current	I_Q	Sleep (LDOs off), SWIF = V_{IN}		100	160	µA
		Sleep (LDOs on), SWIF = V_{IN}, $V_{IN} > (V_{LDO} + 300mV)$, $I_{LDO} \leq 200mA$		220	340	
		Charge pump in 1x mode, 4 backlights on		3.8	4.65	mA
		Charge pump in 1.5x mode, 4 backlights on		4.6	5.85	
		Charge pump in 2x mode, 4 backlights on		4.6	5.85	
Fault Protection						
Output Short Circuit Current Limit	$I_{OUT(SC)}$	VOUT pin shorted to GND		300		mA
Over-Temperature	T_{OTP}			160		°C

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Fault Protection (continued)						
Charge Pump Over-Voltage Protection	V_{OVP}	VOUT pin open circuit, $V_{OUT} = V_{OVP}$ rising threshold	5.3	5.7	6.0	V
Undervoltage Lockout	V_{UVLO}	Decreasing V_{IN}		2.4		V
	$V_{UVLO-HYS}$			300		mV
Charge Pump Electrical Specifications						
Maximum Total Output Current	$I_{OUT(MAX)}$	$V_{IN} > 3.4V$, sum of all active LED currents, $V_{OUT(MAX)} = 4.2V$	100			mA
Backlight Current Setting	I_{BL}	Nominal setting for BL1 thru BL4	0.5		25	mA
Backlight Current Accuracy	I_{BL_ACC}	$V_{IN} = 3.7V$, $I_{BL} = 12mA$, $T_A = 25°C$	-8	±1.5	+8	%
Backlight Current Matching	I_{BL-BL}	$V_{IN} = 3.7V$, $I_{BL} = 12mA$ (2)	-3.5	±0.5	+3.5	%
1x Mode to 1.5x Mode Falling Transition Voltage	$V_{TRANS1x}$	$I_{OUT} = 40mA$, $I_{BLn} = 10mA$, $V_{OUT} = 3.2V$		3.27		V
1.5x Mode to 1x Mode Hysteresis	V_{HYST1x}	$I_{OUT} = 40mA$, $I_{BLn} = 10mA$, $V_{OUT} = 3.2V$		250		mV
1.5x Mode to 2x Mode Falling Transition Voltage	$V_{TRANS1.5x}$	$I_{OUT} = 40mA$, $I_{BLn} = 10mA$, $V_{OUT} = 4.0V$ (3)		2.92		V
2x Mode to 1.5x Mode Hysteresis	$V_{HYST1.5x}$	$I_{OUT} = 40mA$, $I_{BLn} = 10mA$, $V_{OUT} = 4.0V$ (3)		300		mV
Current Sink Off-State Leakage Current	I_{BLn}	$V_{IN} = V_{BLn} = 4.2V$		0.1	1	µA
Pump Frequency	f_{PUMP}	$V_{IN} = 3.2V$		250		kHz
LDO Electrical Specifications						
LDO1 Voltage Setting	V_{LDO1}	Range of nominal settings in 100mV increments	2.5		3.3	V
LDO2 Voltage Setting	V_{LDO2}	Range of nominal settings in 100mV increments	1.5		1.8	V
LDO1, LDO2 Output Voltage Accuracy	V_{LDO1}, V_{LDO2}	$V_{IN} = 3.7V$, $I_{LDO} = 1mA$	-3.5	±3	+3.5	%
Line Regulation	ΔV_{LINE}	LDO1, $I_{LDO1} = 1mA$, $V_{OUT} = 2.8V$		2.1	7.2	mV
		LDO2, $I_{LDO2} = 1mA$, $V_{OUT} = 1.8V$		1.3	4.8	

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LDO Electrical Specifications (continued)						
Load Regulation	ΔV_{LOAD}	V_{LDO1} = 3.3V, V_{IN} = 3.7V, I_{LDO1} = 1mA to 100 mA			25	mV
		V_{LDO2} = 1.8V, V_{IN} = 3.7V, I_{LDO2} = 1mA to 100 mA			20	
Dropout Voltage[4]	V_D	I_{LDO1} = 100mA		100	150	mV
Current Limit	I_{LIM}		200			mA
Power Supply Rejection Ratio	$PSRR_{LDO1}$	2.5V < V_{LDO1} < 3V, f < 1kHz, C_{BYP} = 22nF, I_{LDO1} = 50mA, V_{IN} = 3.7V with 0.5V_{P-P} ripple		50		dB
	$PSRR_{LDO2}$	f < 1kHz, C_{BYP} = 22nF, I_{LDO2} = 50mA, V_{IN} = 3.7V with 0.5V_{P-P} ripple		60		
Output Voltage Noise	e_{n-LDO1}	LDO1, 10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDO} = 1µF, I_{LDO1} = 50 mA, V_{IN} = 3.7V, 2.5V < V_{LDO1} < 3V		100		μV_{RMS}
	e_{n-LDO2}	LDO2, 10Hz < f < 100kHz, C_{BYP} = 22nF, C_{LDO} = 1µF, I_{LDO2} = 50 mA, V_{IN} = 3.7V		50		
Minimum Output Capacitor	$C_{LDO(MIN)}$			1		µF
Digital I/O Electrical Specifications (SWIF)						
Input High Threshold	V_{IH}	V_{IN} = 5.5V	1.6			V
Input Low Threshold	V_{IL}	V_{IN} = 3.0V			0.4	V
Input High Current	I_{IH}	V_{IN} = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{IN} = 5.5V	-1		+1	µA
SemWire Bit Rate	f_{SWIF}		10		75	kbit/s
SemWire Start-up Time[5]	t_{EN}		1			ms
SemWire Disable Time[6]	t_{DIS}		10			ms
SemWire Data Latch Delay[7]	D_{DL}			5		bit

Notes:

(1) ΔV_F is the voltage difference between any two LEDs.

(2) Current matching equals ± [$I_{BL(MAX)}$ - $I_{BL(MIN}$] / [$I_{BL(MAX)}$ + $I_{BL(MIN)}$].

(3) Test voltage is V_{OUT} = 4.0V — a relatively extreme LED voltage — to force a transition during test. Typically V_{OUT} = 3.2V for white LEDs.

(4) Dropout is defined as (V_{IN} - V_{LDO1}) when V_{LDO1} drops 100mV from nominal. Dropout does not apply to LDO2 since it has a maximum output voltage of 1.8V.

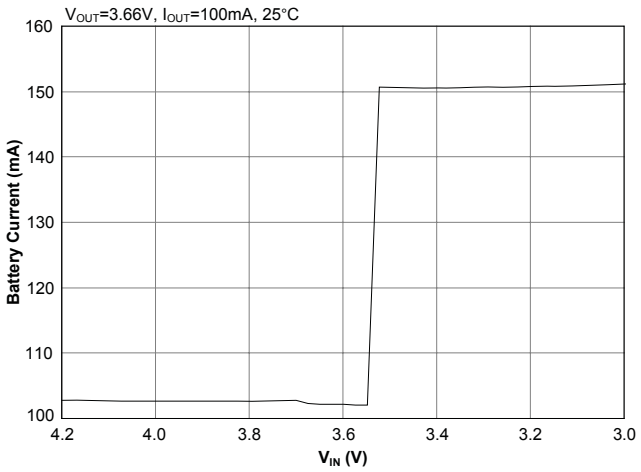
(5) The SemWire start-up time is the minimum period that the SWIF pin must be held high to enable the part before commencing communication.

(6) The SemWire disable time is the minimum period that the SWIF pin must be pulled low to shut the part down.

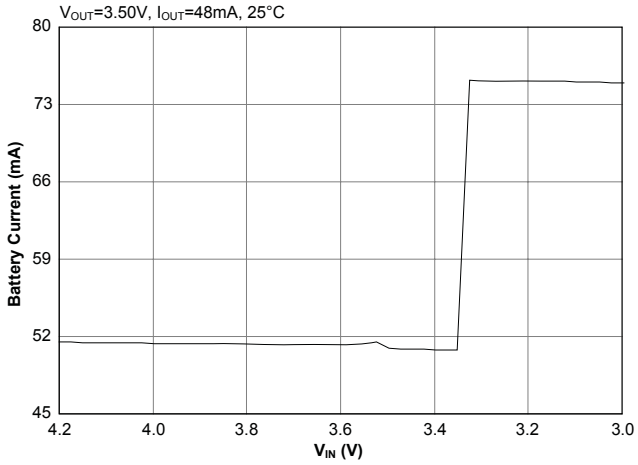
(7) The SemWire data latch delay is the maximum duration after communication has ended before the register is updated.

Typical Characteristics

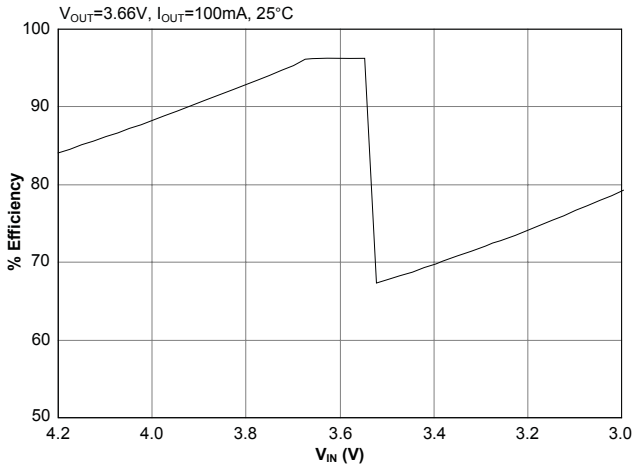
Battery Current (4 LEDs) — 25mA Each



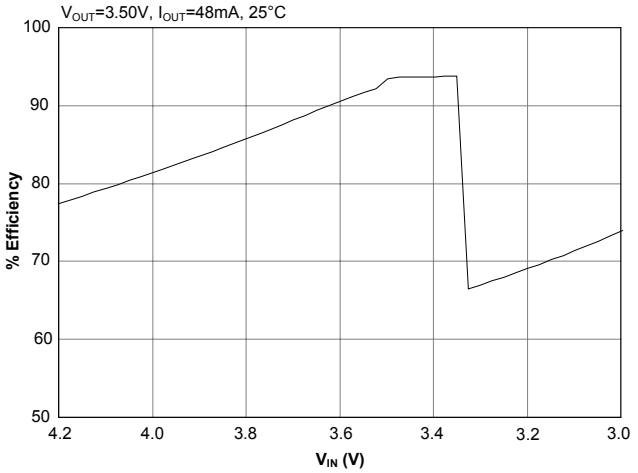
Battery Current (4 LEDs) — 12mA Each



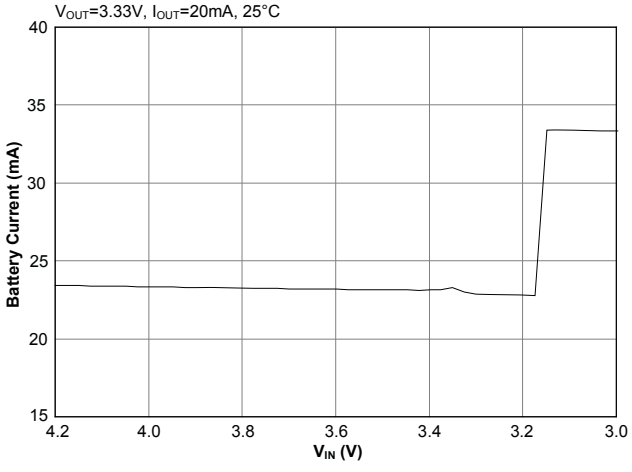
Backlight Efficiency (4 LEDs) — 25mA Each



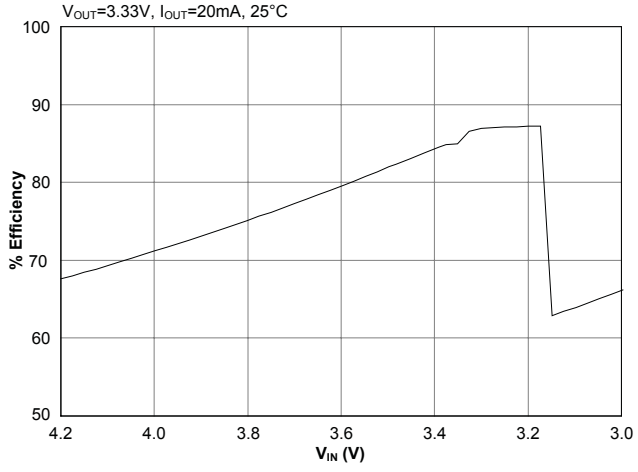
Backlight Efficiency (4 LEDs) — 12mA Each



Battery Current (4 LEDs) — 5.0mA Each

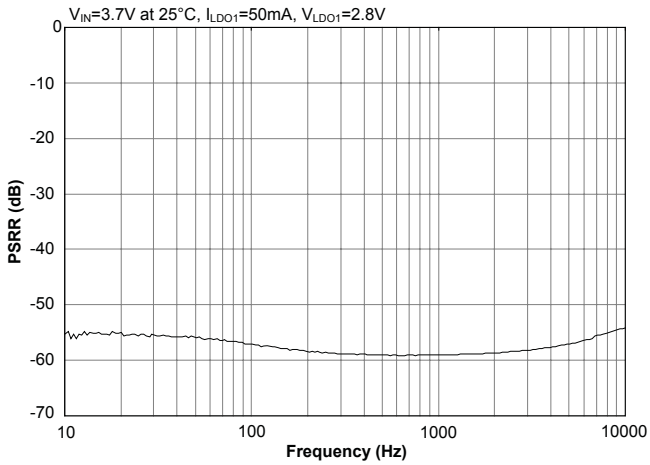


Backlight Efficiency (4 LEDs) — 5.0mA Each

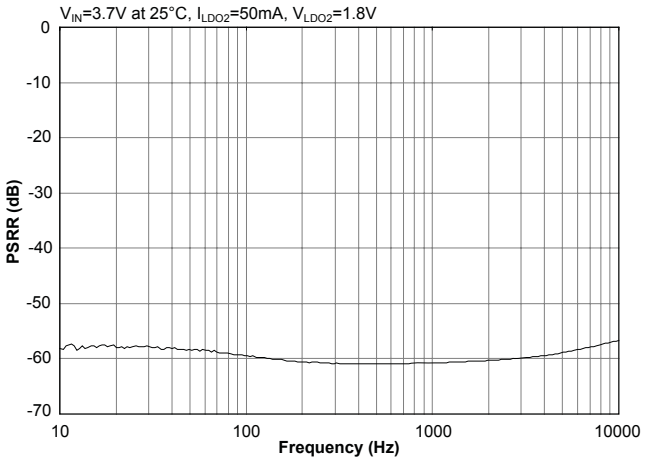


Typical Characteristics (continued)

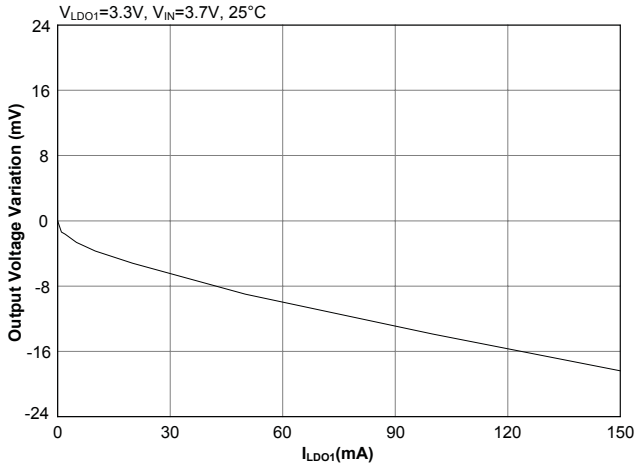
PSRR vs. Frequency (LDO1)



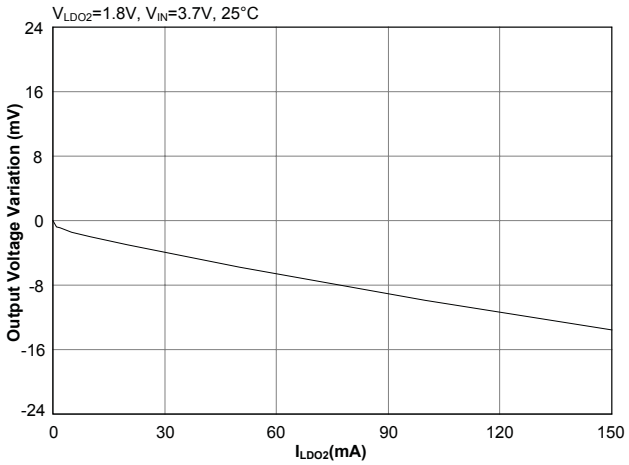
PSRR vs. Frequency (LDO2)



Load Regulation (LDO1)

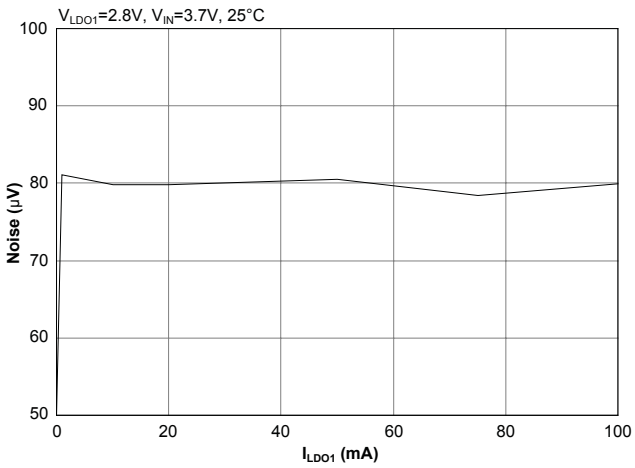


Load Regulation (LDO2)

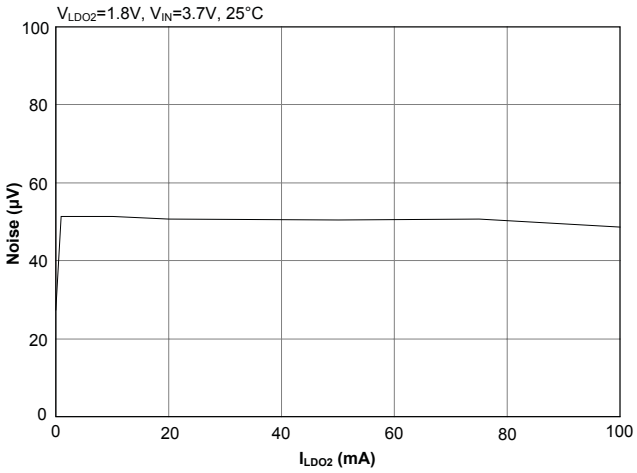


Typical Characteristics (continued)

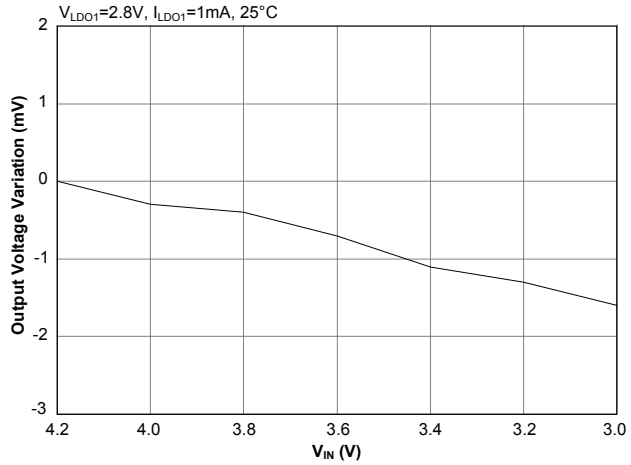
Noise vs Load Current (LDO1)



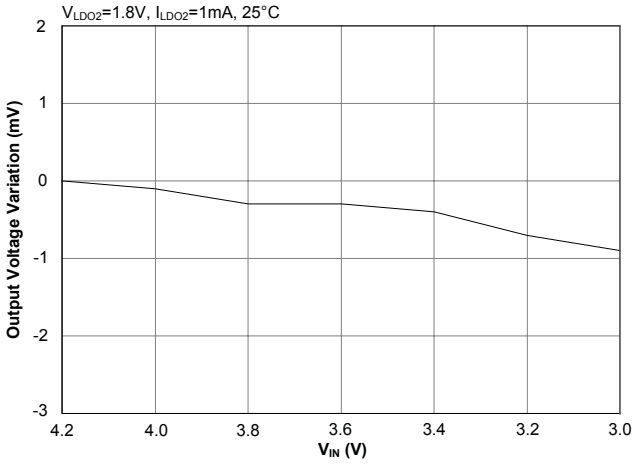
Noise vs Load Current (LDO2)



Line Regulation (LDO1)

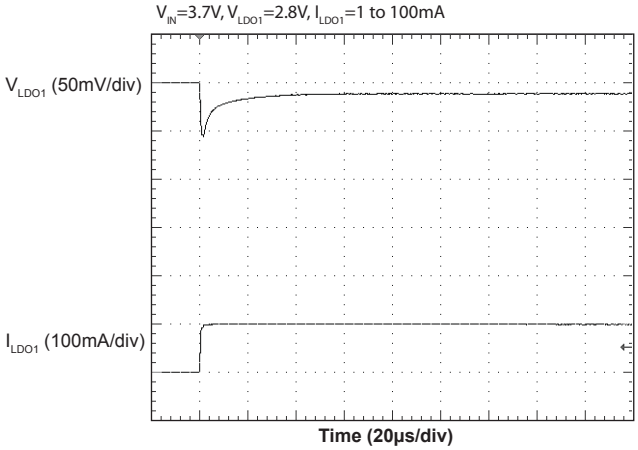


Line Regulation (LDO2)

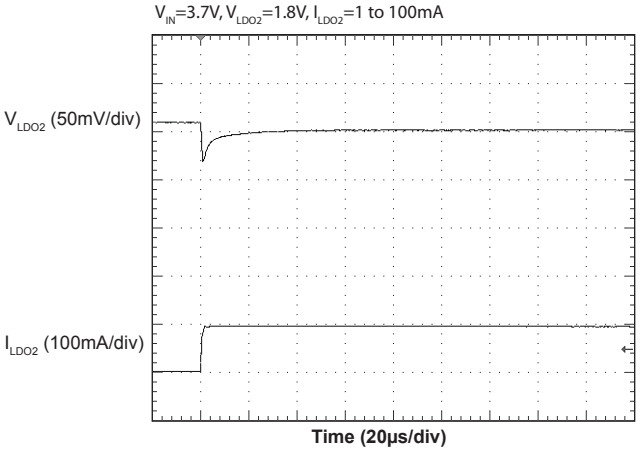


Typical Characteristics (continued)

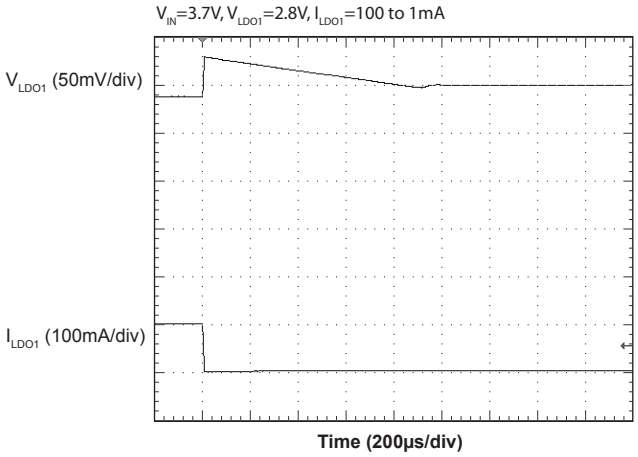
Load Transient Response (LDO1) — Rising Edge



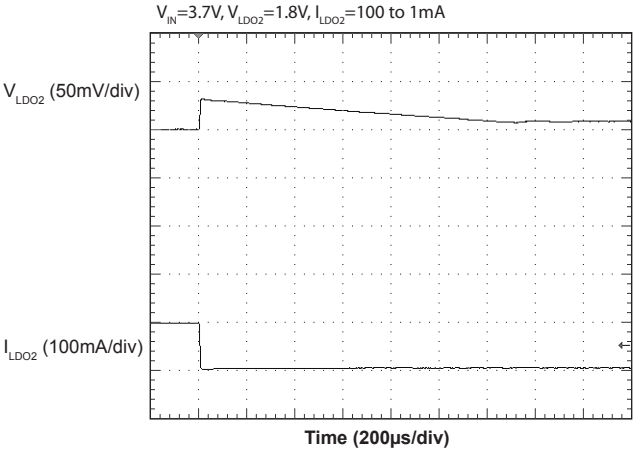
Load Transient Response (LDO2) — Rising Edge



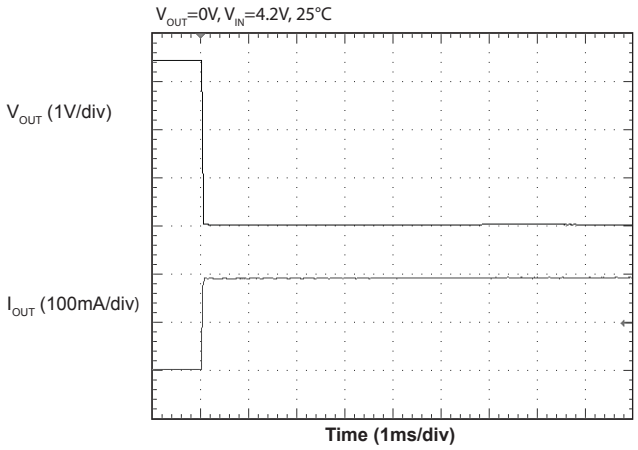
Load Transient Response (LDO1) — Falling Edge



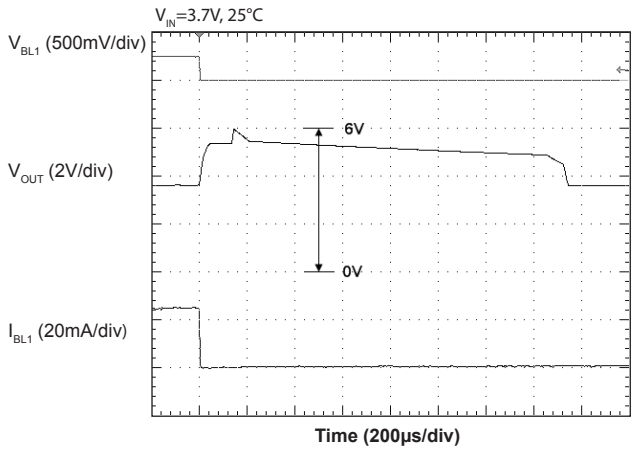
Load Transient Response (LDO2) — Falling Edge



Output Short Circuit Current Limit



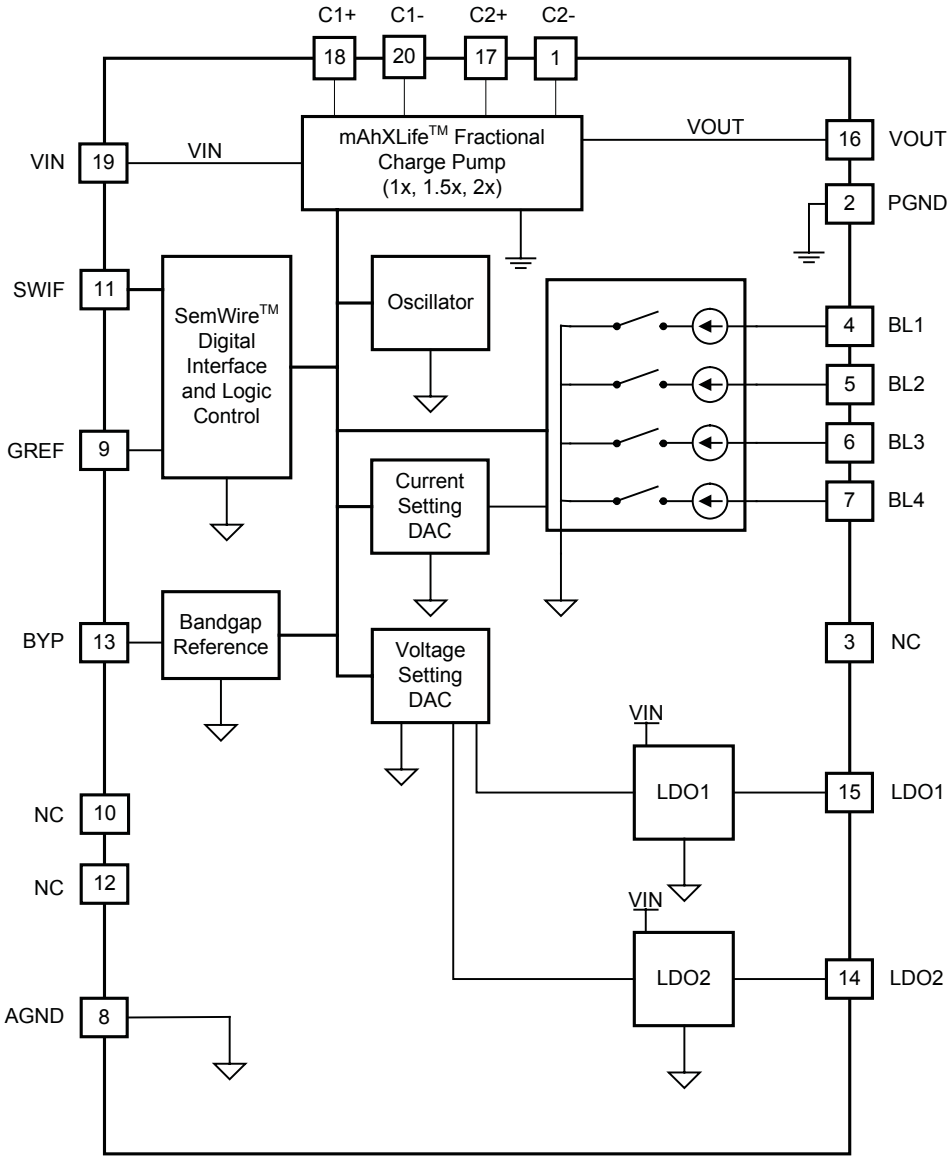
Output Open Circuit Protection



Pin Descriptions

Pin #	Pin Name	Pin Function
1	C2-	Negative connection to bucket capacitor 2 — requires a 1µF capacitor connected to C2+
2	PGND	Ground pin for high current charge pump
3	NC	Unused pin — do not terminate
4	BL1	Current sink output for main backlight LED 1 — leave this pin open if unused
5	BL2	Current sink output for main backlight LED 2 — leave this pin open if unused
6	BL3	Current sink output for main backlight LED 3 — leave this pin open if unused
7	BL4	Current sink output for main backlight LED 4 — leave this pin open if unused
8	AGND	Analog ground pin — connect to ground and separate from PGND current
9	GREF	Ground reference — connect to ground
10	NC	Unused pin — do not terminate
11	SWIF	SemWire single wire interface pin — used to enable/disable the device and to set up all internal registers (refer to Register Map and SemWire Interface sections)
12	NC	Unused pin — do not terminate
13	BYP	Bypass pin for voltage reference — connect with a 22nF capacitor to AGND
14	LDO2	Output of LDO2 — connect with a 1µF capacitor to AGND
15	LDO1	Output of LDO1 — connect with a 1µF capacitor to AGND
16	VOUT	Charge pump output — all LED anode pins should be connected to this pin — requires a 2.2µF capacitor to PGND
17	C2+	Positive connection to bucket capacitor 2 — requires a 1µF capacitor connected to C2-
18	C1+	Positive connection to bucket capacitor 1 — requires a 1µF capacitor connected to C1-
19	VIN	Battery voltage input — connect with a 1µF capacitor to PGND
20	C1-	Negative connection to bucket capacitor 1 — requires a 1µF capacitor connected to C1+
T	THERMAL PAD	Thermal pad for heatsinking purposes — connect to ground plane using multiple vias — not connected internally

Block Diagram



Applications Information

General Description

This design is optimized for handheld applications supplied from a single Li-Ion cell and includes the following key features:

- A high efficiency fractional charge pump that supplies power to all LEDs
- Four matched current sinks that control LED backlighting current, with 0.5mA to 25mA per LED
- Two adjustable LDOs with outputs ranging from 2.5V to 3.3V for LDO1 and 1.5V to 1.8V for LDO2, adjustable in 100mV increments
- A SemWire single wire interface that provides control of all device functions

High Current Fractional Charge Pump

The backlight outputs are supported by a high efficiency, high current fractional charge pump output at the VOUT pin. The charge pump multiplies the input voltage by 1, 1.5, or 2 times. The charge pump switches at a fixed frequency of 250kHz in 1.5x and 2x modes and is disabled in 1x mode to save power and improve efficiency.

The mode selection circuit automatically selects the 1x, 1.5x or 2x mode based on circuit conditions. Circuit conditions such as low input voltage, high output current, or high LED voltage place a higher demand on the charge pump output. A higher numerical mode may be needed momentarily to maintain regulation at the VOUT pin during intervals of high demand, such as the droop at the VIN pin during a supply voltage transient. The charge pump responds to these momentary high demands, setting the charge pump to the optimum mode (1x, 1.5x or 2x), as needed to deliver the output voltage and load current while optimizing efficiency. Hysteresis is provided to prevent mode toggling.

The charge pump requires two bucket capacitors for low ripple operation. One capacitor must be connected between the C1+ and C1- pins and the other must be connected between the C2+ and C2- pins as shown in the typical application circuit diagram. These capacitors should be equal in value, with a minimum capacitance of 1µF to support the charge pump current requirements. The device also requires a 1µF capacitor on the VIN pin and a 2.2µF capacitor on the VOUT pin to minimize noise and support the output drive requirements. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

LED Backlight Current Sinks

The backlight current is set via the SemWire interface. The current is regulated to one of 32 values between 0.5mA and 25mA. The step size varies depending upon the current setting. Between 0.5mA and 12mA, the step size is 0.5mA. The step size increases to 1mA for settings between 12mA and 15mA and 2mA for settings greater than 15mA. This feature allows finer adjustment for dimming functions in the low current setting range and coarse adjustment at higher current settings where small current changes are not visibly noticeable in LED brightness.

All backlight current sinks have matched currents, even when there is variation in the forward voltages (ΔV_F) of the LEDs. A ΔV_F of 1.2V is supported when the input voltage is at 3.0V. Higher ΔV_F LED mis-match is supported when V_{IN} is higher than 3.0V. All current sink outputs are compared and the lowest output is used for setting the voltage regulation at the VOUT pin. This is done to ensure that sufficient bias exists for all LEDs.

The backlight LEDs default to the off state upon power-up. For backlight applications using less than four LEDs, any unused output must be left open and the unused LED driver must remain disabled. When writing to the Backlight Enable Control register, a zero (0) must be written to the corresponding bit of any unused output.

Applications Information (continued)

Backlight Quiescent Current

The quiescent current required to operate all four backlights is reduced by 1.5mA when backlight current is set to 4.0mA or less. This feature results in higher efficiency under light-load conditions. Further reduction in quiescent current will result from using fewer than four LEDs.

Fade-In and Fade-Out

Backlight brightness can be set to automatically fade-in when current is set to increase and fade-out when current is set to decrease. When enabled with a new current setting, the current will step through each incremental setting between the old and new values. The result is a visually smooth change in brightness with a rate of fade that can be set to 8, 16, 24, or 32 ms per step.

Programmable LDO Outputs

Two low dropout (LDO) regulators are provided for camera module I/O and core power. Each LDO has at least 100mA of available load current with ±3.5% accuracy. The minimum current limit is 200mA, so outputs greater than 100mA are possible at somewhat reduced accuracy.

A 1µF, low ESR capacitor should be used as a bypass capacitor on each LDO output to reduce noise and ensure stability. In addition, it is recommended that a minimum 22nF capacitor be connected from the BYP pin to ground to minimize noise and achieve optimum power supply rejection. A larger capacitor can be used for this function, but at the expense of increasing turn-on time. Capacitors with X7R or X5R ceramic dielectric are strongly recommended for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them unsuitable for this application.

Shutdown State

The device is disabled when the SWIF pin is low. All registers are reset to default condition when SWIF is low.

Sleep Mode

When all LEDs are off, sleep mode is activated. This is a reduced current mode that helps minimize overall current consumption by turning off the clock and the charge pump while continuing to monitor the serial interface for commands. Both LDOs can be powered up while in sleep mode.

SemWire Single Wire Interface Functions

All device functions can be controlled via the SemWire single wire interface. The interface is described in detail in the SemWire Interface section of the datasheet.

Protection Features

The SC624 provides several protection features to safeguard the device from catastrophic failures. These features include:

- Output Open Circuit Protection
- Over-Temperature Protection
- Charge Pump Output Current Limit
- LDO Current Limit
- LED Float Detection

Output Open Circuit Protection

Over-Voltage Protection (OVP) is provided at the VOUT pin to prevent the charge pump from producing an excessively high output voltage. In the event of an open circuit at VOUT, the charge pump runs in open loop and the voltage rises up to the OVP limit. OVP operation is hysteretic, meaning the charge pump will momentarily turn off until V_{OUT} is sufficiently reduced. The maximum OVP threshold is 6.0V, allowing the use of a ceramic output capacitor rated at 6.3V with no fear of over-voltage damage.

Over-Temperature Protection

The Over-Temperature (OT) protection circuit helps prevent the device from overheating and experiencing a catastrophic failure. When the junction temperature exceeds 160°C, the device goes into thermal shutdown with all outputs disabled until the junction temperature is reduced. All register information is retained during thermal shutdown.

Applications Information (continued)

Charge Pump Output Current Limit

The device also limits the charge pump current at the VOUT pin (typically 300mA).

LDO Current Limit

The device limits the output currents of LDO1 and LDO2 to help prevent it from overheating and to protect the loads. The minimum limit is 200mA, so load current greater than the rated 100mA can be used with degraded accuracy and larger dropout without tripping the current limit.

LED Float Detection

Float detect is a fault detection feature of the LED current sink outputs. If an output is programmed to be enabled and an open circuit fault occurs at any current sink output, that output will be disabled to prevent a sustained output OVP condition from occurring due to the resulting open loop. Float detect ensures device protection but does not ensure optimum performance. Unused LED outputs must be disabled to prevent an open circuit fault from occurring.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 1 illustrates a proper two-layer PCB layout for the SC624 and supporting components. Following fundamental layout rules is critical for achieving the performance specified in the Electrical Characteristics table. The following guidelines are recommended when developing a PCB layout:

- Place all bypass and decoupling capacitors — C1, C2, CIN, COUT, CLDO1, CLDO2, and CBYP as close to the device as possible.
- All charge pump current passes through VIN, VOUT, and the bucket capacitor connection pins. Ensure that all connections to these pins make use of wide traces so that the resistive drop on each connection is minimized.
- The thermal pad should be connected to the ground plane using multiple vias to ensure proper thermal connection for optimal heat transfer.

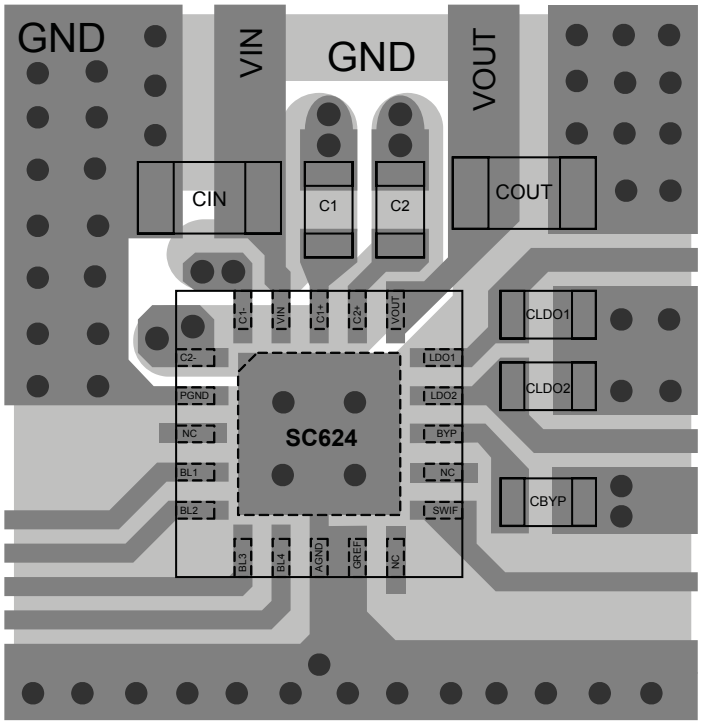


Figure 1 — Recommended PCB Layout

- Make all ground connections to a solid ground plane as shown in the example layout (Figure 3).
- If a ground layer is not feasible, the following groupings should be connected:
  - PGND — CIN, COUT
  - AGND — Ground Pad, CLDO1, CLDO2, CBYP
- If no ground plane is available, PGND and AGND should be routed back to the negative battery terminal as separate signals using thick traces. Joining the two ground returns at the terminal prevents large pulsed return currents from mixing with the low-noise return currents of the LDOs.
- Both LDO output traces should be made as wide as possible to minimize resistive losses.

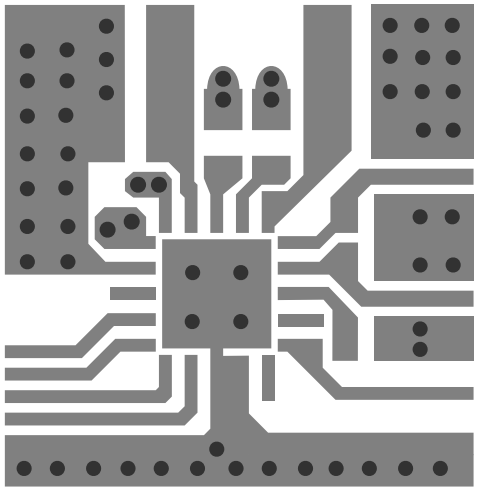


Figure 2 — Layer 1

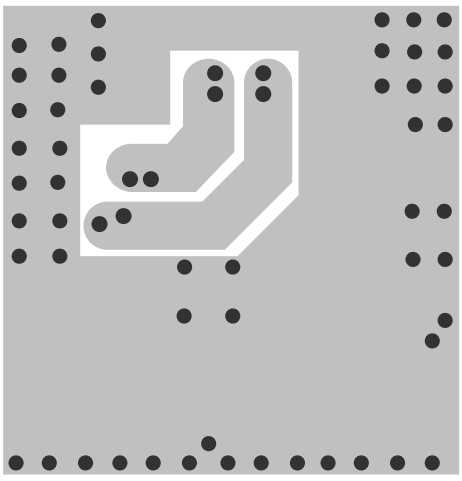


Figure 3 — Layer 2

Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Reset Value	Description
0x00	FADE_1	FADE_0	FADE_EN	BL_4	BL_3	BL_2	BL_1	BL_0	0x00	Backlight Current Control
0x01	0(1)	0(1)	0(1)	0(1)	BLEN_4	BLEN_3	BLEN_2	BLEN_1	0x00	Backlight Enable Control
0x03	0(1)	LDO2_2	LDO2_1	LDO2_0	LDO1_3	LDO1_2	LDO1_1	LDO1_0	0x00	LDO Control

Notes:
(1) 0 = always write a 0 to these bits

Register and Bit Definitions

Backlight Current Control Register (0x00)

This register is used to set the currents for the backlight current sinks, as well as to enable and set the fade step rate. These current sinks need to be enabled in the Backlight Enable Control register to be active.

FADE[1:0]

These bits are used to set the rise/fall rate between two backlight currents as follows:

FADE_1	FADE_0	Fade Feature Rise/Fall Rate (ms/step)
0	0	32
0	1	24
1	0	16
1	1	8

The number of steps in changing the backlight current will be equal to the change in binary count of bits BL[4:0].

FADE_EN

This bit is used to enable or disable the fade feature. When the fade function is enabled and a new backlight current is set, the backlight current will change from its current value to a new value set by bits BL[4:0] at a rate of 8ms to 32ms per step. A new backlight level cannot be written during an ongoing fade operation, but an ongoing fade operation may be cancelled by resetting the fade bit. Clearing the fade bit during an ongoing fade operation changes the backlight current immediately to the value of BL[4:0]. The number of counts to complete a fade operation equals the difference between the old and new backlight values to increment or decrement the BL[4:0] bits. If the fade bit is cleared, the current level will change immediately without the fade delay. The rate of fade may be changed dynamically, even while a fade operation is active, by writing new values to the FADE_1 and FADE_0 bits. The total fade time is determined by the number of steps between old and new backlight values, multiplied by the rate of fade in ms/step. The longest elapsed time for a full scale fade-out of the backlight is nominally 1.024 seconds when the default interval of 32ms is used.

Register and Bit Definitions (continued)

BL[4:0]

These bits are used to set the current for the backlight current sinks. All enabled backlight current sinks will sink the same current, as shown in Table 1.

Table 1 — Backlight Current Control Bits

BL_4	BL_3	BL_2	BL_1	BL_0	Backlight Current (mA)
0	0	0	0	0	0.5
0	0	0	0	1	1.0
0	0	0	1	0	1.5
0	0	0	1	1	2.0
0	0	1	0	0	2.5
0	0	1	0	1	3.0
0	0	1	1	0	3.5
0	0	1	1	1	4.0
0	1	0	0	0	4.5
0	1	0	0	1	5
0	1	0	1	0	5.5
0	1	0	1	1	6
0	1	1	0	0	6.5
0	1	1	0	1	7
0	1	1	1	0	7.5
0	1	1	1	1	8
1	0	0	0	0	8.5
1	0	0	0	1	9
1	0	0	1	0	9.5
1	0	0	1	1	10
1	0	1	0	0	10.5
1	0	1	0	1	11
1	0	1	1	0	11.5
1	0	1	1	1	12
1	1	0	0	0	13
1	1	0	0	1	14
1	1	0	1	0	15
1	1	0	1	1	17
1	1	1	0	0	19
1	1	1	0	1	21
1	1	1	1	0	23
1	1	1	1	1	25

BL Enable Control Register (0x01)

This register is used to enable the backlight current sinks.

BLEN[4:1]

These bits are used to enable current sinks (active high, default low).

BLEN_4 — Enable bit for backlight BL4
BLEN_3 — Enable bit for backlight BL3
BLEN_2 — Enable bit for backlight BL2
BLEN_1 — Enable bit for backlight BL1

When enabled, the current sinks will carry the current set by the backlight current control bits BL[4:0], as shown in Table 1.

Register and Bit Definitions (continued)

LDO Control Register (0x03)

This register is used to enable the LDOs and to set their output voltages.

LDO2[2:0]

These bits are used to set the output voltage of LDO2, as shown in Table 2.

Table 2 — LDO2 Control Bits

LDO2_2	LDO2_1	LDO2_0	LDO2 Output Voltage
0	0	0	OFF
0	0	1	1.8V
0	1	0	1.7V
0	1	1	1.6V
1	0	0	1.5V
101 through 111 are not used			OFF

LDO1[3:0]

These bits set the output voltage of LDO1, as shown in Table 3.

Table 3 — LDO1 Control Bits

LDO1_3	LDO1_2	LDO1_1	LDO1_0	LDO1 Output Voltage
0	0	0	0	OFF
0	0	0	1	3.3V
0	0	1	0	3.2V
0	0	1	1	3.1V
0	1	0	0	3.0V
0	1	0	1	2.9V
0	1	1	0	2.8V
0	1	1	1	2.7V
1	0	0	0	2.6V
1	0	0	1	2.5V
1010 through 1111 are not used				OFF

SemWire Interface

Semwire Interface Functions

The SWIF pin is a write-only single wire interface. It provides the capability to address up to 32 registers to control device functionality. The protocol for using this interface is described in the following subsections.

Driving the SWIF Pin

The SWIF pin should be driven by a GPIO from the system microcontroller. The output level can be configured as either a push-pull driver (TTL or CMOS levels) or as an open drain driver with an external pull-up resistor.

Enabling the Device

The SWIF pin must be pulled from low to high for a period of greater than 1ms (t_{EN}) to enable the device into the sleep state. In the sleep state, the device bandgap is active, UVLO monitoring is active, and the serial interface is monitored for communication.

Automatic Sleep State

If the backlight current sinks are disabled, the device automatically enters the sleep state in order to minimize the current draw from the battery. When in sleep mode, the charge pump and oscillator are both disabled. The LDOs remain on if enabled.

Disabling the Device

The SWIF pin must be pulled from high to low for a period greater than 10ms (t_{DIS}) in order to shut down the device. In this state the device remains disabled until the SWIF pin is pulled high for a period greater than 1ms. All registers return to the default state.

SemWire Communication Protocol and Timing

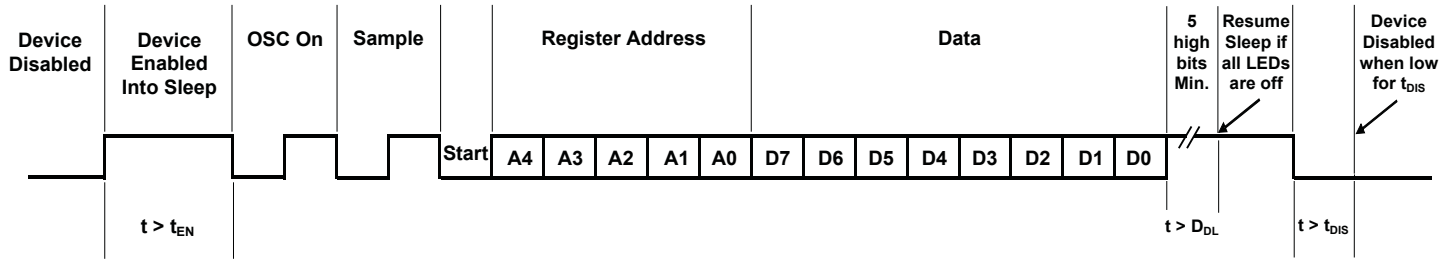
The following six step communication sequence controls all device functions when the device is enabled.

1. OSC On — The SWIF pin is toggled low for one bit duration and high for one bit duration in order to enable the oscillator. The oscillator is turned off in the sleep state to minimize quiescent current.
2. Sample — The SWIF pin is toggled low for one bit duration and high for one bit duration. During this time, the device samples the bit rate and determines the bit rate at which the register address and data values that follow will arrive. The sample rate is at least 20 times the bit rate ensuring robust communication synchronization.
3. Start — The SWIF pin is pulled low for one bit duration, which starts communication with the target register.
4. Address — The next 5 bits are the address of the target register — MSB first, LSB last.
5. Data — The next 8 bits are the data written to the target register — MSB first, LSB last.
6. Standby — After the last data bit is sent, the SWIF pin is pulled high for 5 bit durations to return the device to standby before another data write can take place. If all LEDs are disabled, the device will go back to sleep mode.

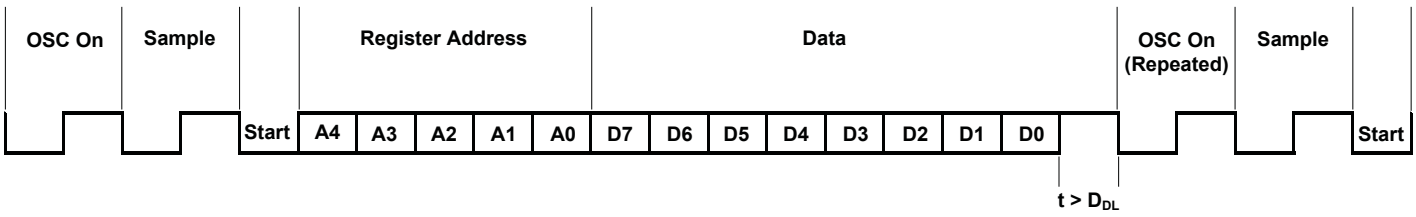
NOTE: The bit rate must be set by the host controller to a rate that is between the minimum and maximum frequencies listed in the Electrical Characteristics section.

SemWire Interface (continued)

Single Write Operation

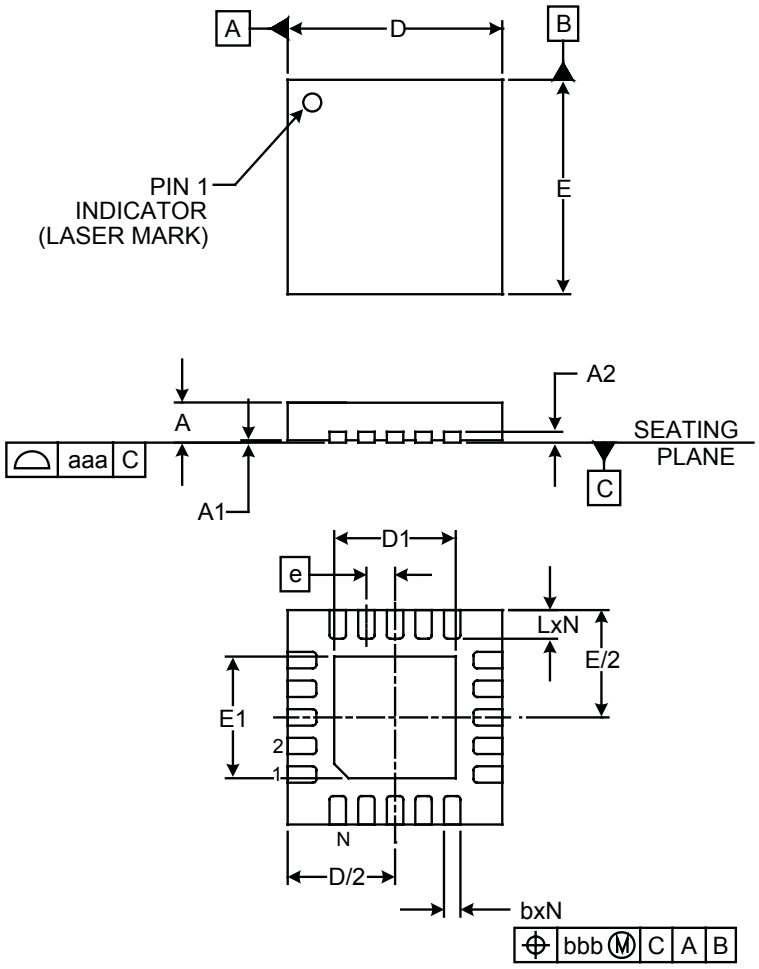


Concatenated Write Operation



To concatenate write operations, repeat Osc On, Sample and Start after the DO bit of the previous sequence as shown.

Outline Drawing — MLPQ-UT-20 3x3

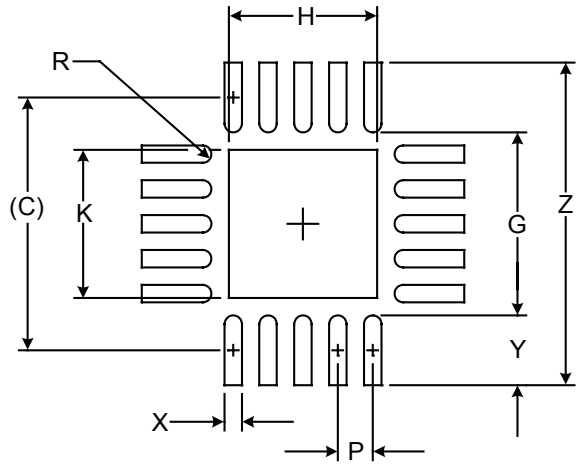


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP is 1.90 x 190mm.

Land Pattern — MLPQ-UT-20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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