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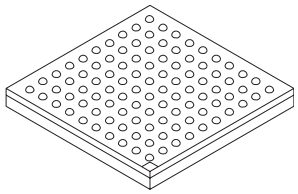
Preliminary Information

Quad Input Redundant IDCS Clock Generator

MPC9894

QUAD INPUT REDUNDANT IDCS CLOCK GENERATOR



VF SUFFIX
100-LEAD MAP BGA PACKAGE
CASE 1462

The MPC9894 is a differential input and output, PLL-based Intelligent Dynamic Clock Switch (IDCS) and clock generator specifically designed for redundant clock distribution systems. The device receives up to four LVPECL clock signals and generates eight phase-aligned output clocks. The MPC9894 is able to detect failing clock signals and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated. The device offers eight low-skew clock outputs organized into four output banks, each configurable to support the different clock frequencies. The extended temperature range of the MPC9894 supports telecommunication and networking requirements.

Features

- 8 differential LVPECL output pairs
- Quad-redundancy reference clock inputs
- IDCS-on-chip intelligent dynamic clock switch
- Smooth output phase transition during clock failover switch
- Automatically detects clock failures
- Clock activity monitor
- Clock qualifier inputs
- Manual clock select and automatic switch modes
- 21.25 — 340 MHz output frequency range
- Specified frequency and phase slew rate on clock switch
- LVCMOS compatible control inputs and outputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL bypass)
- low-skew characteristics: maximum 50 ps1 output-to-output
- I^2C interface for device configuration
- Low cycle-to-cycle and period jitter
- IEEE 1149.1 JTAG Interface
- 100-ball MAPBGA package
- Supports 2.5 V or 3.3 V supplies with 2.5 V and 3.3 V I/O
- Junction temperature range -40°C to +110°C

Functional Description

The MPC9894 is a quad differential redundant input clock generator. The device contains logic for clock failure detection and auto switching for clock redundant applications. The generator uses a fully integrated PLL to generate clock signals from any one of four redundant clock sources. The PLL multiplies the frequency of the input reference clock by one, two, four, eight or divides the reference clock by two or four. The frequency-multiplied clock signal drives four banks of two differential outputs. Each bank allows an individual frequency-divider configuration. All outputs are phase-aligned[2] to each other. Due to the external PLL feedback, the clock signals of all outputs are also phase-aligned[2] to the selected input reference clock, providing virtually zero-delay capability.

The integrated IDCS continuously monitors all four clock inputs and indicates a clock failure for each clock input. When a false clock signal is detected on the active clock, the MPC9894 switches to a redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. The MPC9894 also provides a manual mode that allows for user-controlled clock switches.

The device is packaged in a 11x11 mm^2 100-ball MAPBGA package.

1. Final specification subject to change.
2. At coincident rising edges.

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DEVICE DESCRIPTION

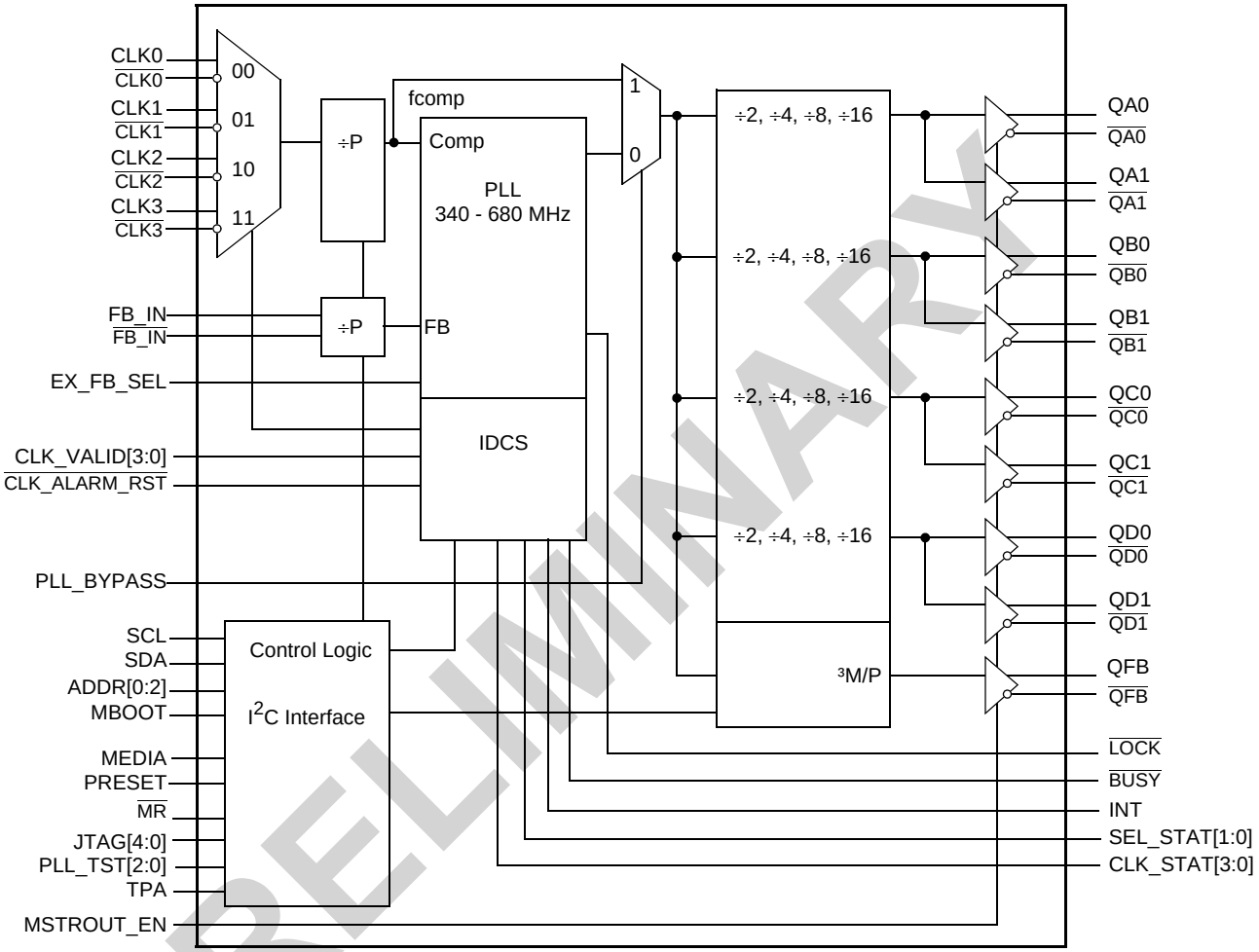


Figure 1. MPC9894 Block Diagram

Table 1. PIN CONFIGURATIONS

Pin	I/O	Type	Function	Supply	Active State
Clock Inputs and Outputs					
CLK0, $\overline{\text{CLK0}}$ CLK1,$\overline{\text{CLK1}}$ CLK2, $\overline{\text{CLK2}}$ CLK3,$\overline{\text{CLK3}}$	Input	LVPECL	PLL reference clock inputs (differential) (internal pulldown)	VDDIC	—
FB_IN, $\overline{\text{FB\_IN}}$	Input	LVPECL	PLL feedback signal input (differential). When configured for external feedback, the QFB output should be connected to FB_IN. (internal pulldown)	VDDIC	—
QA[1:0], $\overline{\text{QA[1:0]}}$	Output	LVPECL	Bank A differential outputs	VDDAB	—
QB[1:0], $\overline{\text{QB[1:0]}}$	Output	LVPECL	Bank B differential outputs	VDDAB	—
QC[1:0], $\overline{\text{QC[1:0]}}$	Output	LVPECL	Bank C differential outputs	VDDCD	—
QD[1:0], $\overline{\text{QD[1:0]}}$	Output	LVPECL	Bank D differential outputs	VDDCD	—
QFB, $\overline{\text{QFB}}$	Output	LVPECL	Differential PLL feedback output. QFB must be connected to FB_IN for correct operation	VDDCD	—
Control Inputs and Outputs					
EX_FB_SEL	Input	LVCMOS	Selects between external feedback and internal feedback	VDD	high
CLK_VALID[3:0]a	Input	LVCMOS	Validates the clock inputs CLK0 to CLK3 (internal pullup)	VDD	high

Table 1. PIN CONFIGURATIONS (Continued)

Pin	I/O	Type	Function	Supply	Active State
$\overline{\text{CLK\_ALARM\_RST}}$	Input	LVCMOS	Reset of all four alarm status flags and clock selection status flag (internal pullup)	VDD	low
PLL_BYPASS	Input	LVCMOS	Select static test mode (internal pulldown)	VDD	high
MEDIA	Input	LVCMOS	Output impedance control	VDD	high
$\overline{\text{MR}}$	Input	LVCMOS	Device reset (internal pullup)	VDD	low
$\overline{\text{LOCK}}$	Output	LVCMOS	PLL lock indicator	VDD	low
CLK_STAT[3:0]	Output	LVCMOS	Clock input status indicator	VDD	high
SEL_STAT[1:0]	Output	LVCMOS	Reference clock selection indicator	VDD	high
$\overline{\text{BUSY}}$	Output	LVCMOS	IDCS switching activity indicator	VDD	low
MBOOT	Input	LVCMOS	Activates I^2C boot sequence (internal pulldown)	VDD	high
PRESET	Input	LVCMOS	Enables Preset configuration of configuration registers on release of $\overline{\text{MR}}$ (internal pulldown)	VDD	high
$\overline{\text{INT}}$	Output	OD	Indicate any status IDCS change	VDD	low
MSTROUT_EN	Input	LVCMOS	Master Enable for all Outputs (internal pulldown)	VDD	high
SEL_2P5V	Input	LVCMOS	Device core power supply selection for VDD and VDDA	VDD	high
I^2C Interface					
SCL	I/O	OD	I^2C interface control, clock	VDD	—
SDA	I/O	OD	I^2C interface control, data	VDD	—
ADDR[2:0]	Input	LVCMOS	I^2C interface address lines (10K pullup)	VDD	high
IEEE 1149.1 and Test					
TMS	Input	LVCMOS	JTAG test mode select(10K pullup)	VDDIC	—
TDI	Input	LVCMOS	JTAG test data input(10K pullup)	VDDIC	—
TDO	Output	LVCMOS	JTAG test data output	VDDIC	—
TCK	Input	LVCMOS	JTAG test clock	VDDIC	—
$\overline{\text{TRST}}$	Input	LVCMOS	JTAG test reset(10K pullup)	VDDIC	—
PLL_TEST[2:0]	Input	LVCMOS	PLL_TEST pins (factory use only, MUST BE CONNECTED TO GND)	N/A	—
TPA	Output	LVCMOS	PLL Analog test pin (factory use only, MUST BE CONNECT TO GND)	VDDA	—
Power and Ground					
GND	Supply	Ground	Negative power supply	—	—
VDD	Supply	—	Positive power supply for the device core, output status and control inputs. (3.3 V or 2.5 V)	—	—
VDDAB	Supply	—	Supply voltage for output banks A and B (QA0 through QB1) (3.3 V or 2.5 V)	—	—
VDDCD	Supply	—	Supply voltage for output banks C and D (QC0 through QD1) and QFB (3.3 V or 2.5 V)	—	—
VDDIC	Supply	—	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN (3.3 V or 2.5 V)	—	—-
VDDA	Supply	—	Clean supply for analog portions of the PLL (This voltage is derived via a RC filter from the V_{DD} supply)	—	—

a. bit order = msb to lsb.

Table 2. FUNCTION TABLE

Control	Default	0	1
Control inputs			
PLL_BYPASS	0	PLL enabled. The input to output frequency relationship is according to Table 9 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. This is considered to be a test mode and clock monitoring and clock switching are disabled during this operation.
CLK_VALID[3:0]	0	The associated clock input is considered to be invalid and usable	The associated clock input is considered to be a valid usable clock input
$\overline{\text{CLK\_ALARM\_RST}}$	1	CLK_STAT[3:0] and SEL_STAT[1:0] flags are reset: CLK_STAT[3:0] = 0000 and SEL_STAT[1:0] = 00. $\overline{\text{CLK\_ALARM\_RST}}$ is an one-shot function.	CLK_STAT[3:0] and SEL_STAT[1:0] flags are active
MR	1	Reset of data generators and output dividers. The MPC9894 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles	Outputs enabled (active)
MBOOT	0	I^2C read/write mode	I^2C boot mode
PRESET	0	Normal Operation	Uses Configuration Register PRESET values on $\overline{\text{MR}}$
EX_FB_SEL	0	Selects internal feedback path	Selects external feedback path
MEDIA	0	low output impedance (QA0 to QD1 and QFB)	50 Ω output impedance (QA0 to QD1 and QFB)
SEL_2P5V	0	Selects 3.3 V for core V_{DD}	Selects 2.5 V for core V_{DD}
MSTROUT_EN		All outputs disabled (synchronous with clock being low)	All outputs enabled
Control outputs			
$\overline{\text{LOCK}}$[a]		PLL is locked	PLL is unlocked
$\overline{\text{BUSY}}$[a]		The IDCS has initiated a clock switch.	No clock switch currently performed
$\overline{\text{INT}}$		IDCS status has changed (indicates an assertion of CLK_STAT[3:0] or deassertion of $\overline{\text{LOCK}}$)	No status change
CLK_STAT[3:0]		Associated clock input not valid	Associated clock input valid
SEL_STAT[1:0]		Encoded value refer to Table 7	Encoded value refer to Table 7

a. The combined pins of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 are used to indicate a catastropic failure. Refer to section “PLL Out-of-Lock Conditions.”

OPERATION INFORMATION

Basic functional description

The MPC9894 is a quad-redundancy IDCS clock generator. The redundancy feature allows automatic switching from the reference clock source to a secondary clock source on detection of a failed reference clock. The MPC9894 will detect and report a missing clock on any of its four inputs. Based upon the current idcs mode setting and the qualifier input pins, the MPC9894 will switch to the next qualified secondary clock.

The input clock sources, CLK0, CLK1, CLK2, and CLK3, are assumed to be the same frequency[1] but non-phase-related sources. When a clock switch occurs, the phase alignment to the new clock source will occur over an extended time period, eliminating runt clock output pulses. The maximum rate of phase change is specified in the AC parameter Delta Period per Cycle($^{\Delta}$PER/CYC). The device uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by a variety of values, including 0.25, 0.5, 1, 2, 4 or 8. For a complete list refer to Table 9. The frequency multiplied clock signal drives four independent output banks. Each output bank is phase-aligned to the input reference clock phase, providing virtually zero-delay capability[2].

The configuration of the MPC9894 series of clock generators is performed through either the I^2C interface or by the preset configuration mode. The I^2C interface uses a 2 pin interface to transmit clock and data to and from a series of configuration and status registers in the MPC9894.

Definitions

IDCS:

Intelligent Dynamic Clock Switch. The IDCS monitors the clock inputs CLK0, CLK1, CLK2, and CLK3. Upon a failure of the reference clock signal, the IDCS switches to a qualified secondary clock signal and the status flags are set.

Reference clock signal:

The input clock signal that is selected by the IDCS or IDCS_MODE[2:0] as the input reference to the PLL.

Primary clock:

The input clock signal selected by IDCS_MODE[2:0]. The primary clock may or may not be the reference clock, depending on idcs mode and IDCS status.

Secondary clock:

The input clock signal which will be selected by the IDCS upon an automatic clock switch.

Tertiary, Quaternary clocks:

The input clock signals that will be selected by the IDCS, in turn, after the current secondary clock. This clock selection is based upon a round robin rotational sequence

Manual IDCS mode:

The reference clock input is selected by IDCS_MODE[0xx].

Automatic IDCS mode:

The reference clock signal is determined by the IDCS.

Selected clock:

The SEL_STAT[1:0] flags indicate the reference clock signal.

Qualified clock:

The corresponding CLK_VALID[3:0] signal is logic high, the associated CLK_STAT status bit is logic high and no clock failure is present.

Bit Ordering:

The bit ordering convention used in this document for both pin and register documentation is NAME[7:0] where bit 7 is the most significant bit and 0 is the least significant bit.

1. Refer to Table 39 for clock frequency specification
2. using external feedback

DEVICE CONFIGURATION

I²C Configuration and I²C Addressing

The MPC9894 is configured via a series of 8-bit registers. The bits in these registers allow a wide range of control over the operation of the MPC9894 clock generator. These registers are accessed via an I²C interface through which a 7-bit address is sent from the I²C master to select the specific I²C slave device being accessed. The address for this clock driver is found in the first of the MPC9894 I2C registers. The format of this address has a fixed most-significant four bits of binary 1101 while the least-significant 3 address bits are read from the 3 ADDR pins. This provides the capability to configure up to 8 clock devices on a single I²C interface.

In addition, activation of the MBOOT pin on power-up or reset initiates a automatic boot sequence allowing the clock generators to be initialized from a I²C compatible EEPROM. In this case the MPC9894 becomes an I²C master and the configuration bits are filled by the information from the first 6 bytes of the EEPROM. This allows the clock to be configured without a controlling I²C bus master if desired. The PRESET pin allows the device to be configured without a I²C bus master.

The detailed register descriptions are found in the section, I²C Interface and configuration/status register.

IDCS MODE Configuration

Three register bits are used to configure the MPC9894 in either an automatic clock switch mode or into a manual clock select mode. The three mode select bits are defined in Table 3.

IDCS modes 000 through 011 allow manual selection between the four clock sources. IDCS modes 100 through 111 enable the automatic mode of the IDCS.

Table 3. MPC9894 IDCS Configuration

IDCS_MODE [2:0]	Description	Primary Clock	Secondary Clock[a]	Tertiary Clock	Quaternary Clock
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

a. For CLK_VALID[3:0] = 1111 and input clock validity

Automatic IDCS Mode

In the automatic mode, the clock failure detection is enabled and the IDCS overwrites the selected clock on a clock failure. The IDCS operation requires PLL_BYPASS = 0 and IDCS_MODE[2] = 1. The reference clock is handled in a round robin method based upon clock validity and the qualification input CLK_VALID[3:0]: The qualification input is obtained from the four input pins, CLK_VALID[3:0]. If any of the CLK_VALID pins are low the associated clock input will be considered “unqualified” and thus not selected as a reference clock. Alternatively, if a clock input does not have a valid clock signal, it will not be selected and the next qualified and valid clock is selected as the reference clock.

For example, if IDCS_MODE[2:0] = 100 (the IDCS is in automatic mode), CLK_VALID[3:0] = 1111 and CLK0, CLK1, CLK2, and CLK3 have valid input clock signals then CLK0 is the primary clock and CLK1 is the secondary clock. The IDCS selects the primary clock as the reference clock and the PLL will phase-lock the clock outputs to the CLK0 input. Upon the failure of CLK0 the IDCS will select CLK1 as the reference clock and initiate a switch, making CLK1 the reference clock and CLK2 the secondary clock. If CLK1 fails, the IDCS will switch to CLK2, etc.

A de-asserted CLK_VALID[] pin disables the associated clock input as secondary clock. The associated clock input cannot be selected by the IDCS as secondary clock signal. For instance, if CLK0 is the primary clock and CLK_VALID[3:0] = 1101, the IDCS will select CLK2 upon a clock failure of CLK0 (CLK1 is disabled by the CLK_VALID1 input, allowing external logic to control the IDCS switch logic). If a clock is the reference clock signal and its associated CLK_VALID signal is switched from ‘valid' to ‘invalid', the IDCS initiates a clock input switch, selecting the next available clock input (secondary clock).

An invalid clock[1] signal triggers the associated clock status output (CLK_STAT[3:0]), independent of the primary and reference clock. These pins go set on a clock failure and remain set (sticky) until the $\overline{\text{CLK\_ALARM\_RST}}$ pin or the individual alarm reset bits (ALARM_RST[3:0]) are asserted. The CLK_STAT[3:0] outputs are mirrored in the device register 4 for I²C bus access.

After each successful IDCS-commanded switch, the primary clock as set by IDCS_MODE[1xx] is no longer the reference clock. The user may reset the IDCS flags by asserting the individual ALARM_RST[3:0] bits after each IDCS-commanded switch. Activation of ALARM_RST[3:0] does not change the reference clock. A user-commanded change of the primary clock in automatic mode requires a write command to the IDCS_MODE[2:0] = 0xx bits (the primary clock and SEL_STAT[1:0] can be freely changed by setting IDCS_MODE[2:0] = 1xx). If the reference clock is not the primary clock, a write command to IDCS_MODE[2:0] = 1xx will cause the PLL to lock on the primary clock, given the new primary clock is a qualified clock.

1. See “Clock failure detection” on page 9 .

Table 4. Input Clock Qualifier and Status Flag

Input Clock	Associated Input Qualifier[a]	Associated Input Clock Status Flag	
		Pin	Register location
CLK0	CLK_VALID0	CLK_STAT0	Device register 5, bit 3
CLK1	CLK_VALID1	CLK_STAT1	Device register 5, bit 4
CLK2	CLK_VALID2	CLK_STAT2	Device register 5, bit 5
CLK3	CLK_VALID3	CLK_STAT3	Device register 5, bit 6

a. The input qualifier logic can be enabled or disabled by setting the QUAL_EN bit in register 3.

Table 5. Input Clock Status CLK_STAT[3:0]

CLK_STAT[]	Description
0	Clock input failure
1	Clock input signal valid

Table 6. Clock Input Qualifier CLK_VALID[3:0]

CLK_VALID[]	Associated Input Clock
0	Not qualified and will not be selected
1	Qualified

The SEL_STAT[1:0] pins indicate which of the four input clocks is the current reference clock. In the automatic mode and In the case of the reference clock failure, the SEL_STAT flag will indicate a reference clock different from the original primary clock selected by IDCS_MODE[2:0]. The CLK_STAT outputs are mirrored in register 5, bits 1:0 for I^2C bus access.

Table 7. SEL_STAT[1:0]

SEL_STAT[1:0]	Selected clock input
00	CLK0
01	CLK1
10	CLK2
11	CLK3

If all four clock inputs are not qualified the VCO will slew to its lowest frequency. This condition will be indicated by the $\overline{LOCK}$ pin being de-asserted. The MPC9894 will remain in this state until an input clock is restored and the device is reset via the $\overline{MR}$ pin.

Clock Failure Detection

The MPC9894 clock failure dectection is performed using an input clock amplitude check combined with an activity detector. The following conditions will trigger a failed clock status (CLK_STATn = 0) on any qualified clock (CLK_VALIDn = 1). These conditions are:

1. Either or both CLKx, $\overline{CLKx}$ are disconnected from the input clock source and open.
2. CLKx and $\overline{CLKx}$ are shorted together
3. Either or both CLKx or $\overline{CLKx}$ are shorted to GND
4. Both CLKx and $\overline{CLKx}$ are shorted to a power supply
5. Amplitude of CLKx or $\overline{CLKx}$ is less than $V_{PP, OK}$ (refer to AC specification, Table 39)

In addition, the currently selected clock is checked by a phase-frequency detector after the input divider (P). This is triggered by a phase step of mae($\varnothing$). This phase detector will issue a failed clock status (CLK_STATn = 0) within 'P' clock cycles.

The IDCS does not detect changes of the reference frequency or the reference frequency being out of the specified input frequency range. This includes errors such as reference frequency drift due to crystal aging etc.

Clearing of IDCS Alarm Flags

The input clock status flags are set by a clock failure and remain set until manually cleared (sticky). Clearing can be done by either of two methods. All status flags can be cleared by the package pin, $\overline{CLK\_ALARM\_RST}$. Or individual status flags can be cleared via register bits, ALARM_RST[3:0]. The $\overline{CLK\_ALARM\_RST}$ pin is activated by a negative edge on the pin. This clears all CLK_STAT[3:0] flags and returns the IDCS to the primary clock source. The SEL_STAT[1:0]-selected clock indicator now reflects the IDCS_MODE[2:0] setting.

By using ALARM_RST[3:0] (register 2) individual CLK_STAT[3:0] bits are cleared by writing a logic 0 to the individual bit in this register. It is important to note that this action does not return the IDCS to the primary clock.

IDCS Manual Mode

The manual request IDCS mode is selected by IDCS_MODE[2:0] = 0xx. The PLL functions normally and all four inputs clocks are monitored. The reference clock will always be the clock signal selected by IDCS_MODE[1:0] and will be indicated by SEL_STAT[1:0]. A manual-requested clock switch (by changing the IDCS_MODE[0xx] signal) will only be executed if the new clock is valid. The SEL_STAT[1:0] pins/bits should be checked after the manual request to ensure the clock switch occurred.

Interrupt Operation

The MPC9894 pin, $\overline{\text{INT}}$, may be used to interrupt a microprocessor or microcontroller. This open drain output pin goes active or low on any of the following occurrences

1. A clock failure as indicated by any of bits 6 thru 3 being set in the status register
2. A out-of-lock condition for the PLL as indicated by either the $\overline{\text{LOCK}}$ pin or bit 2 of the status register.

The interrupted processor would then use the I^2C interface to read the status register (bit 7) to determine if this MPC9894 generated the interrupt. If the interrupt was caused by this MC9894, the status register would then be analyzed to determine the reason for the interrupt and then the appropriate action taken.

In order for interrupts to occur, the INT_E bit must be set in the Device Configuration and Output Clock Enable Register. Once the interrupt flag has been set, reading of the Status Register clears the INT flag.

Clock Operation on Power-Up

On or after power-up, the MPC9894 must be reset via the $\overline{\text{MR}}$ pin. The MPC9894 may be powered-up in either of three configurations. These configurations are selected by the PRESET pin and MBOOT pin.

If PRESET is low, on release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a benign mode with all clock outputs disabled. The device is ready to be and must be programmed via the I^2C interface prior to operation.

If the PRESET pin is high on the release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a run state. In this case the IDCS is configured for automatic mode, CLK0 to be the primary clock, a divide by 2 on clock bank A and B outputs, a divide by 8 on clock C and D outputs, all clock output banks enabled and interrupts enabled. If using the preset mode, then at least one of the clock inputs must have the correct input frequency prior to $\overline{\text{MR}}$ going high.

Later in this document, tables defining the I^2C interface registers describe both configurations. The default (reset) information is for the normal reset operation, while the default (preset) information describes the values for each configuration bit on activation of the PRESET pin. In order to return the MPC9894 to either the preset or reset configuration the $\overline{\text{MR}}$ pin must be activated.

Refer to the Boot Mode section for a description of the MBOOT pin.

PLL Feedback

The MPC9894 may be operated with either an internal or an external PLL feedback path. The selection of internal vs. external feedback is made with the pin, EX_FB_SEL. If external feedback is desired, the EX_FB_SEL pin should be connected to VDD and a connection from QFB/$\overline{\text{QFB}}$ to FB_IN/$\overline{\text{FB\_IN}}$ must be made. External feedback provides a known relationship between the clock input and the feedback input for phase synchronization of output clock signals to the clock input. If this phase synchronization is not required, the MPC9894 may be configured for internal feedback by the connection of EX_FB_SEL to ground. In this configuration, the connection from the feedback output to the feedback input is not required. The feedback output may be used as a separate output to produce a reference clock output.

PLL Out-of-Lock Conditions

The $\overline{\text{LOCK}}$ pin and associated status bit indicates the lock state of the PLL. After power-up and prior to writing configuration data to the control registers, an out-of-lock condition will be indicated by $\overline{\text{LOCK}}$ = 1. If a valid clock is available and proper configuration data is written to the control registers, $\overline{\text{LOCK}}$ will then indicate the PLL is in a locked condition with $\overline{\text{LOCK}}$ = 0.

The combination of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 is used to indicate a catastrophic failure of the PLL. This condition will occur on the following:

1. All input clocks have failed or no clock is present.
2. External feedback has been selected with the EX_FB_SEL pin and an external feedback signal is not present on the FB_IN/$\overline{\text{FB\_IN}}$ inputs. It should be noted that if this condition occurs during the initial PLL lock acquisition the PLL will produce a clock that is locked to the internal feedback path. However, the catastrophic failure status of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 will occur.

Recovery from the catastrophic failure condition requires repairing the cause of the failure, followed by a master reset to be issued to the MPC9894.

CLOCK OUTPUT TRANSITION

A MPC9894 clock switch, either in IDCS manual or IDCS automatic mode, follows the next positive edge of the newly selected reference clock signal. The positive edge of the feedback clock and the newly selected reference clock edge will start to slew to alignment by adjusting the feedback edge placement a small amount of time in each clock cycle. Figure 2 “Clock Switch” shows a failed primary input clock with the MPC9894 switching to and aligning to the secondary clock. This small amount of additional time in each clock cycle will ensure that the output clock does not have any large phase changes or frequency changes in a short period of time. The alignment will be to either 1) the closest edge, either forward or backward or 2) toward the lagging clock edge. The maximum rate of period change is specified in the AC parameter tables with the parameter of $^{\Delta}$PER/CYC. This parameter implies that the output clock edge will never change more than the specified amount in any one cycle.

The busy signal is used to indicate that the MPC9894 is in the process of slewing to the new input clock alignment. The signal is accessed thru the $\overline{\text{BUSY}}$ pin and goes set upon a clock switch. The pin is reset once the phase realignment is completed. During the period that $\overline{\text{BUSY}}$ is active, the configuration register of the MPC9894 should not be written with new configuration data.

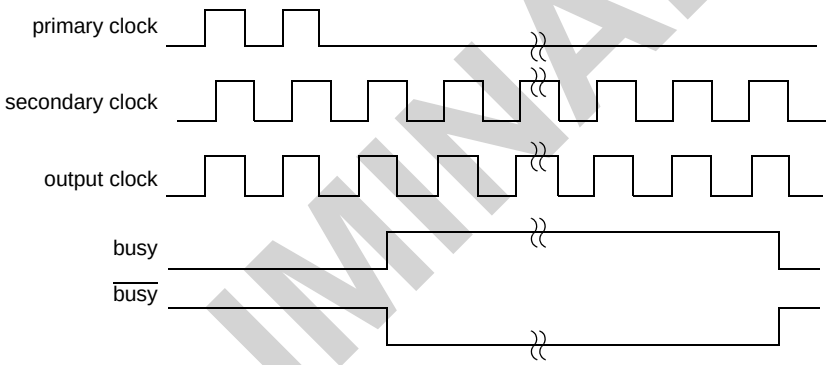


Figure 2. Clock Switch

For example, if the current input clock of 62.5 MHz and the secondary clock are 180 degrees out of phase then the minimum clock transiition time can be calculated by

$$t_{cycle} = 1 \div f_{cycle} = 1 \div 62.5\ MHz = 16\ ns$$

Therefore 180 degree clock difference is

$$t_{cycle} \div 2 = 8\ ns$$

Assuming a $^{\Delta}$PER/CYC of 40 ps, then

$$8ns \div 40\ ps/cycle = 200\ cycles.$$

This is the minimum number of cycles that will be required for the alignment to the new clock. The alignment to the new clock phase may occur slower than this but never faster.

The alignment on clock failure is selectable between either 1) the closest edge, either forward or backward or 2) toward the lagging clock edge. The selection of the alignment method is selected in the Slew_Control bit (bit 5) of the Device Configuration and Output Enable Register. This selection allows the user to select the alignment method that best suits the application. The characteristics and subsquent advantages and disadvantages of each method are described as follows.

1. Slew to closest edge
   a. The alignment is either forward toward the lagging edge or backward toward the leading edge.
   b. The alignment to the closest edge ensures re-alignment to the new clock input in the minimum time.
   c. In applications where the input clocks are closely aligned, there is no ambiguity on the direction of clock slew.
   d. The clock output frequency will either increase or decrease based on direction of clock slew.
2. Slew to lagging edge
   a. The output frequency always decreases. Thus the clock frequency never violates a maximum frequency specification in the user system.
   b. when input clocks are closely aligned (within SPO + jitter) the MPC9894 may align to the closest edge or to the lagging edge. In the case of multiple MPC9894s with equivelent clock inputs one MPC9894 may align in one direction while an other MPC9894 may align to the opposite direction.

If default values for the Slew_Control is not the configuration desired then the reconfiguration of the slew method should be perform soon after power-up and the configuration should remain fixed from that point.

INPUT AND OUTPUT FREQUENCY CONFIGURATION

Configuring the MPC9894 input and output frequencies requires programming the internal PLL input, feedback and output dividers. The output frequency is represented by the following formula:

$$f_{OUT} = [(f_{REF} \div P) \cdot M] \div N$$

where f_{REF} is the reference frequency of the selected input clock source (reference input), M is the PLL feedback divider and N is a output divider. The PLL input divider P, the feedback divider M and the output divider are configured by the device registers 1 and 4. The MPC9894 has four output banks (Bank A, B, C, and D) and each output bank can be configured individually as shown in Table Table 8.

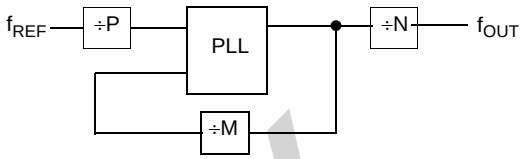


Figure 3. PLL Frequency Calculation

Table 8. Configuration of PLL P, M and N Frequency Dividers

Divider	Available Values	Configuration Through
PLL Input Divider (P)	÷1, ÷32, ÷3, ÷4, ÷5, ÷6	Input_FB_Div[3:0], Register 4, bit 3:0
PLL Feedback Divider (M)	÷8, ÷12, ÷16	
PLL Output Divider, Bank A (N_A)	÷2, ÷4, ÷8, ÷16	FSEL_B[1:0], Register 1, bit 7:6
PLL Output Divider, Bank B (N_B)	÷2, ÷4, ÷8, ÷16	FSEL_B[1:0], Register 1, bit 5:4
PLL Output Divider, Bank C (N_C)	÷2, ÷4, ÷8, ÷16	FSEL_C[1:0], Register 1, bit 3:2
PLL Output Divider, Bank D (N_D)	÷2, ÷4, ÷8, ÷16	FSEL_D[1:0], Register 1, bit 1:0

The reference frequency f_{REF} and the selection of the PLL input divider (P) and feedback-divider (M) is limited by the specified VCO frequency range. f_{REF}, P and M must be configured to match the VCO frequency range of 340 to 680 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \div P \cdot M) \le f_{VCO,MAX}$$

The PLL input divider (P) can be used to situate the VCO in the specified frequency range. The PLL input divider effectively extends the usable input frequency range.

The output frequency for each bank can be derived from the VCO frequency and output divider (N):

$$f_{QA}[1:0] = f_{VCO} \div N_A$$
$$f_{QB}[1:0] = f_{VCO} \div N_B$$
$$f_{QC}[1:0] = f_{VCO} \div N_C$$
$$f_{QD}[1:0] = f_{VCO} \div N_D$$

Table 9 illustrates the possible input clock frequency configurations of the MPC9894. Note that the VCO lock range is always 340 MHz to 680 MHz, setting lower and upper boundaries for the frequency range of the device.

Table 9. Input and output frequency ranges

Input_FB_Div[3:0]	P	M	f_{ref} range MHz	Output frequency for any bank A, B, C or D (FSEL_x) and ratio to fref			
				N = 2	N = 4	N = 8	N = 16
0	÷1	÷16	21.25 - 42.5	$8 \cdot f_{ref}$	$4 \cdot f_{ref}$	$2 \cdot f_{ref}$	f_{ref}
1	÷1	÷12	28.33 -56.67	$6 \cdot f_{ref}f$	$3 \cdot f_{ref}$	$1.5 \cdot f_{ref}$	$0.75 \cdot f_{ref}$
2	÷2	÷12	56.66 -113.34	$3 \cdot f_{ref}f$	$1.5 \cdot f_{ref}$	$0.75 \cdot f_{ref}$	$0.375 \cdot f_{ref}$
3	÷1	÷8	42.5 - 85.0	$4 \cdot f_{ref}f$	$2 \cdot f_{ref}$	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$
4	÷2	÷16	42.5 - 85.0	$4 \cdot f_{ref}$	$2 \cdot f_{ref}$	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$
5	reserved						
6	÷2	÷8	85.0 - 170.0	$2 \cdot f_{ref}$	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$	$0.125 \cdot f_{ref}$
7	÷3	÷12	85.0 - 170.0	$2 \cdot f_{ref}$	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$	$0.125 \cdot f_{ref}$
8	÷4	÷16	85.0 - 170.0	$2 \cdot f_{ref}$	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$	$0.125 \cdot f_{ref}$
9	reserved						
10	÷4	÷12	113.32 - 226.64	$1.5 \cdot f_{ref}$	$0.75 \cdot f_{ref}$	$0.375 \cdot f_{ref}$	$0.1875 \cdot f_{ref}$
11	reserved						
12	reserved						
13	reserved						
14	4	÷8	170.0 - 340.0	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$	$0.25 \cdot f_{ref}$	$0.125 \cdot f_{ref}$
15	6	÷12	170.0 - 340.0	$1 \cdot f_{ref}$	$0.5 \cdot f_{ref}$	$0.25 \cdot f_{ref}$	$0.125 \cdot f_{ref}$

I²C INTERFACE AND CONFIGURATION/STATUS REGISTERS

The following tables summarize the bit configurations for the registers accessible via the I²C interface. The register values are read or written over the I²C interface by the I²C Master. This sequence starts with the I²C start command, followed by the I²C device address and read/write byte. This is then followed by the address of the register that is to be accessed. In the case of a write, the register address byte is followed by the data to be written to that register. In the case of a read, the device will then respond with the data from that register. At the conclusion of the transfer an I²CStop command is issued by the Master to terminate the transfer. For a complete description of the I²Cprotocol refer to the v2.1 I²C specification.

Table 10 lists the registers that are accessible via the I²C interface.

Table 10. I²C Registers

Address	Register
0x00	Table 11 “Slave Address (Register 0 — Read Only)”
0x01	Table 12 “Output Configuration Register (Register 1 — Read/Write)”
0x02	Table 14 “Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)”
0x03	Table 17 “Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)”
0x04	Table 22 “Input and Feedback Divider Configuration Register (Register 4 — Read/Write)”
0x05	Table 24 “Status Register (Register 5 — Read Only)”
0x06	Table 25 “Output Power-Up Register (Register 6 — Read/Write)”
0x07	Table 27 “Feedback Power-Up Register (Register 7 — Read/Write)”

Boot Mode

When the I²C boot mode is activated on power-up or reset via the MBOOT pin, the entire set of writable configuration registers are written with a 6-byte sequence. This sequence starts with the Output Configuration Register, and is followed by the Mode Configuration and Alarm Reset Register, the Device Configuration and Output Clock Enable Register, the Input and Feedback Divider Configuration Register, the Output Power-Up Register and the Feedback Power-Up Register. This equates to the register sequence of 1, 2, 3, 4, 6, 7. This sequence starts with the start command, the device select and read/write(write) byte, followed by the beginning byte address for reading from the EEPROM. This is then followed by the start command, device select and read/write (read) and four current address read bytes. The device address is the binary 7-bit value of 1010000. This I²C sequence is compatible with industry standard I²C bus EEPROMs such as STMicroelectronics M24C01, or equivalent.

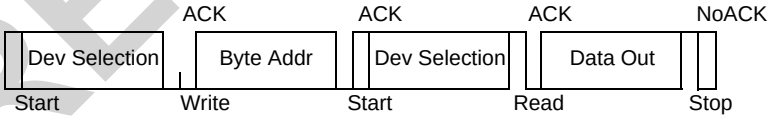


Figure 4. Boot mode random access read

Slave Address Register

The Slave Address register contains the I²C address that is used to determine if the data on the I²C interface is addressed to this device. The seven-bit address is determined with the fixed value of binary 1101 followed by variable bits that are obtained from the three address pins. The three input pins allow for 8 different addresses for a given clock generator, allowing up to 8 clock generators to be addressed on a single I²C interface.

Table 11. Slave Address (Register 0 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADD_R5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		1	1	0	1			
Preset default		1	1	0	1			

Output Configuration Register

The output configuration register is divided into four, 2 bit-groups with each group selecting the divide ratio for output banks A through bank D, refer to Table 12. For each bank, four output divider settings (÷2, ÷4, ÷8, ÷16) are available, refer to Table 12.

Table 12. Output Configuration Register (Register 1 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

Table 13. PLL Output Divider N (FSEL_A to FSEL_D)

FSEL_x[1:0]	Value
00	÷2
01	÷4
10	÷8
11	÷16

Mode Configuration Register

The mode configuration register, refer to Table 14, is a read/write register and contains the fields for mode selection as well as alarm reset.

The mode of the MPC9894 may be changed by writing the three least significant Mode Configuration Register bits to the desired value. The current idcs mode of the MPC9894 may be obtained by reading this register.

The alarm reset bits, found in bit positions 6 thru 3, may be used to individually reset the status flags of register 5. Each of these flag bits are associated with the four clock inputs pins and indicate a failed clock input. Clearing of a clock status flag is performed by writing a logic 1 to the individual bit (or bits if more than one flag is to be cleared). Care should be taken to insure that the idcs mode information is written to the proper value when resetting the clock status bits. The four alarm reset bits always read as a logic 0. If a clock input status flag is cleared and the clock input is still in a failed state, the status flag will go set within 4 clock cycles after being cleared.

Table 14. Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (Refer to Table 15)				IDCS_MODE[2:0] (Refer to Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 15. Individual reset of CLK_STAT[x] bits

ALARM_RST[x]	Description
0	no action
1	The status flag CLK_STAT[x] is cleared by setting of this bit. (bit always reads as zero)

Table 16. MPC9894 IDCS configuration[a]

IDCS_MODE [2:0]	Description	Primary clock	Secondary clock[b]	Tertiary clock[b]	Quaternary clock[b]
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

a. This is a repeat of table 3.

b. For CLK_VALID[3:0] = 1111 and input clock validity.

Device Configuration and Output Enable Register

The Device Configuration and Output Enable Register is used to individually enable or disable each bank of outputs. Output banks are enabled by setting the corresponding bit to a logic 1 and disabled by setting the bit to a logic 0 as described in Table 21 “Output Clock Stop/Enable”. The disable logic sets the outputs of the addressed bank synchronously to logic low state (Qx[] = 0 and Qx[] = 1). The clock output enable/stop bits can be set asynchronous to any clock signal without the risk of generating of runt pulses. The PLL feedback output QFB cannot be disabled when MPC9894 is configured for external feedback.

The Device Configuration Register, bit 6, QUAL_EN is used to enable or disable all clock input qualifier pins. Asserting this bit enables the Clock Qualifier Input Pins CLK_VALID[3:0]. Deasserting this bit disables these pins such that inputs on CLK_VALID[3:0] are ignored.

The INT_E bit, in bit position7, is used to enable or disable interrupts from occurring on the INT pin. The setting of the interrupt flag (bit 7 of the Status Register) is unaffected by this bit.

Table 17. Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

Table 18. Interrupt Signal ($\overline{\text{INT}}$) Enable INT_E

INT_E	Description
0	Interrupt signal $\overline{\text{INT}}$ is disabled
1	Interrupt signal $\overline{\text{INT}}$ is enabled

Table 19. Input Clock Qualifier Enable QUAL_EN

QUAL_EN	Description
0	CLK_VALID[3:0] are disabled (clock qualifier signals are disabled)
1	CLK_VALID[3:0] are enabled (clocks can be qualified)

Table 20. Slew Control

Slew_Control	Description
0	Clock slew direction on clock switch is toward the closest edge
1	Clock slew direction on clock switch is toward the lagging edge

Table 21. Output Clock Stop/Enable

ENABLE_Qx	Description
0	Output bank x is disabled (clock stop in logic low state)
1	Output bank x is enabled

Input and Feedback Divider Configuration Register

Table 22. Input and Feedback Divider Configuration Register (Register 4 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

The Input and Feedback Divider Configuration Register is used to select the input divider value and the feedback divider values. The four bits for Input_FB_Div allow 16 combinations of input and feedback divider ratios. Some input and output frequency ranges may overlap allowing a choice of PLL closed loop bandwidths. This selection may be useful when PLL devices are cascaded.

Table 23. Input_FB_Div[3:0]

Input_FB_Div[3:0]	Input Divider (P)	Feedback Divider (M)
0000	1	16
0001	1	12
0010	2	12
0011	1	8
0100	2	16
0101	reserved	
0110	2	8
0111	3	12
1000	4	16
1001	reserved	
1010	4	12
1011	reserved	
1100	reserved	
1101	reserved	
1110	4	8
1111	6	12

Device Status Register

The Device Status Register contains a copy of the status SEL_STAT[1:0], $\overline{\text{LOCK}}$ and CLK_STAT[3:0] pins. In addition, bit 7 is an INT flag bit, which is used to indicate a setting of a bit in the CLK_STAT[3:0], a clearing of the $\overline{\text{LOCK}}$ bit and a change in the value of the SEL_STAT[1:0] bits.

The CLK_STAT[3:0] bits are sticky and remain set until manually reset through the Mode Configuration Register.

The setting of the register INT bit is reflected on the interrupt pin only if interrupts are enabled. Enabling interrupts is done by the setting of the INT_E bit which is located in the Device Configuration Register. Reading of the Status Register clears the INT flag.

Table 24. Status Register (Register 5 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of $\overline{\text{INT}}$ signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				$\overline{\text{LOCK}}$ Inverse of $\overline{\text{LOCK}}$ signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

Output Power-Up Register

The Output Power-Up Register configures each of the 8 LVPECL outputs for either power-up or a power-down state. The use of these bits allows power consumption to be reduced when all of the clock outputs are not used. Placing an output in the power-down condition is not synchronous with the clock edges.

Table 25. Output Power-Up Register (Register 6 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB01	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

Table 26. Clock Output Power-Up Bits

PWR_Qxx	Description
0	Output Power-Down
1	Output Power-Up

Feedback Power-Up Register

The Feedback Power-Up register bit 0 is used to configure the MPC9894 feedback output in either a power-up state or a power-down state. Note this register bit is valid for internal feedback configuration only. When external feedback is selected QFB is always enabled and in a power-up state. The remaining bits of this register are unused and read as a logic 0.

Table 27. Feedback Power-Up Register (Register 7 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

Table 28. Feedback Output Power-Up Bit

PWR_QFB	Description
0	Feedback Output Power-Down
1	Feedback Output Power-Up

IEEE Std.1149.1(JTAG)

This section describes the IEEE Std. 1149.1 compliant Test Access Port (TAP) and Boundary Scan Architecture implementation in the MPC9894. Special private instructions are provided to assist in production test control. These instructions combined with control of the test mode inputs and the use of shared inputs and outputs provide for full production test mode access and control.

Test Access Port Interface Signals

Table 29 lists the TAP interface signals and their descriptions.

Table 29. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test Clock	Test logic clock.	Input	-
TMS	Test Mode Select	TAP mode control input.	Input	-
TDI	Test Data In	Serial test instruction/data input.	Input	-
TRST_B	Test Reset Bar	Asynchronous test controller reset.	Input	-
TDO	Test Data Out	Serial test instruction/data output.	Output	-

Instruction Register

Table 30. Instruction Register

Bit Position	4	3	2	1	0
Field	IR				
Capture-IR Value	0	0	0	0	1

Instructions

Table 31 lists the public instructions provided in the implementation and their instruction codes. Public instructions are accessible by the customer for board test and may also be used for production chip test.

Table 31. TAP Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	11111	Bypass Register
CLAMP	01100	Bypass Register
EXTEST	00000	Boundary Scan Register
HIGHZ	01001	Bypass Register
IDCODE	00001	ID Register
SAMPLE	00010	Boundary Scan Register

Boundary-Scan Register

A full description of the boundary scan register may be found in the BSDL file.

Device Identification Register (0x0281D01D)

Table 32. Device Idenitfication Register

Bit Position	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	version				part number																manufacturer ID											
Value	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1

POWER SUPPLY CONFIGURATION

The MPC9894 operates from either a 3.3 V or 2.5 V voltage supply for the device core. The pin SEL_2P5V is used to logically indicate the core supply voltage. This selection is done by setting the pin to a logic 1 for 2.5 V or logic 0 for 3.3 V operation.

The input and output supply voltage may be set for either 3.3 V or 2.5 V and can be individually set for inputs and banks of outputs. Table 33 “Power Supply Configuration” lists the supply pins and what pin or group of pins are associated with each supply. Note, that for output skew and SPO specifications to be valid the input, feedback input and output, and the output bank must all be at the same voltage level.

Table 33. Power Supply Configuration

Supply voltage	Description	Value
V_{DD}	Positive power supply for the device core, output status and control inputs. (3.3 V or 2.5 V)	3.3 V or 2.5 V
V_{DDAB}	Supply voltage for output banks A and B (QA0 through QB1)	3.3 V or 2.5 V
V_{DDCD}	Supply voltage for output banks A and B (QC0 through QD1) and QFB	3.3 V or 2.5 V
V_{DDIC}[a]	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN	3.3 V or 2.5 V
V_{DDA}	Clean supply for Analog portions of the PLL (This voltage is derived via an RC filter from the V_{DD} supply)	derived from V_{DD}

a. VDDIC (Supply of FB_IN) must be equal to VDDCD (Supply of QFB) to ensure the SPO specification is met.

Power Supply Sequencing and $\overline{MR}$ operation

Figure 5 defines the release time and the minumum pulse length for $\overline{MR}$ pin. The $\overline{MR}$ release time is based upon the power supply being stable and within V_{DD} specifications. Refer to Table 39 for actual parameter values. The MPC9894 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

V_{DD} must ramp up prior to or concurrent with the other power supply pins. It is recommended that the maximum slew rate for the V_{DD} supply not exceed 0.5 V/ms.

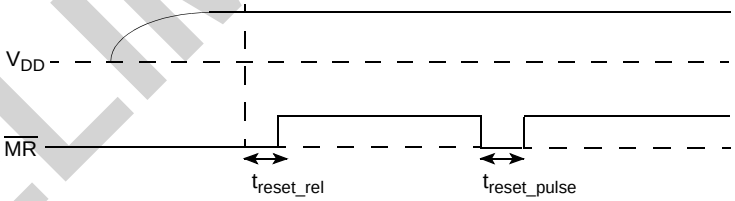


Figure 5. MR operation

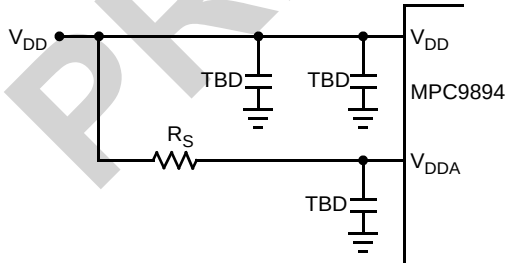


Figure 6. V_{CC} Power Supply Bypass

Power Supply Bypassing

The MPC9894 is a mixed analog/digital product. The differential architecture of the MPC9894 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth

Clock Outputs

The MPC9894 clock outputs are differential LVPECL voltage compatible. The outputs are designed to drive a single 50 Ω impedance load that is properly terminated. The media pin is used to select between either of two output termination techniques.

Selection of media = 0 sets all of the outputs to drive up to 50 ohm parallel terminated (to Vtt) transmission lines. With media = 1 the outputs are designed to drive 50 Ω transmission line terminated with a single 100 differential load resistor. See figures 7 and 8 for diagrams of each of these termination techniques. Note, that the traditional output pulldown resistors for emitter follower biasing are not required for the MPC9894. If external feedback is used, the QFB output must be terminated with the same technique as selected with the media pin. Once a termination technique is chosen, that technique must be used for all MPC9894 outputs to guarantee output skew timing.

The recommended termination technique is media = 1. This provides a simpler termination method and also reduces overall power consumption of the MPC9894. Unused outputs may be powered-down via the Output Power-Up and Feedback Power-Up registers to conserve power. If external feedback is selected the programming of the PWR_QFB bit is ignored.

Table 34. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	-0.3	4.0	V	
$V_{DDAB, CD}$	Supply Voltage (differential outputs)	-0.3	4.0	V	
V_{DDIC}	Supply Voltage (differential inputs)	-0.3	4.0	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	-0.3	V_{DD}	V	
V_{IN}	DC Input Voltage[b]	-0.3	V_{DDx}+0.3	V	
V_{OUT}	DC Output Voltage[c]	-0.3	V_{DDx}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

b. V_{DDx} references power supply pin associated with specific input pin.

c. V_{DDx} references power supply pin associated with specific output pin.

Table 35. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage (LVPECL)		V_{DD} - 2		V	LVPECL outputs
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	500			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		TBD		pF	Inputs
θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T_J	Junction Temperature[a]	-40		110	°C	

a. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (Refer to Application Note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9894 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9894 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 36. DC CHARACTERISTICS (T_J = -40°C to +110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V_{DD} = 2.5 V±5% and $V_{DDAB,CD}$ = 2.5 V±5%						
I_{DD}	Maximum Quiescent Supply Current (core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}$[b]	Maximum Quiescent Supply Current, outputs terminated 50 Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDA} pin
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins
Supply Current for V_{DD} = 3.3 V±5% and $V_{DDAB,CD}$ = 3.3 V±5% or $V_{DDAB,CD}$ = 2.5 V±5%						
I_{DD}	Maximum Quiescent Supply Current (core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}$[c]	Maximum Quiescent Supply Current, outputs terminated 50 Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDIN} pins
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins

a. DC characteristics are design targets and pending characterization.

b. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).

c. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).

Table 37. PECL DC CHARACTERISTICS (T_J = -40°C to +110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL clock inputs (CLKx, $\overline{CLKx}$ and FB_IN, $\overline{FB\_IN}$)b for V_{DDIC} = 3.3 V ±5% or V_{DDIC} = 2.5 V ±5%						
V_{PKPK}	AC Differential Input Voltage[c]	0.2		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[d]	1.25		V_{DD}-0.3	V	Differential operation
I_{IN}	Input Current[a]			±100	mA	V_{PP} = 0.8 V and $V_{CMR} = V_{DDL}$-0.7 V
Differential PECL clock outputs (QA0 to QD1 and QFB) for $V_{DDAB,CD}$ = 3.3 V ±5% or $V_{DDAB,CD}$ = 2.5 V ±5%						
V_{OH}	Output High Voltage	TBD	$V_{DDAB,CD}$-1.0	TBD	V	Termination 50 Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	$V_{DDAB,CD}$-1.7	TBD	V	Termination 50 Ω to V_{TT}
Z_{OUT}	Output Impedance MEDIA = 0 MEDIA = 1		TBD 50		Ω Ω	see Figure 7 see Figure 8

a. DC characteristics are design targets and pending characterization.

b. Clock inputs driven by PECL compatible signals.

c. V_{PKPK} is the minimum differential input voltage swing required to maintain AC characteristics.

d. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 38. LVCMOS I/O DC CHARACTERISTICS (T_J = -40°C to +110°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Single-ended LVCMOS inputs for V_{DD} = 3.3 V ±5%						
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -6 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 6 mA
Z_{OUT}	Output Impedance	40		62	Ω	
I_{IN}	Input Currentb			10	µA	$V_{IN} = V_{DDL}$ or GND
Single-ended LVCMOS inputs for V_{DD} = 2.5 V±5%						
V_{IH}	Input High Voltage	1.7		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.9			V	I_{OH} = -6 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 6 mA
Z_{OUT}	Output Impedance	45		70	Ω	
I_{IN}	Input Currentb			10	µA	$V_{IN} = V_{DDL}$ or GND

a. DC characteristics are design targets and pending characterization.

b. Inputs have pull-down resistors affecting the input current.

Table 39. AC CHARACTERISTICS (T_J = -40°C to +110°C)[a b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{DD} = 3.3 V ±5%, $V_{DDAB,CD,IC}$ = 3.3 V ±5% or $V_{DDAB,CD,IC}$ = 2.5 V ±5%							
Input and output timing specification							
f_{ref}	Input reference frequency		21.25		42.5	MHz	Input_FB_Div[3:0] = 0
			28.33		56.67	MHz	Input_FB_Div[3:0] = 1
			56.66		113.34	MHz	Input_FB_Div[3:0] = 2
			42.5		85	MHz	Input_FB_Div[3:0] = 3,4
			85.0		170	MHz	Input_FB_Div[3:0] = 6,7,8
			113.32		226.68	MHz	Input_FB_Div[3:0] = 10
			170		340	MHz	Input_FB_Div[3:0] = 14,15
	Input reference frequency in PLL bypass modec				TBD	MHz	PLL bypass
f_{VCO}	VCO frequency ranged		340		680	MHz	
f_{MAX}	Output Frequency	÷2 output	170.0		340.0	MHz	PLL locked
		÷4 output	85.0		170.0	MHz	
		÷8 output	42.5		85.0	MHz	
		÷16 output	21.25		42.5	MHz	
f_{refDC}	Reference Input Duty Cycle		40		60	%	
f_{refacc}	Input Frequency Accuracye				500	ppm	
$mae_{(\varnothing)}$	Misaligned Edge Specification		±600		±1600	ps	
t_r, t_f	Output Rise/Fall Time				800	ps	20% to 80%
DC	Output duty cycle		47.5	50	52.5	%	
f_{I2C}	I^2C frequency range				100	kHz	
Differential input and output voltages							
V_{PP}	Differential input voltagef (peak-to-peak) (PECL)				1.3	V	
$V_{PP, OK}$	Differential input voltageg (peak-to-peak) (PECL)		TBD			V	
$V_{PP, NOK}$	Differential input voltageh (peak-to-peak) (PECL)				TBD	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) (PECL)		TBD	0.8		V	
PLL and IDCS specifications							
$t_{(\varnothing)}$	Propagation Delay (static phase offset) CLKX, $\overline{CLKX}$ to FB_IN, $\overline{FB\_IN}$		-100		+100	ps	PLL locked with external feedback selected
$t_{sk(O)}$	Output-to-output Skew within a banki				50	ps	
	Output-to-output Skew across a banki				TBD		
$^{\Delta}$PER/CYC	Rate of change of periodj	÷2 output			+40	ps	slew_control = 1
		÷4 output			+80		
		÷8 output			+120		
		÷16 output			+160		
$^{\Delta}$PER/CYC	Rate of change of periodk	÷2 output			±40	ps	slew_control = 0
		÷4 output			±80		
		÷8 output			±120		
		÷16 output			±160		
Jitter and bandwidth specifications							
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1 σ)			10	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1 σ)		TBD		ps	
$t_{JIT(ý)}$	I/O Phase Jitter	RMS (1 σ)		TBD		ps	
BW	PLL closed loop bandwidthl			TBD		kHz	

Table 39. AC CHARACTERISTICS (T_J = -40°C to +110°C)[a b] (Continued)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{DD} = 3.3 V ±5%, $V_{DDAB,CD,IC}$ = 3.3 V ±5% or $V_{DDAB,CD,IC}$ = 2.5 V ±5%						
$\overline{MR}$ and PLL Lock						
t_{LOCK}	Maximum PLL Lock Time			10	µs	
t_{reset_ref}	$\overline{MR}$ hold time on power up	2			ps	
t_{reset_pulse}	$\overline{MR}$ hold time	100			ns	

a. AC characteristics are design targets and pending characterization.

b. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.

c. In bypass mode, the MPC9894 divides the input reference clock.

d. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.

e. All Input Clock frequencies must be within this value to guarantee smooth phase transition on input clock switch.

f. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.

g. $V_{PP, OK}$ is the minimum differential input voltage swing required for a valid clock signal. Above $V_{PP, OK}$ the input will be detected as a good clock (see IDCS).

h. $V_{PP, NOK}$ is the maximum differential input voltage swing for a guaranteed bad clock. Below $V_{PP, NOK}$ the input will be detected as a failed clock (see IDCS).

i. $V_{DDAB} = V_{DDCD}$.

j. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.

k. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.

l. -3 dB point of PLL transfer characteristics.

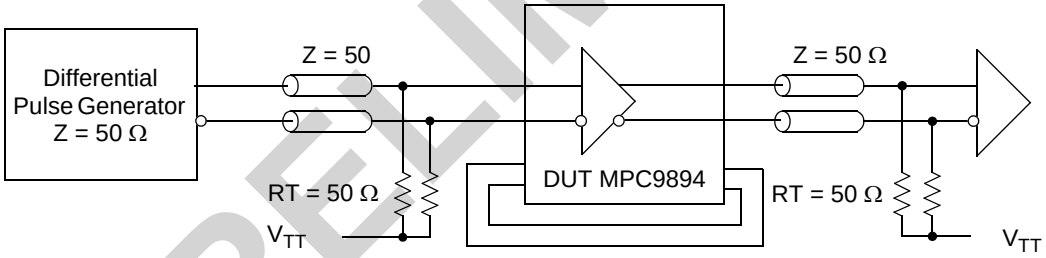


Figure 7. MPC9894 AC test reference (Media = 0)

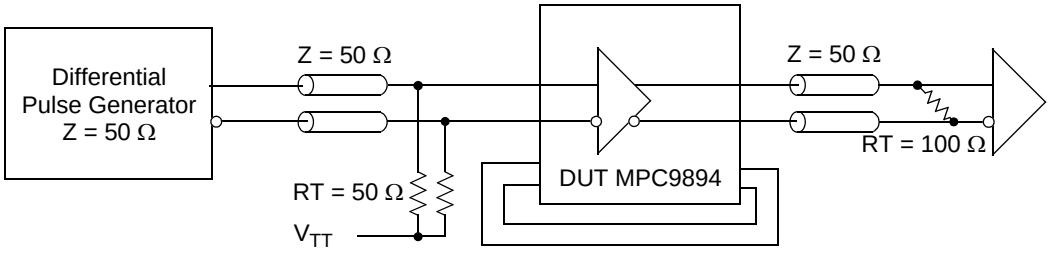


Figure 8. MPC9894 AC test reference (Media = 1)

MPC9894 Pin and Package

Table 40. MPC9894 Pin Listing

Signal Name	Description	Direction	Type	Active State	Supply	Pin
CLK0	Clock0 Positive Input	Input	LVPECL	-	VDDIC	D1
$\overline{\text{CLK0}}$	Clock0 Negative Input	Input	LVPECL	-	VDDIC	D2
CLK1	Clock1 Positive Input	Input	LVPECL	-	VDDIC	E3
$\overline{\text{CLK1}}$	Clock1 Negative Input	Input	LVPECL	-	VDDIC	E2
CLK2	Clock2 Positive Input	Input	LVPECL	-	VDDIC	F3
$\overline{\text{CLK2}}$	Clock2 Negative Input	Input	LVPECL	-	VDDIC	F2
CLK3	Clock3 Positive Input	Input	LVPECL	-	VDDIC	G1
$\overline{\text{CLK3}}$	Clock3 Negative Input	Input	LVPECL	-	VDDIC	G2
FB_IN	Feedback Clock Positive Input	Input	LVPECL	-	VDDIC	C1
$\overline{\text{FB\_IN}}$	Feedback Clock Negative Input	Input	LVPECL	-	VDDIC	C2
QA0	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K4
$\overline{\text{QA0}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J4
QA1	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K5
$\overline{\text{QA1}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J5
QB0	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K7
$\overline{\text{QB0}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J7
QB1	Positive Differential Clock Output	Output	LVPECL	-	VDDAB	K6
$\overline{\text{QB1}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDAB	J6
QC0	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A7
$\overline{\text{QC0}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B7
QC1	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A6
$\overline{\text{QC1}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B6
QD0	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A4
$\overline{\text{QD0}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B4
QD1	Positive Differential Clock Output	Output	LVPECL	-	VDDCD	A5
$\overline{\text{QD1}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B5
QFB	Postive Differential Clock Output	Output	LVPECL	-	VDDCD	A3
$\overline{\text{QFB}}$	Negative Differential Clock Output	Output	LVPECL	-	VDDCD	B3
CLK_VALID3	Qualifier for clock input CLK3	Input	LVCMOS	High	VDD	F10
CLK_VALID2	Qualifier for clock input CLK2	Input	LVCMOS	High	VDD	E10
CLK_VALID1	Qualifier for clock input CLK1	Input	LVCMOS	High	VDD	E9
CLK_VALID0	Qualifier for clock input CLK0	Input	LVCMOS	High	VDD	E8
$\overline{\text{CLK\_ALARM\_RST}}$	Reset of all four alarm status flags and clock selection status flag	Input	LVCMOS	Low	VDD	F8
PLL_BYPASS	Select PLL of static test mode	Input	LVCMOS	High	VDD	F9
MEDIA	Output impedance control (high = 50 Ω)	Input	LVCMOS	High	VDD	E7
SCL	I^2C Interface Control, Clock	I/O	LVCMOS	-	VDD	C9

Table 40. MPC9894 Pin Listing (Continued)

Signal Name	Description	Direction	Type	Active State	Supply	Pin
SDA	I^2C Interface Control, Data	I/O	LVCMOS	-	VDD	C10
ADDR2	I^2C Interface Control, Address 2 (MSB)	Input	LVCMOS	-	VDD	A9
ADDR1	I^2C Interface Control, Address 1	Input	LVCMOS	-	VDD	B8
ADDR0	I^2C Interface Control, Address 1 (LSB)	Input	LVCMOS	-	VDD	A8
$\overline{MR}$	Device Master Reset	Input	LVCMOS	Low	VDD	D10
$\overline{LOCK}$	PLL Lock Indicator	Output	LVCMOS	Low	VDD	G10
CLK_STAT3	Input CLK3 status indicator	Output	LVCMOS	High	VDD	H9
CLK_STAT2	Input CLK2 status indicator	Output	LVCMOS	High	VDD	H10
CLK_STAT1	Input CLK1 status indicator	Output	LVCMOS	High	VDD	G8
CLK_STAT0	Input CLK0 status indicator	Output	LVCMOS	High	VDD	G9
SEL_STAT1	Reference Clock Selection Indicator (MSB)	Output	LVCMOS	High	VDD	K8
SEL_STAT0	Reference Clock Selection Indicator (LSB)	Output	LVCMOS	High	VDD	J8
$\overline{BUSY}$	IDCS switch activity indicator	Output	LVCMOS	High	VDD	J10
MBOOT	Activates I^2C Boot Sequence	Input	LVCMOS	High	VDD	D8
$\overline{INT}$	Indicates any status IDCS change	Output	OD	n/a	VDD	D9
PRESET	Sets preset state	Input	LVCMOS	High	VDD	H7
TMS	JTAG Test Mode Select	Input	LVCMOS	High	VDDIC	D3
TDI	JTAG Test Data Input	Input	LVCMOS	-	VDDIC	H1
$\overline{TRST}$	JTAG Test Reset Bar	Input	LVCMOS	Low	VDD	H2
TCK	JTAG Test Clock	Input	LVCMOS	-	VDDIC	G3
TDO	JTAG Test Data Out	Output	LVCMOS	-	VDDIC	J3
SEL_2P5V	Indicate core VDD level, (high = 2.5V, low = 3.3V)	Input	LVCMOS	-	VDD	D7
MSTROUT_EN	Enable all outputs in sync	Input	LVCMOS	High	VDD	K9
PLL_TEST2	PLL Test Bit 2	Input	LVCMOS	-	VDDAB	H4
PLL_TEST1	PLL Test Bit 1	Input	LVCMOS	-	VDDAB	G5
PLL_TEST0	PLL Test Bit 0 (LSB)	Input	LVCMOS	-	VDDCD	D5
TPA	PLL Analog Test Pin	Output	Analog	-	VDDA	E4
EX_FB_SEL	Select feedback mode (high = external)	Input	LVCMOS	-	VDD	C7
VDD	Control Input, Status Output and Core Supply	Power	-	-	VDD	A10, B9, C3, C8, G7, H8, J9, K10
VDDA	Analog Supply	Power	-	-	VDDA	E1
VDDAB	Supply for A and B bank outputs	Power	-	-	VDDAB	H6, J2, K2
VDDCD	Supply for C and D bank outputs	Power	-	-	VDDCD	A1, C4, C6
VDDIC	Supply for input clocks	Power	-	-	VDDIC	B2, H3, K1
GND	Control Input, Status Output and Core Ground	Ground	-	-	GND	A2, B1, B10, C5, D4, D6, E5, E6, F1, F4, F5, F6, F7, G4, G6, H5, J1, K3

Table 41. MPC9894 PIN DIAGRAM

	1	2	3	4	5	6	7	8	9	10
A	VDDC	GND	QFB	QD0	QD1	QC1	QC0	ADDR0	ADDR2	VDD
B	GND	VDDIC	$\overline{\text{QFB}}$	$\overline{\text{QD0}}$	$\overline{\text{QD1}}$	$\overline{\text{QC1}}$	$\overline{\text{QC0}}$	ADDR1	VDD	GND
C	FB_IN	$\overline{\text{FB\_IN}}$	VDD	VDDCD	GND	VDDCD	EX_FB _SEL	VDD	SCL	SDA
D	CLK0	$\overline{\text{CLK0}}$	TMS	GND	PLL_TES T0	GND	SEL_ 2P5V	MBOOT	$\overline{\text{INT}}$	$\overline{\text{MR}}$
E	VDDA	$\overline{\text{CLK1}}$	CLK1	TPA	GND	GND	MEDIA	CLK_ VALID0	CLK_ VALID1	CLK_ VALID2
F	GND	$\overline{\text{CLK2}}$	CLK2	GND	GND	GND	GND	$\overline{\text{CLK\_}}$ ALARM_ $\overline{\text{RST}}$	PLL_ BYPASS	CLK_ VALID3
G	CLK3	$\overline{\text{CLK3}}$	TCK	GND	PLL_TES T1	GND	VDD	CLK_ STAT1	CLK_ STAT0	$\overline{\text{LOCK}}$
H	TDI	$\overline{\text{TRST}}$	VDDIC	PLL_TES T2	GND	VDDAB	PRESET	VDD	CLK_ STAT3	CLK_ STAT2
J	GND	VDDAB	TDO	$\overline{\text{QA0}}$	$\overline{\text{QA1}}$	$\overline{\text{QB1}}$	$\overline{\text{QB0}}$	SEL_STA T0	VDD	$\overline{\text{BUSY}}$
K	VDDIC	VDDAB	GND	QA0	QA1	QB1	QB0	SEL_ STAT1	MSTROU T_EN	VDD

MPC9894 PROGRAMMING MODEL

Table 42. Slave Address (Register 0 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADD_R5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			
Preset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			

Table 43. Output Configuration Register (Register 1 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

Table 44. Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (See Table 15)				IDCS_MODE[2:0] (See Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 45. Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

Table 46. Input and Feedback Divider Configuration Register (Register 4 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

Table 47. Status Register (Register 5 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of $\overline{\text{INT}}$ signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				LOCK Inverse of $\overline{\text{LOCK}}$ signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

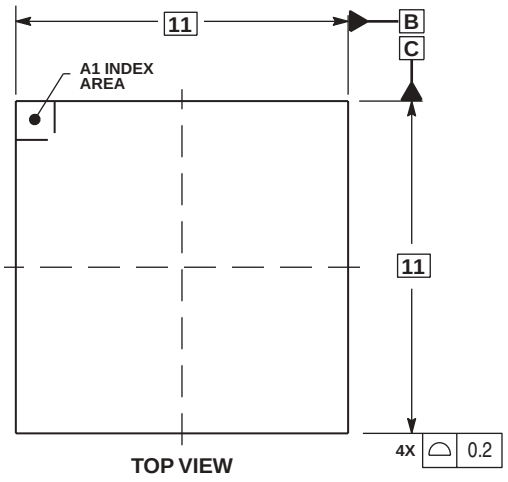
Table 48. Output Power-Up Register (Register 6 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB01	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

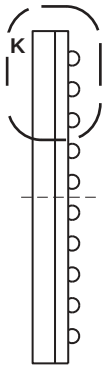
Table 49. Feedback Power-Up Register (Register 7 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

OUTLINE DIMENSIONS

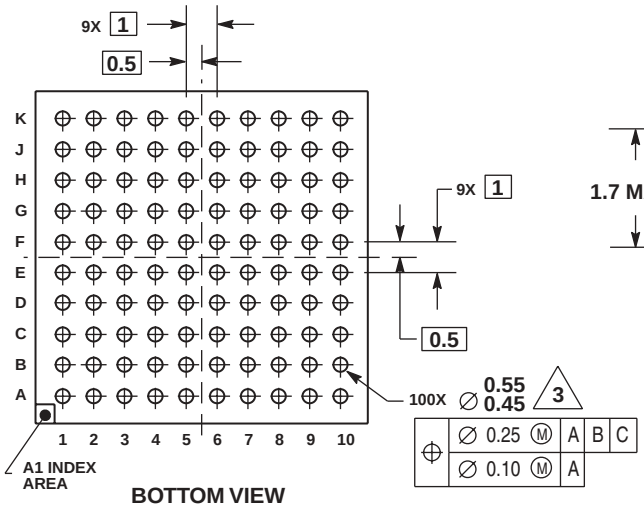


TOP VIEW

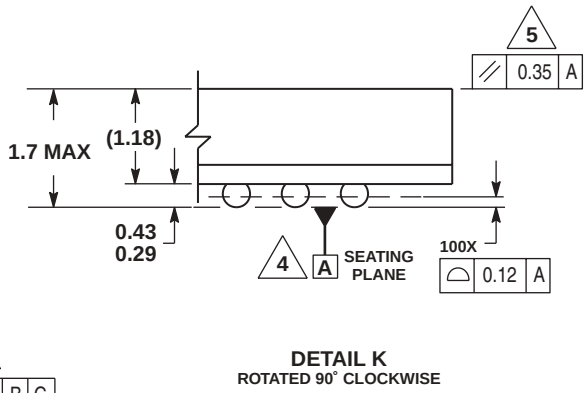


SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGING.



BOTTOM VIEW



DETAIL K
ROTATED 90° CLOCKWISE

VF SUFFIX
100-LEAD MAP BGA PACKAGE
CASE 1462-01
ISSUE O

NOTES

NOTES

NOTES

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