

## System Clock Chip for ATI RS400 P4™-based Systems

### Recommended Application:

ATI RS400 systems using Intel P4™ processors

### Output Features:

- 6 - Pairs of SRC/PCI-Express clocks
- 2 - Pairs of ATIG (SRC/PCI Express\*) clocks
- 3 - Pairs of Intel P4 clocks
- 3 - 14.318 MHz REF clocks
- 1 - 48MHz USB clock
- 1 - 33 MHz PCI clock seed

### Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 300ppm frequency accuracy on CPU & SRC clocks

### Features/Benefits:

- 2- Programmable Clock Request pins for SRC clocks
- Supports CK410 or CK409 frequency table mapping
- Spread Spectrum for EMI reduction
- Outputs may be disabled via SMBus
- External crystal load capacitors for maximum frequency accuracy

### Functionality - (CK410# = 0)

FS_C <sup>1</sup>	FS_B <sup>1</sup>	FS_A <sup>1</sup>	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz
0	0	0	266.66	100.00	33.33	14.318	48.000
		1	133.33	100.00	33.33	14.318	48.000
	1	0	200.00	100.00	33.33	14.318	48.000
		1	166.66	100.00	33.33	14.318	48.000
1	0	0	333.33	100.00	33.33	14.318	48.000
		1	100.00	100.00	33.33	14.318	48.000
	1	0	400.00	100.00	33.33	14.318	48.000
		1	RESERVED			14.318	48.000

### Functionality - (CK410# = 1)

FS_C <sup>1</sup> Byte6 bit5	FS_B <sup>1</sup>	FS_A <sup>1</sup>	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz
0	0	0	100.00	100.00	33.33	14.318	48.000
		1	200.00	100.00	33.33	14.318	48.000
	1	0	133.33	100.00	33.33	14.318	48.000
		1	166.67	100.00	33.33	14.318	48.000
1	0	0	200.00	100.00	33.33	14.318	48.000
		1	400.00	100.00	33.33	14.318	48.000
	1	0	266.67	100.00	33.33	14.318	48.000
		1	333.33	100.00	33.33	14.318	48.000

1. FS\_C, FS\_B and FS\_A are low-threshold inputs. Please see the V<sub>IL,FS</sub> and V<sub>IH,FS</sub> specifications in the Input/Supply/Common Output Parameters Table for correct values.

### Pin Configuration

X1	1	56	VDDREF
X2	2	55	GND
VDD48	3	54	**FS_A/REF0
USB_48MHz	4	53	**FS_B/REF1
GND	5	52	**TEST_SEL/REF2
VTT_PWRGD#/PD	6	51	VDDPCI
SCLK	7	50	**CK410#/PCICLK0
SDATA	8	49	GNDPCI
**FS_C	9	48	*CPU_STOP#
**CLKREQA#	10	47	CPUCLKT0
**CLKREQB#	11	46	CPUCLKC0
SRCCLKT7	12	45	VDDCPU
SRCCLKC7	13	44	GNDCPU
VDDSRC	14	43	CPUCLKT1
GNDSRC	15	42	CPUCLKC1
SRCCLKT6	16	41	CPUCLKT2_ITP
SRCCLKC6	17	40	CPUCLKC2_ITP
SRCCLKT5	18	39	VDDA
SRCCLKC5	19	38	GND A
GNDSRC	20	37	IREF
VDDSRC	21	36	GNDSRC
SRCCLKT4	22	35	VDDSRC
SRCCLKC4	23	34	SRCCLKT0
SRCCLKT3	24	33	SRCCLKC0
SRCCLKC3	25	32	VDDATI
GNDSRC	26	31	GNDATI
ATIGCLKT1	27	30	ATIGCLKT0
ATIGCLKC1	28	29	ATIGCLKC0

ICS951411

**Note:** Pins preceded by \*\*\* have a 120 Kohm Internal Pull Down resistor  
Pins preceded by \*\* have a 120 Kohm Internal Pull Up resistor

**56-pin SSOP & TSSOP**

### Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	X1	IN	Crystal input, Nominally 14.318MHz.
2	X2	OUT	Crystal output, Nominally 14.318MHz
3	VDD48	PWR	Power pin for the 48MHz output.3.3V
4	USB_48MHz	OUT	48.00MHz USB clock
5	GND	PWR	Ground pin.
6	VTT_PWRGD#/PD	IN	Vtt_PwrGd# is an active low input used to determine when latched inputs are ready to be sampled. PD is an asynchronous active high input pin used to put the device into a low power state. The internal clocks, PLLs and the crystal oscillator are stopped.
7	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
8	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
9	**FS_C	IN	Frequency select latch input pin
10	**CLKREQA#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
11	**CLKREQB#	IN	Output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = enabled, 1 = tri-stated
12	SRCCLKT7	OUT	True clock of differential SRC clock pair.
13	SRCCLKC7	OUT	Complement clock of differential SRC clock pair.
14	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
15	GNDSRC	PWR	Ground pin for the SRC outputs
16	SRCCLKT6	OUT	True clock of differential SRC clock pair.
17	SRCCLKC6	OUT	Complement clock of differential SRC clock pair.
18	SRCCLKT5	OUT	True clock of differential SRC clock pair.
19	SRCCLKC5	OUT	Complement clock of differential SRC clock pair.
20	GNDSRC	PWR	Ground pin for the SRC outputs
21	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
22	SRCCLKT4	OUT	True clock of differential SRC clock pair.
23	SRCCLKC4	OUT	Complement clock of differential SRC clock pair.
24	SRCCLKT3	OUT	True clock of differential SRC clock pair.
25	SRCCLKC3	OUT	Complement clock of differential SRC clock pair.
26	GNDSRC	PWR	Ground pin for the SRC outputs
27	ATIGCLKT1	OUT	True clock of differential SRC clock pair.
28	ATIGCLKC1	OUT	Complementary clock of differential SRC clock pair.

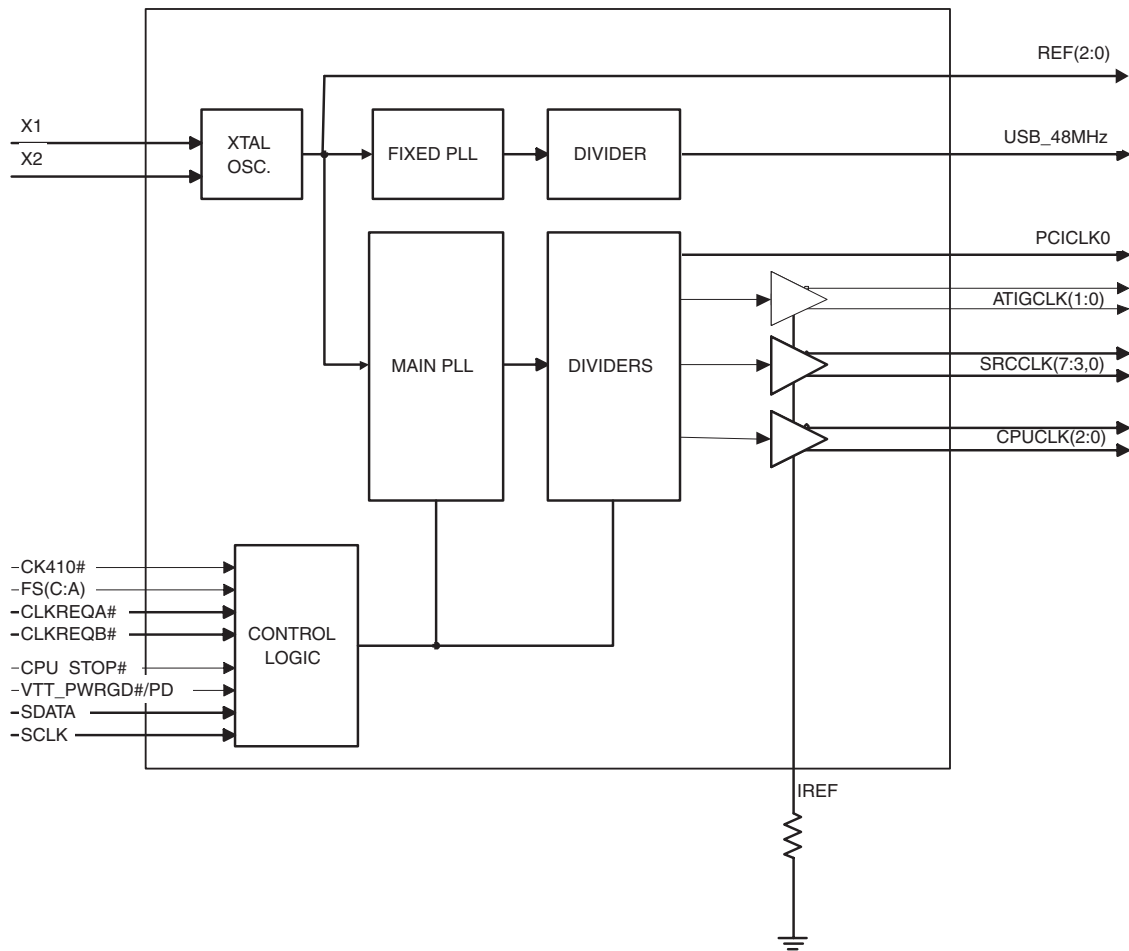
**Pin Description (Continued)**

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
29	ATIGCLKC0	OUT	Complementary clock of differential SRC clock pair.
30	ATIGCLKT0	OUT	True clock of differential SRC clock pair.
31	GNDATI	PWR	Ground for ATI Gclocks, nominal 3.3V
32	VDDATI	PWR	Power supply ATI Gclocks, nominal 3.3V
33	SRCCLKC0	OUT	Complement clock of differential SRC clock pair.
34	SRCCLKT0	OUT	True clock of differential SRC clock pair.
35	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
36	GNDSRC	PWR	Ground pin for the SRC outputs
37	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
38	GNDPLL	PWR	Ground pin for the PLL core.
39	VDDPLL	PWR	3.3V power for the PLL core.
40	CPUCLKC2_ITP	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
41	CPUCLKT2_ITP	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	CPUCLKC1	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	CPUCLKT1	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
44	GNDCPU	PWR	Ground pin for the CPU outputs
45	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
46	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
47	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
48	*CPU_STOP#	IN	Stops all CPUCLK, except those set to be free running clocks
49	GNDPCI	PWR	Ground pin for the PCI outputs
50	**CK410#/PCICLK0	I/O	FS Table select latch input pin / 3.3V PCI clock output. 0 = CK410 FS Table, 1 = CK409 FS Table
51	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
52	**TEST_SEL/REF2	I/O	TEST_SEL: latched input to select TEST MODE / 14.318 MHz reference clock. 1 = All outputs are CK410 REF/N test mode 0 = All outputs behave normally.
53	**FS_B/REF1	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
54	**FS_A/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
55	GNDREF	PWR	Ground pin.
56	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V

**General Description**

ICS951411 provides a single-chip clocking solution for the ATI RS400-based systems using the latest Intel P4 processors. ICS951411 is driven with a 14.318MHz crystal. It generates CPU outputs up to 400MHz and also provides highly accurate SRC clocks for PCI Express support. Two Clock Request pins are provided for Express-Card™ support.

**Block Diagram**



**Power Groups**

Pin Number		Description
VDD	GND	
56	55	Xtal, REF
51	49	PCICLK output
45	44	CPUCLK Outputs
14, 21, 35	15, 20, 26, 36	SRCCLK outputs
32	31	ATIGCLK outputs
39	38	Analog, CPU PLL
3	5	USB_48MHz output

## General SMBus serial interface information for the ICS951411

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2 <sub>(H)</sub>		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N		X Byte
	○	
	○	
	○	
	○	
Byte N + X - 1		
		ACK
P	stoP bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2 <sub>(H)</sub>			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3 <sub>(H)</sub>			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
ACK		X Byte	
			Beginning Byte N
	○		
	○		
	○		
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		

Table1: CPU Frequency Selection Table

Bit 4 CPU FS4 (CK410#)	Bit 3 CPU FS3 (SS_EN)	Bit2 FSC	Bit1 FSB	Bit0 FSA	CPU (MHz)	PCI33 (MHz)	Spread %	
0	0	0	0	0	266.6667	33.3333	No Spread	C K 4 1 0
0	0	0	0	1	133.3333	33.3333		
0	0	0	1	0	200.0000	33.3333		
0	0	0	1	1	166.6668	33.3334		
0	0	1	0	0	333.3335	33.3334		
0	0	1	0	1	100.0000	33.3333		
0	0	1	1	0	400.0000	33.3333		
0	0	1	1	1	Reserved			
0	1	0	0	0	266.6667	33.3333	-0.5%	C K 4 1 0
0	1	0	0	1	133.3333	33.3333		
0	1	0	1	0	200.0000	33.3333		
0	1	0	1	1	166.6668	33.3334		
0	1	1	0	0	333.3335	33.3334		
0	1	1	0	1	100.0000	33.3333		
0	1	1	1	0	400.0000	33.3333		
0	1	1	1	1	Reserved			
1	0	0	0	0	100.0000	33.3333	No Spread	C K 4 0 9
1	0	0	0	1	133.3333	33.3333		
1	0	0	1	0	200.0000	33.3333		
1	0	0	1	1	166.6668	33.3334		
1	0	1	0	0	200.0000	33.3333		
1	0	1	0	1	266.6667	33.3333		
1	0	1	1	0	400.0000	33.3333		
1	0	1	1	1	333.3335	33.3334		
1	1	0	0	0	100.0000	33.3333	-0.5%	C K 4 0 9
1	1	0	0	1	133.3333	33.3333		
1	1	0	1	0	200.0000	33.3333		
1	1	0	1	1	166.6668	33.3334		
1	1	1	0	0	200.0000	33.3333		
1	1	1	0	1	266.6667	33.3333		
1	1	1	1	0	400.0000	33.3333		
1	1	1	1	1	333.3335	33.3334		

Table2: SRC & ATIG Frequency Selection Table

SRC FS4 (SS_EN)	SRC FS3	Bit2 FS2	Bit1 FS1	Bit0 FS0	SRC(7:3,0), ATIG(1:0) (MHz)	Spread %	SRC OverClock
0	0	0	0	0	100.00	0	1.00
0	0	0	0	1	100.00	0	1.00
0	0	0	1	0	100.00	0	1.00
0	0	0	1	1	100.00	0	1.00
0	0	1	0	0	101.00	0	1.01
0	0	1	0	1	101.00	0	1.01
0	0	1	1	0	101.00	0	1.01
0	0	1	1	1	101.00	0	1.01
0	1	0	0	0	102.00	0	1.02
0	1	0	0	1	102.00	0	1.02
0	1	0	1	0	102.00	0	1.02
0	1	0	1	1	102.00	0	1.02
0	1	1	0	0	104.00	0	1.04
0	1	1	0	1	104.00	0	1.04
0	1	1	1	0	104.00	0	1.04
0	1	1	1	1	104.00	0	1.04
1	0	0	0	0	100.00	-0.5%	1.00
1	0	0	0	1	100.00	-0.5%	1.00
1	0	0	1	0	100.00	-0.5%	1.00
1	0	0	1	1	100.00	-0.5%	1.00
1	0	1	0	0	101.00	-0.5%	1.01
1	0	1	0	1	101.00	-0.5%	1.01
1	0	1	1	0	101.00	-0.5%	1.01
1	0	1	1	1	101.00	-0.5%	1.01
1	1	0	0	0	102.00	-0.5%	1.02
1	1	0	0	1	102.00	-0.5%	1.02
1	1	0	1	0	102.00	-0.5%	1.02
1	1	0	1	1	102.00	-0.5%	1.02
1	1	1	0	0	104.00	-0.5%	1.04
1	1	1	0	1	104.00	-0.5%	1.04
1	1	1	1	0	104.00	-0.5%	1.04
1	1	1	1	1	104.00	-0.5%	1.04

**SMBus Table: Frequency Select Register**

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Latched Input or SMBus Frequency Select	RW	Latched Inputs	SMBus	0
Bit 6	-	SS_EN	Spread Enable	RW	OFF	ON	0
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 4	-	CK410#	CPU Freq Select Bit 4	RW	See Table 1: CPU Frequency Selection Table		Latched
Bit 3	-	CPU FS3	CPU SS_EN	RW			0
Bit 2	-	CPU FS_C	CPU Freq Select Bit 2	RW			Latched
Bit 1	-	CPU FS_B	CPU Freq Select Bit 1	RW			Latched
Bit 0	-	CPU FS_A	CPU Freq Select Bit 0	RW			Latched

**NOTE:** Byte 0 bit 6 and Byte 0 bit 3 must **BOTH** be '1' to enable spread for the PCI & CPU clocks.  
Byte 5 bit 4 must be set to 1 to enable spread for the SRC & ATIGCLKS.

**SMBus Table: Output Control Register**

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	50	PCICLK0	Output Enable	RW	Disable	Enable	1
Bit 6	41,40	CPUCLK2	Output Enable	RW	Disable	Enable	1
Bit 5	4	USB_48MHz	Output Enable	RW	Disable	Enable	1
Bit 4	54	REF0	Output Enable	RW	Disable	Enable	1
Bit 3	53	REF1	Output Enable	RW	Disable	Enable	1
Bit 2	52	REF2	Output Enable	RW	Disable	Enable	1
Bit 1	47,46	CPUCLK0	Output Enable	RW	Disable	Enable	1
Bit 0	43,42	CPUCLK1	Output Enable	RW	Disable	Enable	1

**SMBus Table: CLKREQB# Output Control Register**

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	REQBSRC7	CLKREQB# Controls SRC7	RW	Does not control	Controls	0
Bit 6	16,17	REQBSRC6	CLKREQB# Controls SRC6	RW	Does not control	Controls	0
Bit 5	18,19	REQBSRC5	CLKREQB# Controls SRC5	RW	Does not control	Controls	0
Bit 4	22,23	REQBSRC4	CLKREQB# Controls SRC4	RW	Does not control	Controls	0
Bit 3	24,25	REQBSRC3	CLKREQB# Controls SRC3	RW	Does not control	Controls	0
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 0	34,33	REQBSRC0	CLKREQB# Controls SRC0	RW	Does not control	Controls	0

**NOTE:** CPU0\_Stop\_En (Byte2, bit 2) only exists in devices with REV ID = 2 or higher



**SMBus Table: SRCCLK(7:3,0), CLKREQA# Output Control Register**

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	SRCCLK7	Master Output control. Enables or disables output, regardless of CLKREQ# inputs.	RW	Disable	Enable	1
Bit 6	16,17	SRCCLK6		RW	Disable	Enable	1
Bit 5	18,19	SRCCLK5		RW	Disable	Enable	1
Bit 4	22,23	SRCCLK4		RW	Disable	Enable	1
Bit 3	24,25	SRCCLK3		RW	Disable	Enable	1
Bit 2	34,33	SRCCLK0		RW	Disable	Enable	1
Bit 1	24,25	REQASRC3	CLKREQA# Controls SRC3	RW	Does not control	Controls	0
Bit 0	34,33	REQASRC0	CLKREQA# Controls SRC0	RW	Does not control	Controls	0

**SMBus Table: SRCCLK(3,0), ATIGCLK Output Control Register**

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	12,13	REQASRC7	CLKREQA# Controls SRC7	RW	Does not control	Controls	0
Bit 6	16,17	REQASRC6	CLKREQA# Controls SRC6	RW	Does not control	Controls	0
Bit 5	18,19	REQASRC5	CLKREQA# Controls SRC5	RW	Does not control	Controls	0
Bit 4	22,23	REQASRC4	CLKREQA# Controls SRC4	RW	Does not control	Controls	0
Bit 3	27,28	ATIGCLK1	Output Enable These outputs cannot be controlled by CLKREQ# pins.	RW	Disabled	Enabled	1
Bit 2	30,29	ATIGCLK0		RW	Disabled	Enabled	1
Bit 1	CPU, SRC, ATIG	Differential Output Disable Mode	Hi-Z or driven when disabled	RW	Driven	Hi-Z	0
Bit 0	4	USB_48Str	48MHz Strength Control	RW	1X	2X	1

**Note: Do NOT simultaneously select CLKREQA# and CLKREQB# to control an SRC output.  
Behavior of the device is undefined under these conditions.**

**SMBus Table: Output Drive and ATIG Frequency Control Register**

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	52	REF2Str	REF2 Strength Control	RW	1X	2X	1
Bit 6	41,40	CPU2_Stop_En	0 = CPU is free-run 1 = CPU is stopped by	RW	Free-Run	Stoppable	1
Bit 5	43,42	CPU1_Stop_En		RW	Free-Run	Stoppable	1
Bit 4	-	SRCFS4 (SS_EN)	Freq Select Bit 4 (SS_EN)	RW	See Table 2 SRC Frequency Selection		0
Bit 3	-	SRCFS3	Freq Select Bit 3	RW			0
Bit 2	-	SRCFS2	Freq Select Bit 2	RW			0
Bit 1	-	SRCFS1	Freq Select Bit 1	RW			0
Bit 0	-	SRCFS0	Freq Select Bit 0	RW			0

**NOTE: CPU(1:2)\_Stop\_En (Byte5, bit 6:5) only exist in devices with REV ID = 2 or higher**

**SMBus Table: Device ID Register**

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	DevID 7	Device ID MSB	R	-	-	0
Bit 6	-	DevID 6	Device ID 6	R	-	-	0
Bit 5	-	DevID 5	Device ID 5	R	-	-	0
Bit 4	-	DevID 4	Device ID4	R	-	-	1
Bit 3	-	DevID 3	Device ID3	R	-	-	0
Bit 2	-	DevID 2	Device ID2	R	-	-	0
Bit 1	-	DevID 1	Device ID1	R	-	-	1
Bit 0	-	DevID 0	Device ID LSB	R	-	-	1

**SMBus Table: Vendor ID Register**

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	Revision ID Starts at 0 hex for A revision.	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID (0001 = ICS)	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

**SMBus Table: Byte Count Register**

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 9 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			1

**Bytes 9 through 21 are reserved**

**Test Clarification Table**

Comments	HW TEST_SEL/REF2 HW PIN	OUTPUT
1. Power-up w/ TEST_SEL/REF2 > 2.0V to enter test mode.	<0.8V	NORMAL
2. Cycle power to disable test mode	>2.0V	HI-Z

**Absolute Max**

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		$V_{DD} + 0.5V$	V
VDD_In	3.3V Logic Input Supply Voltage	GND - 0.5	$V_{DD} + 0.5V$	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

**Electrical Characteristics - Input/Supply/Common Output Parameters**
 $T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3\text{ V} \pm 5\%$ 

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	$V_{IH}$	3.3 V $\pm 5\%$	2		$V_{DD} + 0.3$	V	1
Input Low Voltage	$V_{IL}$	3.3 V $\pm 5\%$	$V_{SS} - 0.3$		0.8	V	1
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$	-5		5	$\mu\text{A}$	1
Input Low Current	$I_{IL1}$	$V_{IN} = 0\text{ V}$ ; Inputs with no pull-up resistors	-5			$\mu\text{A}$	1
	$I_{IL2}$	$V_{IN} = 0\text{ V}$ ; Inputs with pull-up resistors	-200			$\mu\text{A}$	1
Low Threshold Input-High Voltage	$V_{IH\_FS}$	3.3 V $\pm 5\%$	0.7		$V_{DD} + 0.3$	V	1
Low Threshold Input-Low Voltage	$V_{IL\_FS}$	3.3 V $\pm 5\%$	$V_{SS} - 0.3$		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			400	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			70	mA	1
		all differential pairs tri-stated			12	mA	1
Input Frequency	$F_i$	$V_{DD} = 3.3\text{ V}$		14.31818		MHz	3
Pin Inductance	$L_{pin}$				7	nH	1
Input Capacitance	$C_{IN}$	Logic Inputs			5	pF	1
	$C_{OUT}$	Output pin capacitance			6	pF	1
	$C_{INX}$	X1 & X2 pins			5	pF	1
Clk Stabilization	$T_{STAB}$	From $V_{DD}$ Power-Up or de-assertion of PD# to 1st clock			1.8	ms	1,2
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD#		CPU output enable after PD# de-assertion			300	$\mu\text{s}$	1
Tfall_Pd#		PD# fall time of			5	ns	1
Trise_Pd#		PD# rise time of			5	ns	2
SMBus Voltage	$V_{DD}$		2.7		5.5	V	1
Low-level Output Voltage	$V_{OL}$	@ $I_{PULLUP}$			0.4	V	1
Current sinking at $V_{OL} = 0.4\text{ V}$	$I_{PULLUP}$		4			mA	1
SCLK/SDATA Clock/Data Rise Time	$T_{RI2C}$	(Max $V_{IL} - 0.15$ ) to (Min $V_{IH} + 0.15$ )			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	$T_{FI2C}$	(Min $V_{IH} + 0.15$ ) to (Max $V_{IL} - 0.15$ )			300	ns	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>See timing diagrams for timing requirements.

<sup>3</sup>Input frequency should be measured at the REFOUT pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

**Electrical Characteristics - CPU 0.7V Current Mode Differential Pair**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\mu\text{A}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			$\Omega$	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	400MHz nominal	2.4993		2.5008	ns	2
		400MHz spread	2.4993		2.5133	ns	2
		333.33MHz nominal	2.9991		3.0009	ns	2
		333.33MHz spread	2.9991		3.016	ns	2
		266.66MHz nominal	3.7489		3.7511	ns	2
		266.66MHz spread	3.7489		3.77	ns	2
		200MHz nominal	4.9985		5.0015	ns	2
		200MHz spread	4.9985		5.0266	ns	2
		166.66MHz nominal	5.9982		6.0018	ns	2
		166.66MHz spread	5.9982		6.0320	ns	2
		133.33MHz nominal	7.4978		7.5023	ns	2
		133.33MHz spread	7.4978		7.5400	ns	2
		100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	T <sub>absmin</sub>	400MHz nominal/spread	2.4143			ns	1,2
		333.33MHz nominal/spread	2.9141			ns	1,2
		266.66MHz nominal/spread	3.6639			ns	1,2
		200MHz nominal/spread	4.8735			ns	1,2
		166.66MHz nominal/spread	5.8732			ns	1,2
		133.33MHz nominal/spread	7.3728			ns	1,2
		100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	t <sub>r</sub>	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175		700	ps	1
Fall Time	t <sub>f</sub>	$V_{OH} = 0.525\text{V}$ , $V_{OL} = 0.175\text{V}$	175		700	ps	1
Rise Time Variation	d-t <sub>r</sub>				125	ps	1
Fall Time Variation	d-t <sub>f</sub>				125	ps	1
Duty Cycle	d <sub>t3</sub>	Measurement from differential waveform	45		55	%	1
Skew	t <sub>sk3</sub>	CPU(1:0), $V_T = 50\%$			100	ps	1
Skew	t <sub>sk4</sub>	CPU(1:0) to CPU2_ITP, $V_T = 50\%$			150	ps	1
Jitter, Cycle to cycle	t <sub>jyc-cyc</sub>	Measurement from differential waveform (CPU2_ITP)			125	ps	1
Jitter, Cycle to cycle	t <sub>jyc-cyc</sub>	Measurement from differential waveform, (CPU(1:0))			85	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>3</sup> $I_{REF} = V_{DD}/(3 \times R_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32\text{mA}$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7\text{V}$  @  $Z_O = 50\Omega$ .

### Electrical Characteristics - SRC 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$ ,  $I_{REF} = 475\Omega$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			$\Omega$	1
Voltage High	VHigh	Statistical measurement on single ended signal	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250	350	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges		12	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-300		300	ppm	1,2
Average period	Tperiod	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	Tabmin	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	$t_r$	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175		700	ps	1
Fall Time	$t_f$	$V_{OH} = 0.525\text{V}$ $V_{OL} = 0.175\text{V}$	175		700	ps	1
Rise Time Variation	d- $t_r$			30	125	ps	1
Fall Time Variation	d- $t_f$			30	125	ps	1
Duty Cycle	$d_{t3}$	Measurement from differential waveform	45		55	%	1
Skew	$t_{sk3}$	$V_T = 50\%$			250	ps	1
Jitter, Cycle to cycle	$t_{jyc-cyc}$	Measurement from differential waveform			125	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

<sup>3</sup> $I_{REF} = V_{DD}/(3 \times R_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32\text{mA}$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7\text{V}$  @  $Z_O = 50\Omega$ .

**Electrical Characteristics - PCICLK/PCICLK\_F**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see T <sub>period</sub> min-max values	-300		300	ppm	1,2
Clock period	T <sub>period</sub>	33.33MHz output nominal	29.9910		30.0090	ns	2
		33.33MHz output spread	29.9910		30.1598	ns	2
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.55	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Edge Rate		Rising edge rate	1		4	V/ns	1
Edge Rate		Falling edge rate	1		4	V/ns	1
Rise Time	t <sub>r1</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	0.5		2	ns	1
Fall Time	t <sub>f1</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	0.5		2	ns	1
Duty Cycle	d <sub>t1</sub>	V <sub>T</sub> = 1.5 V	45		55	%	1
Jitter	t <sub>jcy-cyc</sub>	V <sub>T</sub> = 1.5 V			250	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

**Electrical Characteristics - 48MHz, USB**
 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see T <sub>period</sub> min-max values	-100		100	ppm	1,2
Clock period	T <sub>period</sub>	48.00MHz output nominal	20.8313		20.8354	ns	2
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.55	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Edge Rate		Rising edge rate	1		2	V/ns	1
Edge Rate		Falling edge rate	1		2	V/ns	1
Rise Time	t <sub>r1</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	1		2	ns	1
Fall Time	t <sub>f1</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	1		2	ns	1
Duty Cycle	d <sub>t1</sub>	V <sub>T</sub> = 1.5 V	45		55	%	1
Jitter, Cycle to cycle	t <sub>jcy-cyc</sub>	V <sub>T</sub> = 1.5 V			175	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

### Electrical Characteristics - REF-14.318MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see T <sub>period</sub> min-max values	-300		300	ppm	1
Clock period	T <sub>period</sub>	14.318MHz output nominal	69.8270		69.8550	ns	1
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @MIN = 1.0 V, V <sub>OH</sub> @MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @MIN = 1.95 V, @MAX = 0.4 V	29		27	mA	1
Rise Time	t <sub>r1</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	1		2	ns	1
Fall Time	t <sub>f1</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	1		2	ns	1,2
Skew	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 V			500	ps	2
Duty Cycle	d <sub>t1</sub>	V <sub>T</sub> = 1.5 V	45		55	%	1,2
Jitter	t <sub>jycyc-cyc</sub>	V <sub>T</sub> = 1.5 V			1000	ps	1

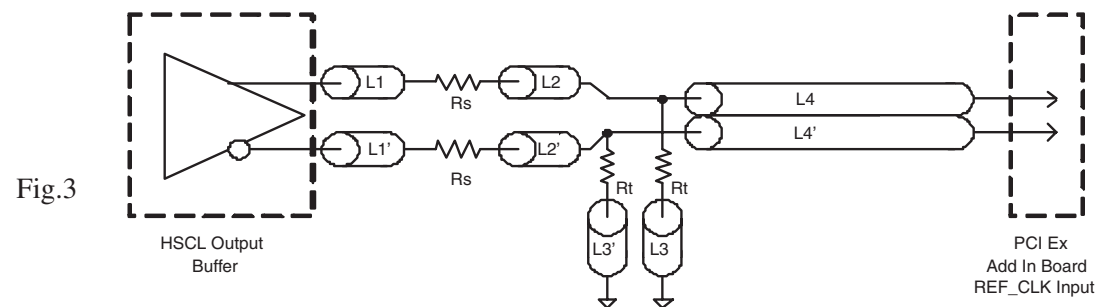
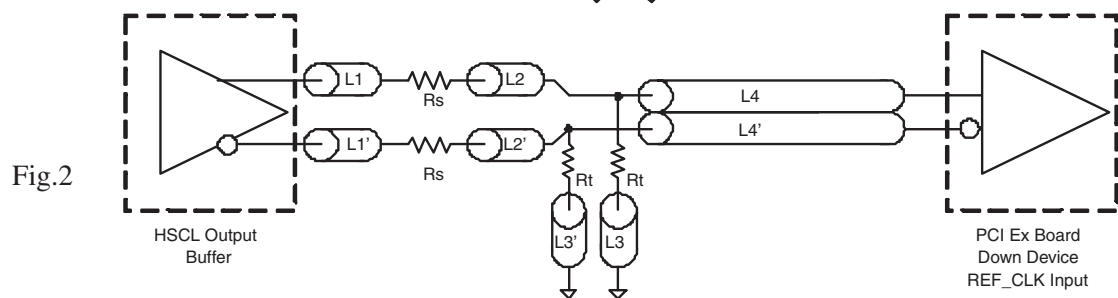
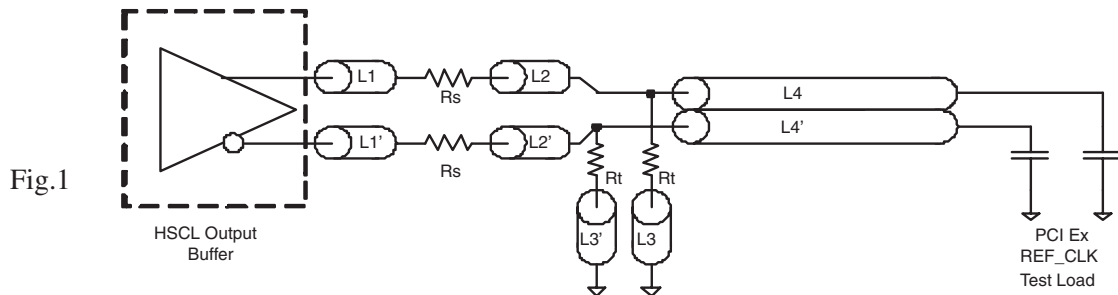
<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	2, 3
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	2, 3
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	2, 3
Rs	33	ohm	2, 3
Rt	49.9	ohm	2, 3

Down Device Differential Routing	Dimension or Value	Unit	Figure
L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace.	2 min to 16 max	inch	2
L4 length, Route as coupled <b>stripline</b> 100 ohm differential trace.	1.8 min to 14.4 max	inch	2

Differential Routing to PCI Express Connector	Dimension or Value	Unit	Figure
L4 length, Route as coupled <b>microstrip</b> 100 ohm differential trace.	0.25 to 14 max	inch	3
L4 length, Route as coupled <b>stripline</b> 100 ohm differential trace.	0.225 min to 12.6 max	inch	3



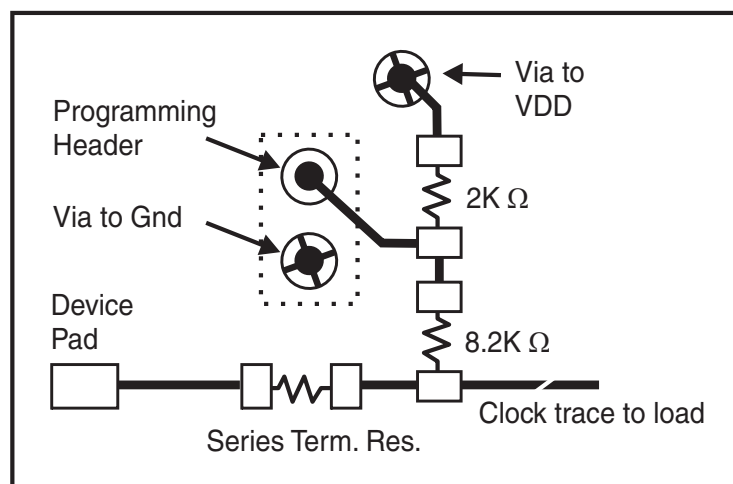


## Shared Pin Operation - Input/Output Pins

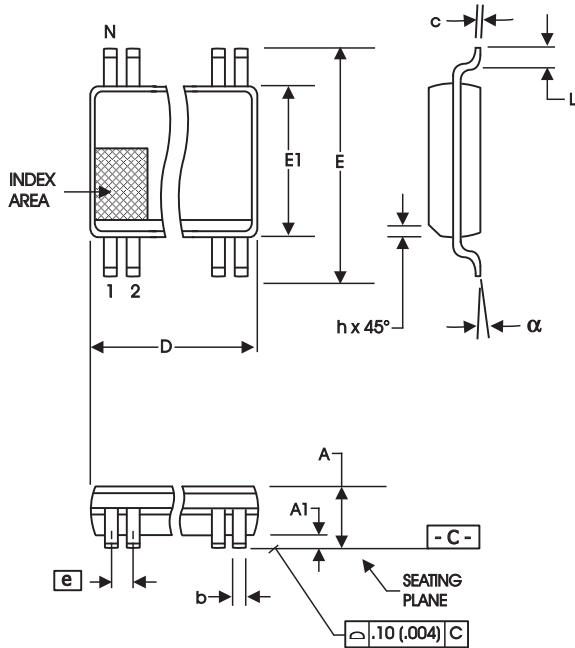
The I/O pins designated by (input/output) on the **ICS951416** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.



**Fig. 1**



**56-Lead, 300 mil Body, 25 mil, SSOP**

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

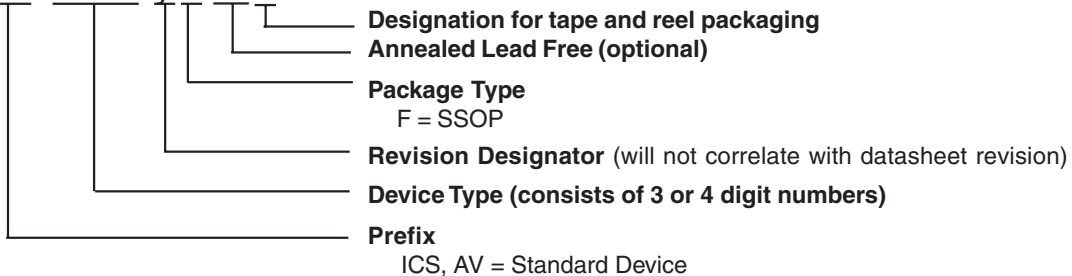
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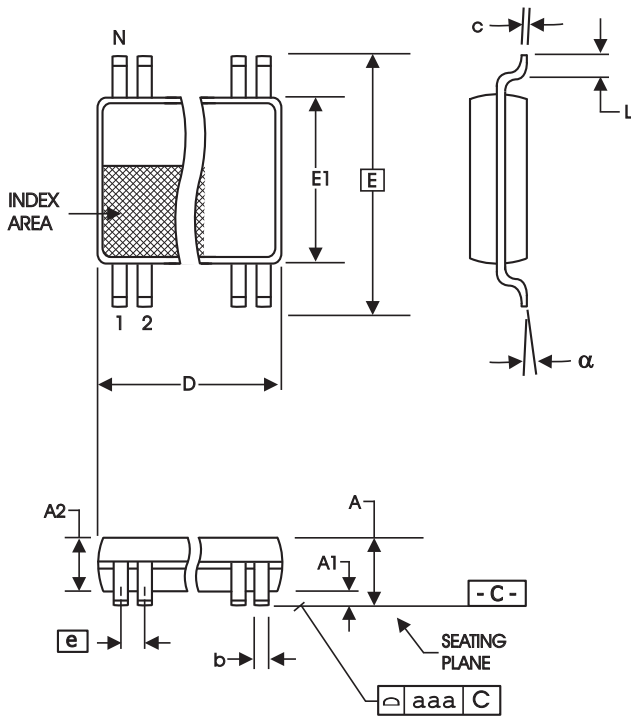
**Ordering Information**

**ICS951411yFLFT**

Example:

**ICS XXXX y F LFT**





**56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP**  
**(240 mil) (20 mil)**

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

**Ordering Information**

**ICS951411yGLFT**

Example:

**ICS XXXX y G LFT**

