SONY

CXD2408AR

Timing Generator for Progressive Scan CCD Image Sensor

Description

The CXD2408AR is an IC developed to generate the timing pulses required by the Progressive Scan CCD image sensors as well as signal processing circuits.

Features

- EIA support
- Electronic shutter function
- Random trigger shutter function
- Sync signal generator
- Supports external synchronization
- Supports non-interlaced operation
- Base oscillation 1560fh (24.5454MHz)

Applications

Progressive Scan CCD cameras

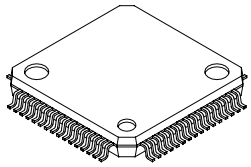
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

ICX074AK, ICX074AL

64 pin LQFP (Plastic)



Absolute Maximum Ratings

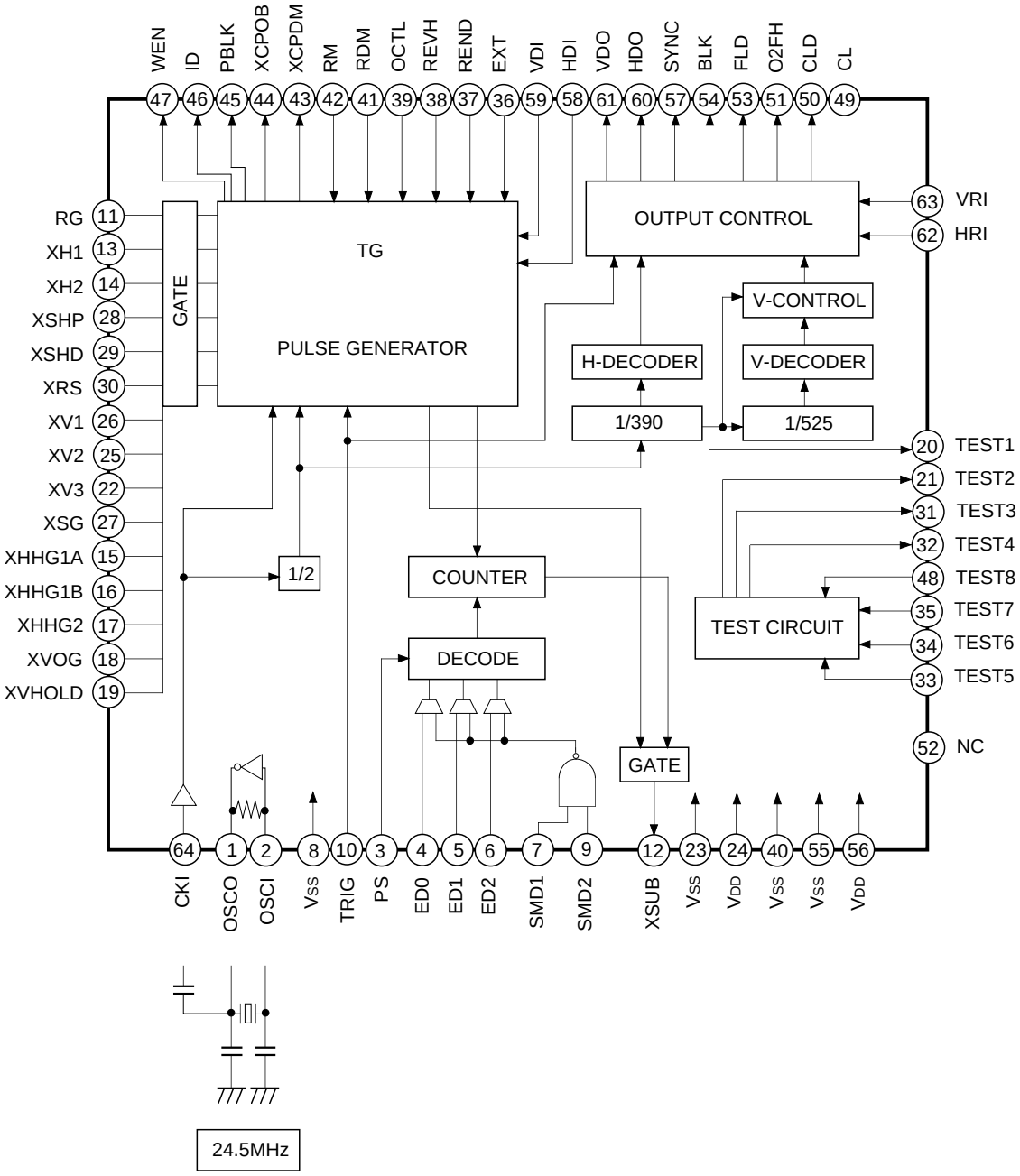
• Supply voltage	V_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

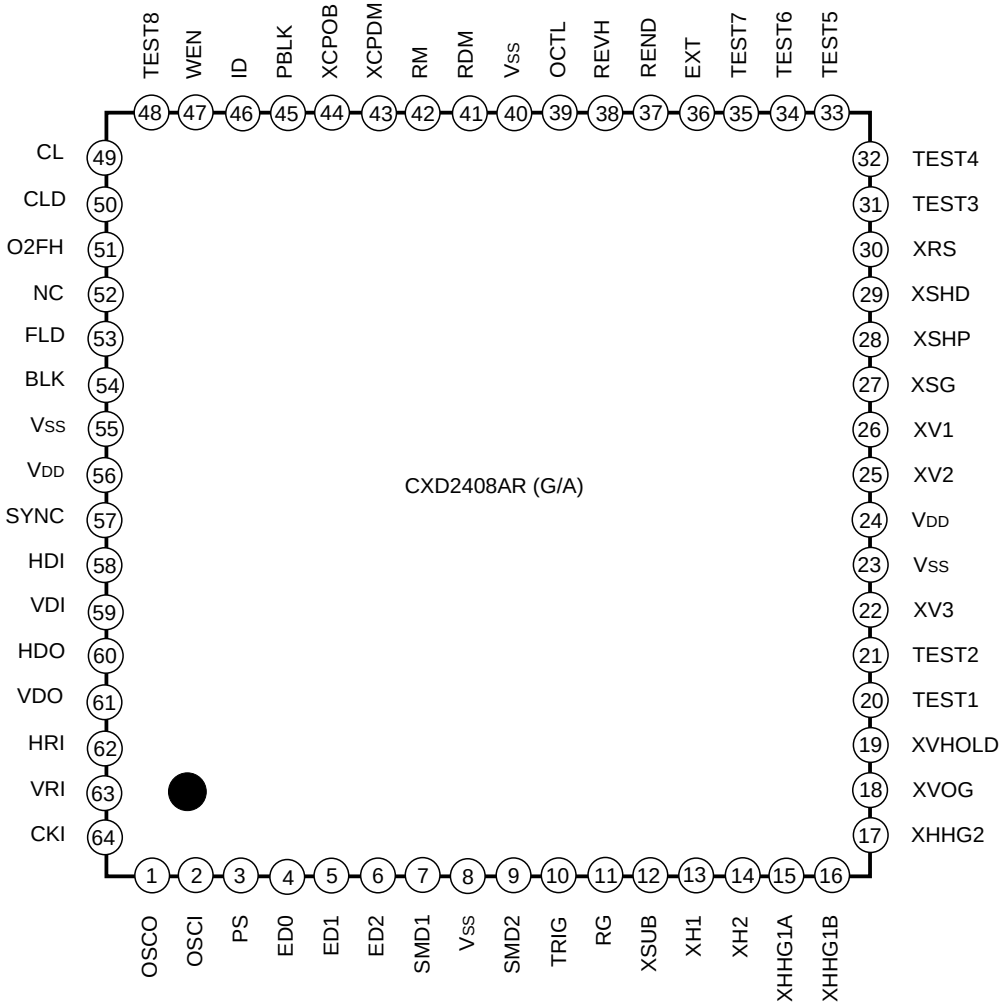
• Supply voltage	V_{DD}	4.75 to 5.25	V
• Operating temperature	Topr	–20 to +75	°C

E96402A68

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	OSCO	O	Inverter output for oscillation.
2	OSCI	I	Inverter input for oscillation.
3	PS	I	Switching for electronic shutter speed input method. (With pull-down resistor) Low: Parallel input, High: Serial input
4	ED0	I	Shutter speed setting. Strobe input for serial mode. (With pull-up resistor)
5	ED1	I	Shutter speed setting. Clock input for serial mode. (With pull-up resistor)
6	ED2	I	Shutter speed setting. Data input for serial mode. (With pull-up resistor)
7	SMD1	I	Shutter mode setting. (With pull-up resistor)
8	Vss	—	GND
9	SMD2	I	Shutter mode setting. (With pull-up resistor)
10	TRIG	I	Trigger input for random trigger shutter.
11	RG	O	Reset gate pulse output.
12	XSUB	O	CCD discharge pulse output.
13	XH1	O	Clock output for CCD horizontal register drive.
14	XH2	O	Clock output for CCD horizontal register drive.
15	XHHG1A	O	Clock output for transfer between CCD horizontal registers.
16	XHHG1B	O	Clock output for transfer between CCD horizontal registers.
17	XHHG2	O	Clock output for transfer between CCD horizontal registers.
18	XVOG	O	Clock output for transfer from CCD vertical register to CCD horizontal register.
19	XVHOLD	O	Clock output for adjusting timing of transfer to CCD horizontal register.
20	TEST1	O	Test output. Normally open.
21	TEST2	O	Test output. Normally open.
22	XV3	O	Clock output for CCD vertical register drive.
23	Vss	—	GND
24	V_{DD}	—	Power supply.
25	XV2	O	Clock output for CCD vertical register drive.
26	XV1	O	Clock output for CCD vertical register drive.
27	XSG	O	CCD sensor charge readout pulse output.
28	XSHP	O	Precharge level sample-and-hold pulse.
29	XSHD	O	Data sample-and-hold pulse.
30	XRS	O	Sample-and-hold pulse.
31	TEST3	O	Test output. Normally open.
32	TEST4	O	Test output. Normally open.
33	TEST5	O	Test output. Normally open.
34	TEST6	O	Test output. Normally open.
35	TEST7	I	Test input. Set at Low in normal operation. (With pull-down resistor)

Pin No.	Symbol	I/O	Description
36	EXT	I	Internal synchronization/external synchronization switching. (With pull-down resistor) Low: Internal synchronization, High: External synchronization
37	REND	I	Normal reset/direct reset switching. (With pull-down resistor) Low: Normal reset, High: Direct reset
38	REVH	I	V reset/HV reset switching. (With pull-down resistor) Low: V reset, High: HV reset
39	OCTL	I	O2FH output control. (With pull-down resistor) Low: No output, High: Output
40	Vss	—	GND
41	RDM	I	Normal operation/random trigger shutter switching. (With pull-down resistor) Low: Normal operation, High: Random trigger shutter
42	RM	I	Switching for output mode. (With pull-down resistor) Low: Non-interlaced, High: Interlaced
43	XCPDM	O	Clamp pulse output.
44	XCPOB	O	Clamp pulse output.
45	PBLK	O	Blanking cleaning pulse output.
46	ID	O	Line identification output.
47	WEN	O	Write enable output.
48	TEST8	I	Test input. (With pull-down resistor)
49	CL	O	fck clock output. (0°)
50	CLD	O	fck clock output. (180°)
51	O2FH	O	2 fH output.
52	NC	—	
53	FLD	O	Field pulse output.
54	BLK	O	Composite blanking output.
55	Vss	—	GND
56	V_{DD}	—	Power supply.
57	SYNC	O	Composite sync output.
58	HDI	I	Horizontal sync signal input.
59	VDI	I	Vertical sync signal input.
60	HDO	O	Horizontal sync signal output.
61	VDO	O	Vertical sync signal output.
62	HRI	I	Horizontal reset signal input.
63	VRI	I	Vertical reset signal input.
64	CKI	I	2 fck clock input.

Electrical Characteristics

DC Characteristics

(V_{DD} = 4.75 to 5.25V, Topr = –20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.75	5.0	5.25	V
Input voltage 1 (Input pins other than those below)	V_{IH1}		0.7V_{DD}			V
	V_{IL1}				0.3V_{DD}	V
Input voltage 2 (Pins 7, 9, 10, 58, 59, 62, 63, and 64)	V_{IH2}		0.7V_{DD}			V
	V_{IL2}				0.3V_{DD}	V
Output voltage 1 (Output pins other than those below)	V_{OH1}	I_{OH} = –2mA	–0.8			V
	V_{OL1}	I_{OL} = 4mA			0.4	V
Output voltage 2 (Pins 28, 29, 30, 31, 32, 33, 34, 49 and 50)	V_{OH2}	I_{OH} = –4mA	–0.8			V
	V_{OL2}	I_{OL} = 8mA			0.4	V
Output voltage 3 (Pins 11, 13, and 14)	V_{OH3}	I_{OH} = –12mA	V_{DD} – 0.8			V
	V_{OL3}	I_{OL} = 12mA			0.4	V
Output voltage 4 (Pin 1)	V_{OH4}	I_{OH} = –12mA	V_{DD}/2			V
	V_{OL4}	I_{OL} = 12mA			V_{DD}/2	V
Feedback resistor	R_{FB}	V_{IN} = Vss or V_{DD}	250k	1M	2.5M	Ω
Pull-up resistor	R_{PU}	V_{IL} = 0V		50k		Ω
Pull-down resistor	R_{PD}	V_{IN} = V_{DD}		50k		Ω
Current consumption	I_{DD}	V_{DD} = 5V ICX074AL in normal operating state		35		mA

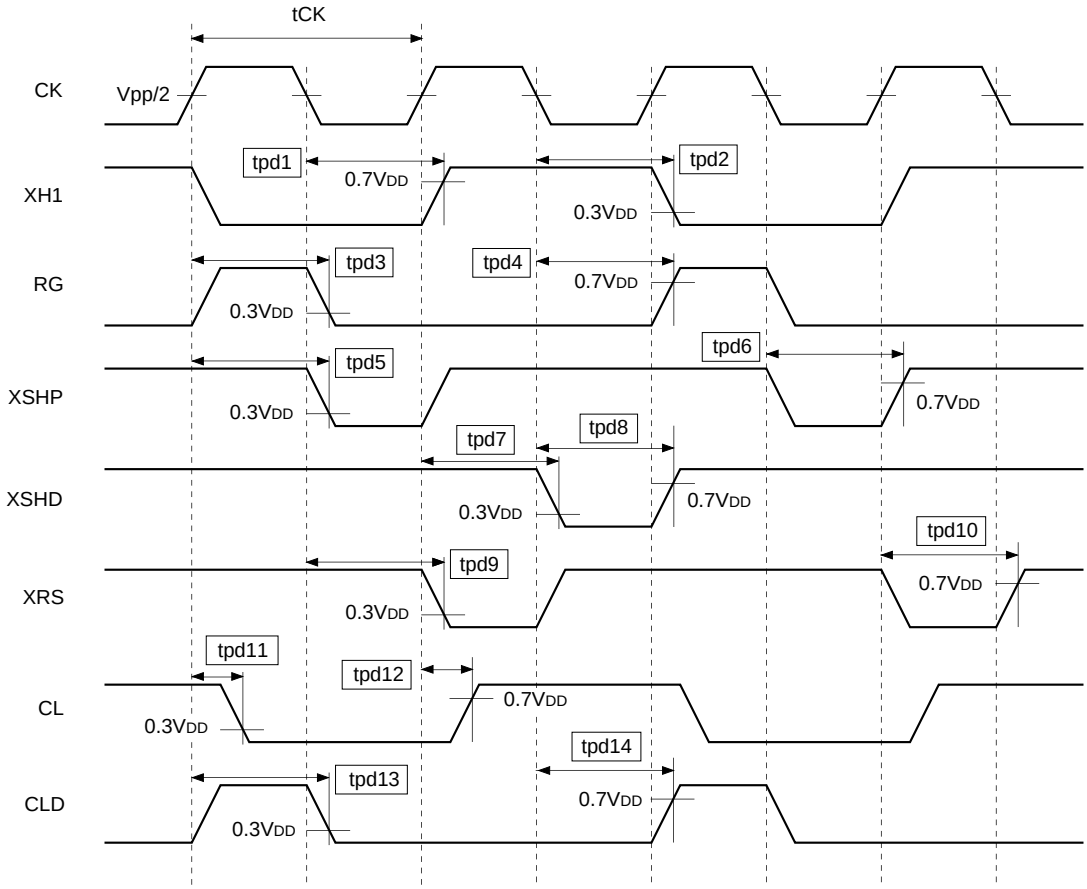
I/O Pin Capacitances

(V_{DD} = V_I = 0V, f_M = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}	—	—	9	pF
Output pin capacitance	C_{OUT}	—	—	11	pF

AC Characteristics

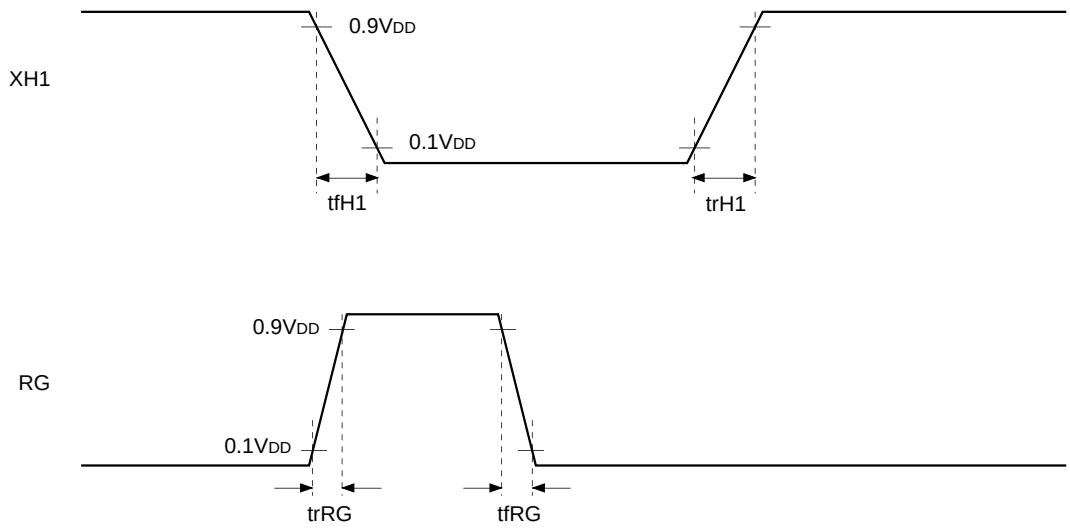
1) Phase characteristics of XH1, RG, XSHP, XSHD, XRS, CL, and CLD



(V_{DD} = 5.0V, Topr = 25°C, Load capacity of CL and CLD = 30pF, Load capacity of XH1, XSHP, XSHD, XRS, and RG = 10pF)

Symbol	Definition	Typ.	Unit
t_{CK}	CK cycle	41	ns
tpd1	XH1 rising delay, activated by the falling edge of CK	28	ns
tpd2	XH1 falling delay, activated by the falling edge of CK	29	ns
tpd3	RG falling delay, activated by the rising edge of CK	27	ns
tpd4	RG rising delay, activated by the falling edge of CK	33	ns
tpd5	XSHP falling delay, activated by the rising edge of CK	36	ns
tpd6	XSHP rising delay, activated by the falling edge of CK	30	ns
tpd7	XSHD falling delay, activated by the rising edge of CK	36	ns
tpd8	XSHD rising delay, activated by the falling edge of CK	29	ns
tpd9	XRS falling delay, activated by the falling edge of CK	34	ns
tpd10	XRS rising delay, activated by the rising edge of CK	28	ns
tpd11	CL falling delay, activated by the rising edge of CK	15	ns
tpd12	CL rising delay, activated by the rising edge of CK	17	ns
tpd13	CLD falling delay, activated by the rising edge of CK	30	ns
tpd14	CLD rising delay, activated by the falling edge of CK	33	ns

Waveform Characteristics of XH1 and RG

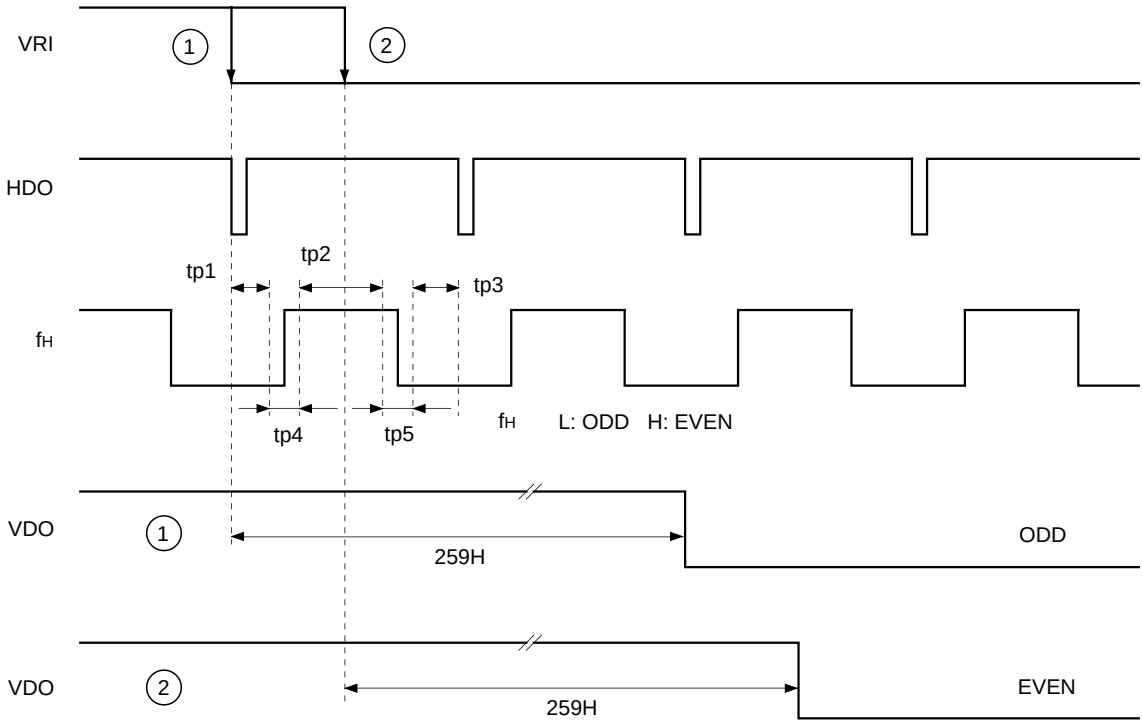


(V_{DD} = 5.0V, Topr = 25°C, Load capacity of XH1 = 10pF, Load capacity of RG = 10pF)

Symbol	Definition	Typ.	Unit
trH1	XH1 rise time	2	ns
tfH1	XH1 fall time	2	ns
trRG	RG rise time	2	ns
tfRG	RG fall time	2	ns

• In the normal reset mode, the signal output is reset to ODD or EVEN field depending on the input timing of the vertical reset signal as shown in the figure below.

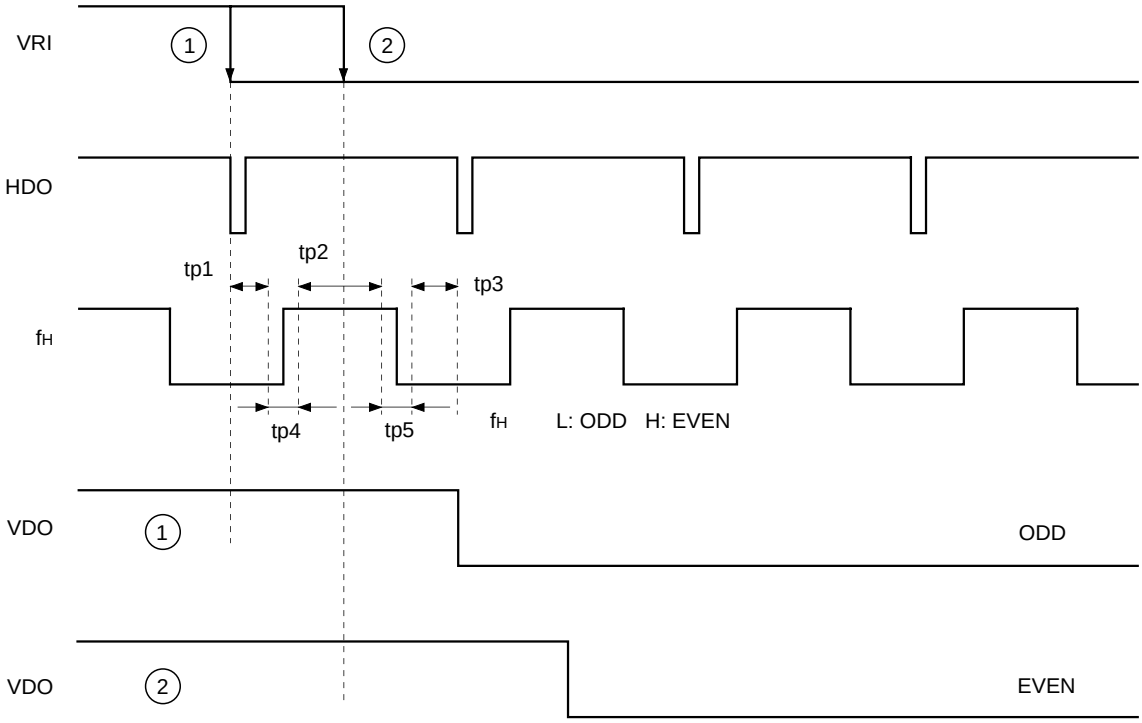
Field identification



Symbol	Definition	Specified value	Unit
tp1	Range of resetting to ODD	21.9	µs
tp2	Range of resetting to EVEN	31.6	µs
tp3	Range of resetting to ODD	9.7	µs
tp4	Prohibited area	200	ns
tp5	Prohibited area	200	ns

• In the direct reset mode, the signal output is reset to ODD or EVEN field depending on the input timing of the vertical reset signal as shown in the figure below.

Field identification



Symbol	Definition	Specified value	Unit
tp1	Range of resetting to ODD	21.9	µs
tp2	Range of resetting to EVEN	31.6	µs
tp3*	Range of resetting to ODD	—	µs
tp4	Prohibited area	200	ns
tp5	Prohibited area	200	ns

* In the direct reset mode, the cycle of HD can be arbitrary. Therefore, tp3 is not specified.

Description of Operation

1. Mode Control

Symbol	Pin No.	L	H	Remarks
RM	42	1/30s non-interlaced	1/60s interlaced	
RDM	41	Normal operation	Random trigger shutter	
PS	3	Parallel	Serial	Electronic shutter speed input method
EXT	36	Internal synchronization	External synchronization	
REND	37	Normal reset	Direct reset	
REVH	38	V reset	HV reset	

2. Mode Relationships

RM	L			H		
	1/30s non-interlaced			1/60s interlaced		
EXT	L		H	L		H
	Internal synchronization		External synchronization	Internal synchronization		External synchronization
RDM	L	H		L	H	
	Normal operation	Random trigger shutter	Normal operation	Normal operation	Random trigger shutter	Normal operation
REND			Direct reset			L: Normal reset; H: Direct reset
REVH			L: V reset; H: HV reset			L: V reset; H: HV reset

: Disabled

3. Electronic Shutter

<Shutter Modes>

SMD1	SMD2	
L	L	Flickerless: Eliminates fluorescent frequency-induced flicker.
L	H	High-speed shutter: Shutter speed faster than 1/60
H	L	Low-speed shutter: Shutter speed slower than 1/60
H	H	No shutter operation

<Shutter Mode and Speed Setting Method>

PS = Low : Parallel input; set by ED0 to ED2, SMD1, and SMD2.

PS = High : Serial input; set by inputting ED0 (strobe), ED1 (clock), and ED2 (data) to each pin.

3-1. Parallel input

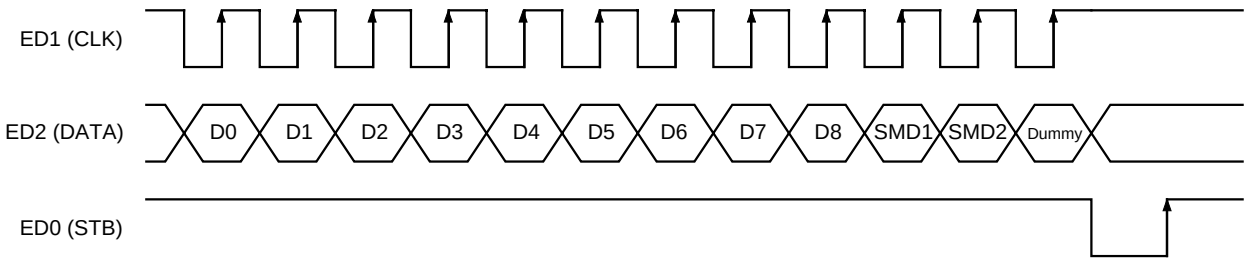
Shutter Speed Compatibility Chart

Mode	PS	SMD1	SMD2	ED0	ED1	ED2	Shutter speed
OFF	L	H	H	X	X	X	Shutter off*
Flickerless	L	L	L	X	X	X	1/100 (s)
High-speed shutter	L	L	H	H	H	H	1/60 (s)
	L	L	H	L	H	H	1/125 (s)
	L	L	H	H	L	H	1/250 (s)
	L	L	H	L	L	H	1/500 (s)
	L	L	H	H	H	L	1/1000 (s)
	L	L	H	L	H	L	1/2000 (s)
	L	L	H	H	L	L	1/4000 (s)
	L	L	H	L	L	L	1/10000 (s)
Low-speed shutter	L	H	L	H	H	H	2FLD
	L	H	L	L	H	H	4FLD
	L	H	L	H	L	H	6FLD
	L	H	L	L	L	H	8FLD
	L	H	L	H	H	L	10FLD
	L	H	L	L	H	L	12FLD
	L	H	L	H	L	L	14FLD
	L	H	L	L	L	L	16FLD

* Shutter speed is 1/30s in 1/30s mode, and 1/60s in 1/60s mode.

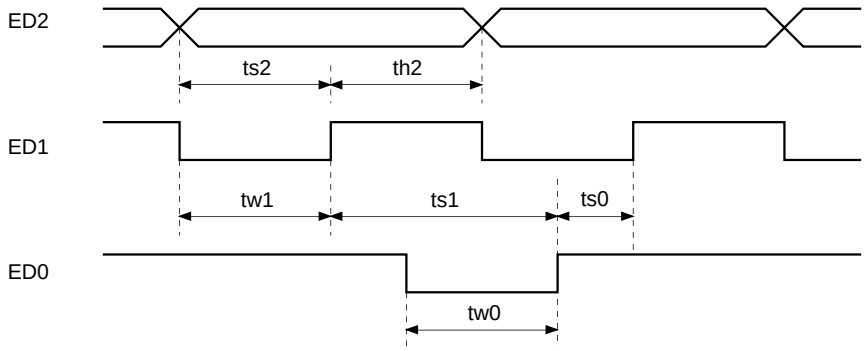
3-2. Serial input

• For serial input (PS = High), SMD1 and SMD2 bits within ED2 (DATA) take priority over SMD1 (Pin 7) and SMD2 (Pin 9) pins as SMD1 and SMD2 (shutter mode control). In this case, control by SMD1 and SMD2 pins is invalid.



ED2 data is latched to the register at the rise of ED1, and transferred to the within at the rise of ED0.

AC Characteristics



Symbol	Definition	Min.	Max.
ts2	ED2 set-up time, activated by the falling edge of ED1	20ns	—
th2	ED2 hold time, activated by the rising edge of ED1	20ns	—
ts1	ED1 rising set-up time, activated by the rising edge of ED0	20ns	—
tw0	ED0 pulse width	20ns	50µs
ts0	ED0 rising set-up time, activated by the rising edge of ED1	20ns	—
tw1	ED1 pulse width (serial input)	20ns	—

3-3. Shutter speed calculation formula

High-speed shutter

$T = [262_{10} - (1FF_{16} - L_{16})] \times 63.56 + 34.78\ (\mu s)$

(*L_{16} = Load value)

Load value	Shutter speed	Calculated value
$0FA_{16}$	1/10000	1/10169
$0FC_{16}$	1/4000	1/4435
100_{16}	1/2000	1/2085
108_{16}	1/1000	1/1012
118_{16}	1/500	1/499
137_{16}	1/250	1/252
176_{16}	1/125	1/125
196_{16}	1/100	1/100

Low-speed shutter

$N = 2 \times (1FF_{16} - L_{16})$ FLD

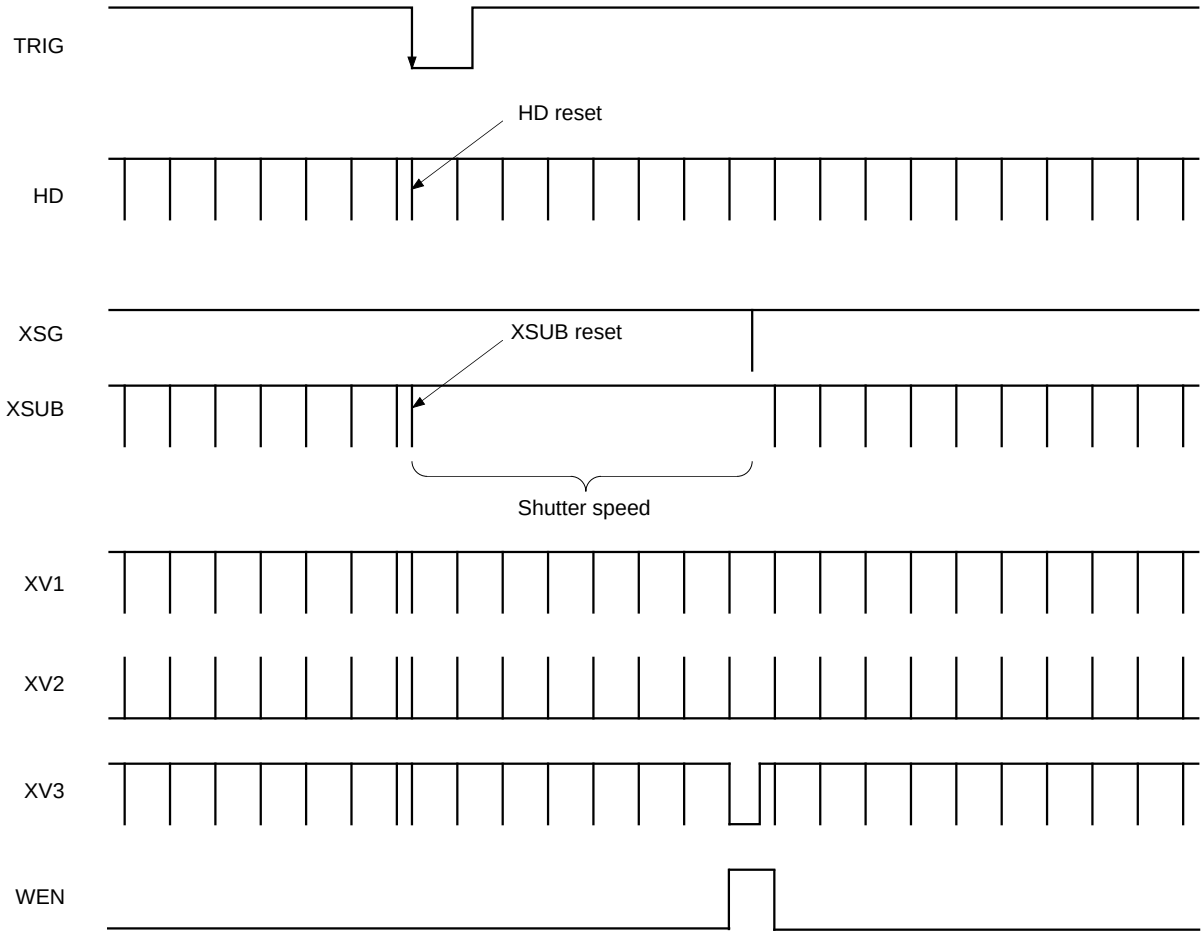
However, the load value of FF_{16} cannot be used .

Load value	Shutter speed (FLD)
$1FE_{16}$	2
$1FD_{16}$	4
:	:
101_{16}	508
100_{16}	510

* In case of starting with serial input setting (PS = H), be sure to transfer shutter speed data in the range of specification after power is turned on, and then use it..

4. Random Trigger Shutter

The random trigger shutter is different from the conventional electronic shutter in that the exposure beginning can be freely set. The exposure period (shutter speed) can be set as with the conventional electronic shutter.
In this mode, XSUB rises for each 1H, and the charge stored in the sensor is discharged. Because the V clock (XV1 to XV3) is continuously operating, any unneeded charge in the vertical CCD is eliminated.
XSG pulse is stopped until the external trigger is detected. The image cannot be monitored until the external trigger is detected and the signal is read out.
When an external trigger is input in this state, HD is forcibly reset when the trigger falls, and XSUB falls once to clear the charge and then halts. XV1 to XV3, XCPDM, XCPOB, and PBLK are reset with HD. From this point, exposure begins, and after the preset exposure period has passed, the XSG pulse falls, the charge is transferred from the sensor to the vertical CCD, and exposure ends. The XSG pulse falls with the time set as in conventional electronic shutters, regardless of VD. Because HD is reset, the exposure period is accurate in 1H units. The WEN pulse is generated synchronously with the XSG pulse. As the WEN pulse specifies the signal start, it can be used as the sync signal for writing image data into the frame memory.
In the random trigger shutter mode, V-direction functions of a sync signal generator are halted. As a result, sync signals VD and FLD are also halted.



5. External Synchronization - Reset

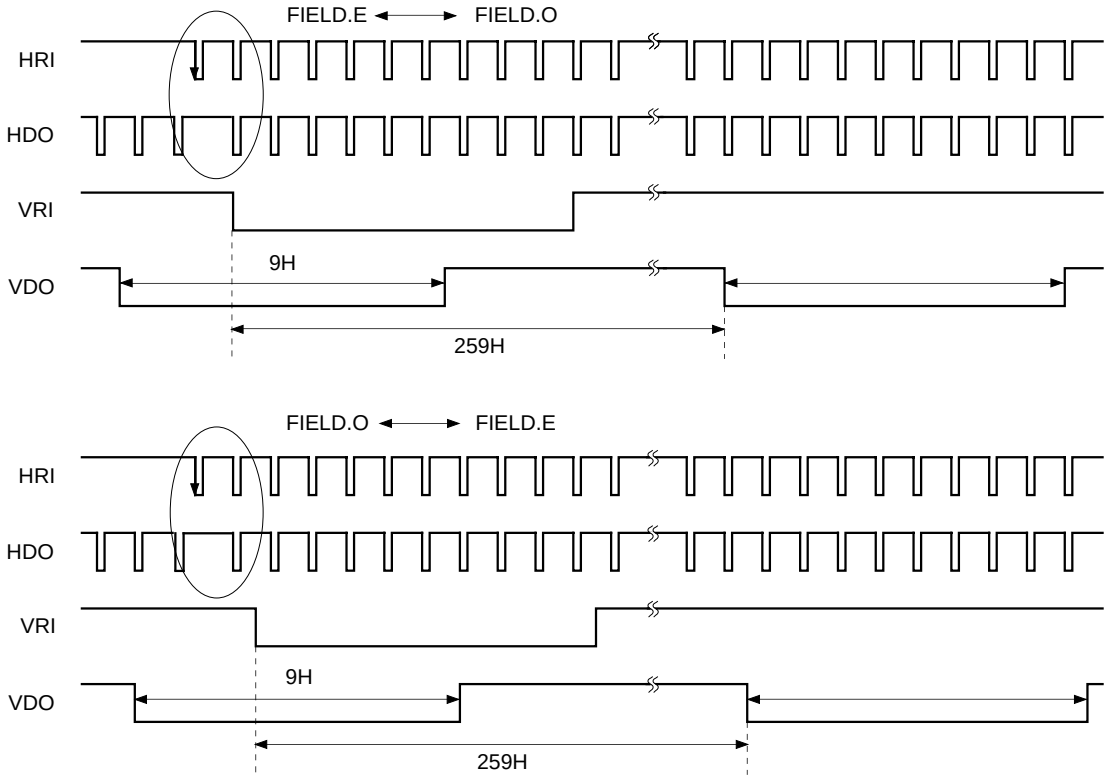
HD and VD are reset to synchronize with the external sync signal.
Resetting is done to synchronize a plural number of camera systems whose clock frequencies are the same.
There are two reset inputs: HRI and VRI. When their falling edge is detected, resetting is carried out. The CXD2408AR has two reset modes: normal reset and direct reset. Details of the reset modes are described in the following pages.

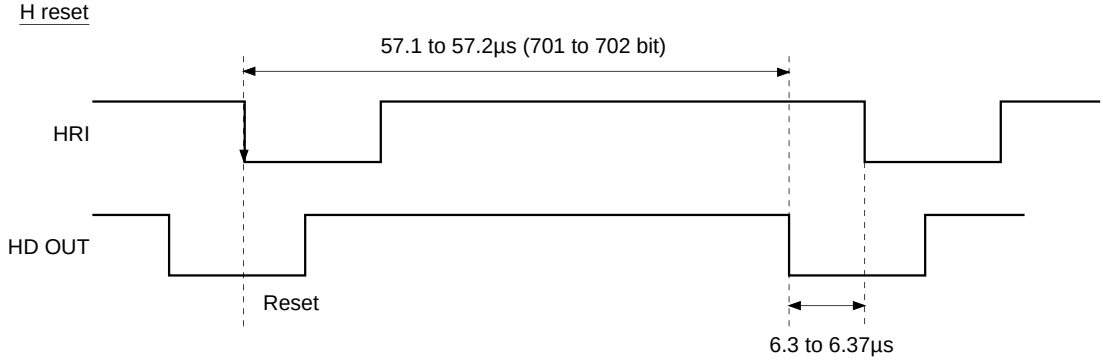
In the 1/30s non-interlaced readout mode, the normal reset mode is not supported, and although the direct reset mode is supported, the field is not identified.

5-1. Normal reset

In the normal reset mode, the reset signal is input for resetting, and the sync signal is output continuously from that time. Only the mode which resets both HD and VD (HV reset) is supported.
When the H reset signal HRI is continuously with an H cycle, resetting is triggered at the first falling edge, and after that point no resets are triggered at edges unless HD after resetting exceeds 2bits (163ns) on the internal clock. In other words, the HRI input jitter is absorbed when it is up to 163 ns. The HRI minimum reset pulse width is 0.3µs.
In the V direction, counting begins from VRI fall, and V is reset to cause VDO to fall after 262.5 – 3.5 = 259H. The VRI minimum reset pulse width is 2H.

Resetting is done for ODD or EVEN field, depending on the input timing of the V reset signal. The identification timing is shown in Electrical Characteristics (Field identification).





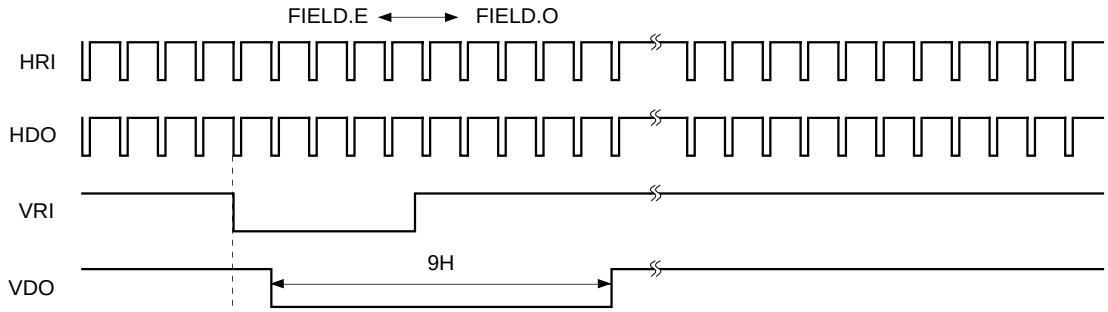
5-2. Direct reset

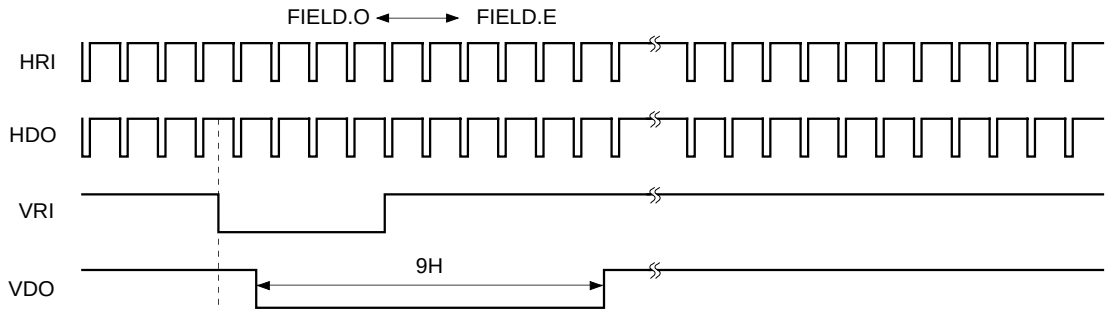
In the direct reset mode, when the reset signal is input for resetting, a sync signal is output, but there is no continuous output.
There are two direct reset modes: one to direct reset VD only (V reset), and one to reset both HD and VD (HV reset). (However, note that even for V reset, the HRI signal is acceptable and the reset timing is the same as in normal reset mode.) In both modes, the VD reset timing is the same.

When the external input V reset signal VRI fall is detected, a judgment is made as to ODD or EVEN. If ODD, V is reset to cause VDO to fall simultaneously with HD fall, and if EVEN, V is reset to cause VDO to fall simultaneously in the middle of HD. VRI requires a minimum pulse width of 2H.
H direct reset detects the fall of H reset signal HRI, and resets H so that HDO falls at the next CL falling edge.
The minimum HRI reset pulse width is 0.3µs.

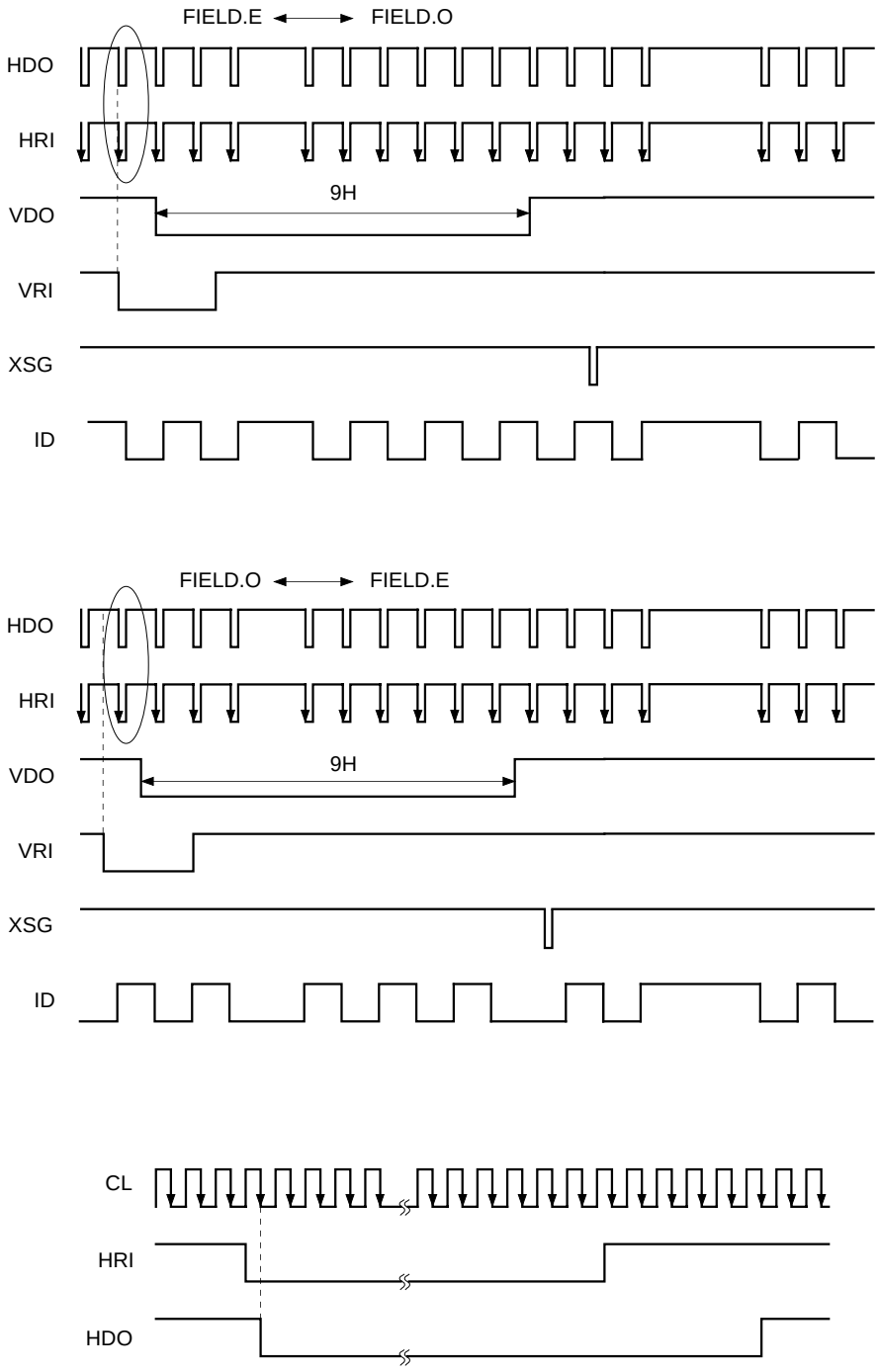
Resetting is done for ODD or EVEN field, depending on the input timing of the V reset signal. The identification timing is shown in Electrical Characteristics (Field identification).

5-2-1. V reset

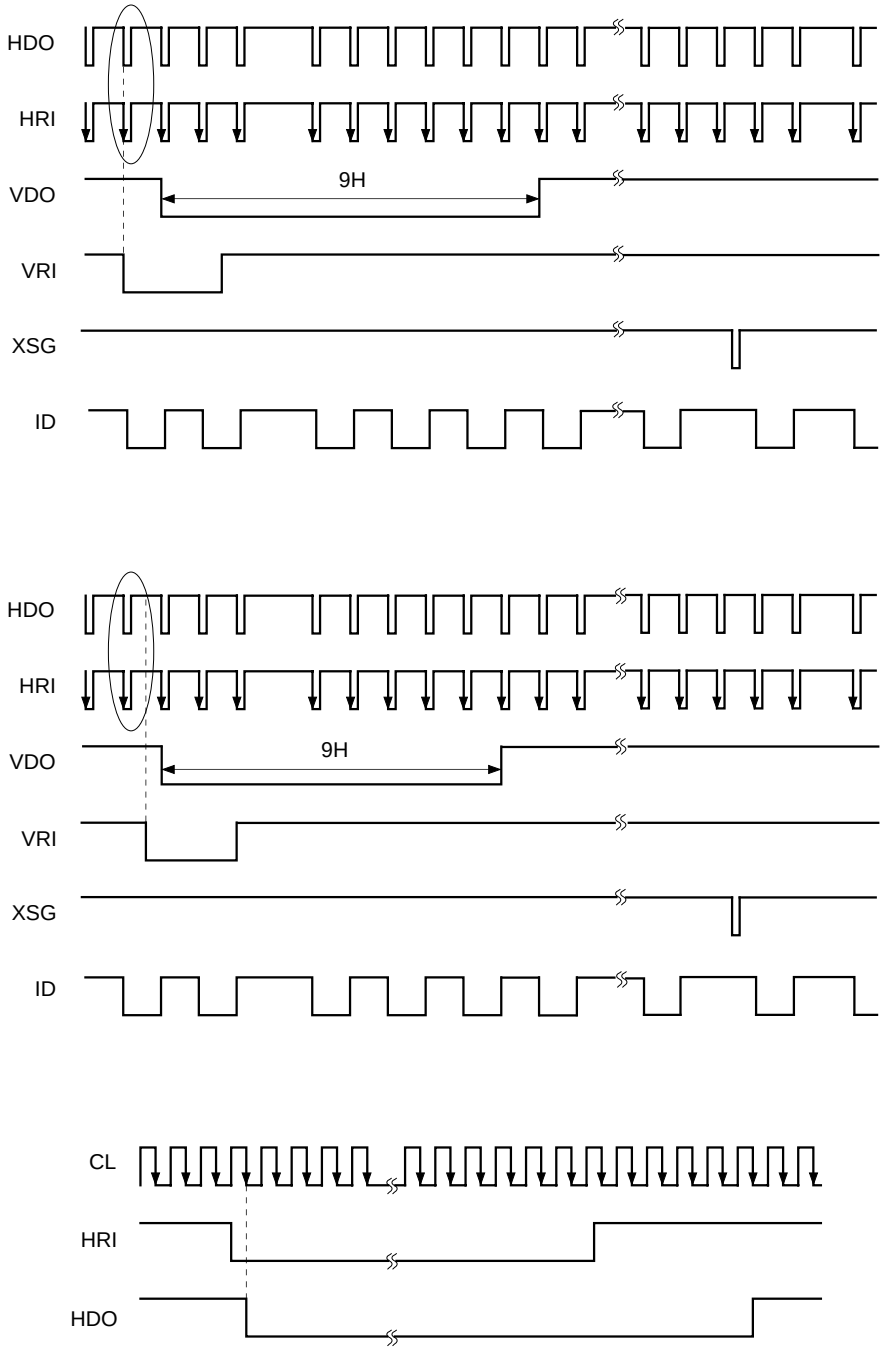




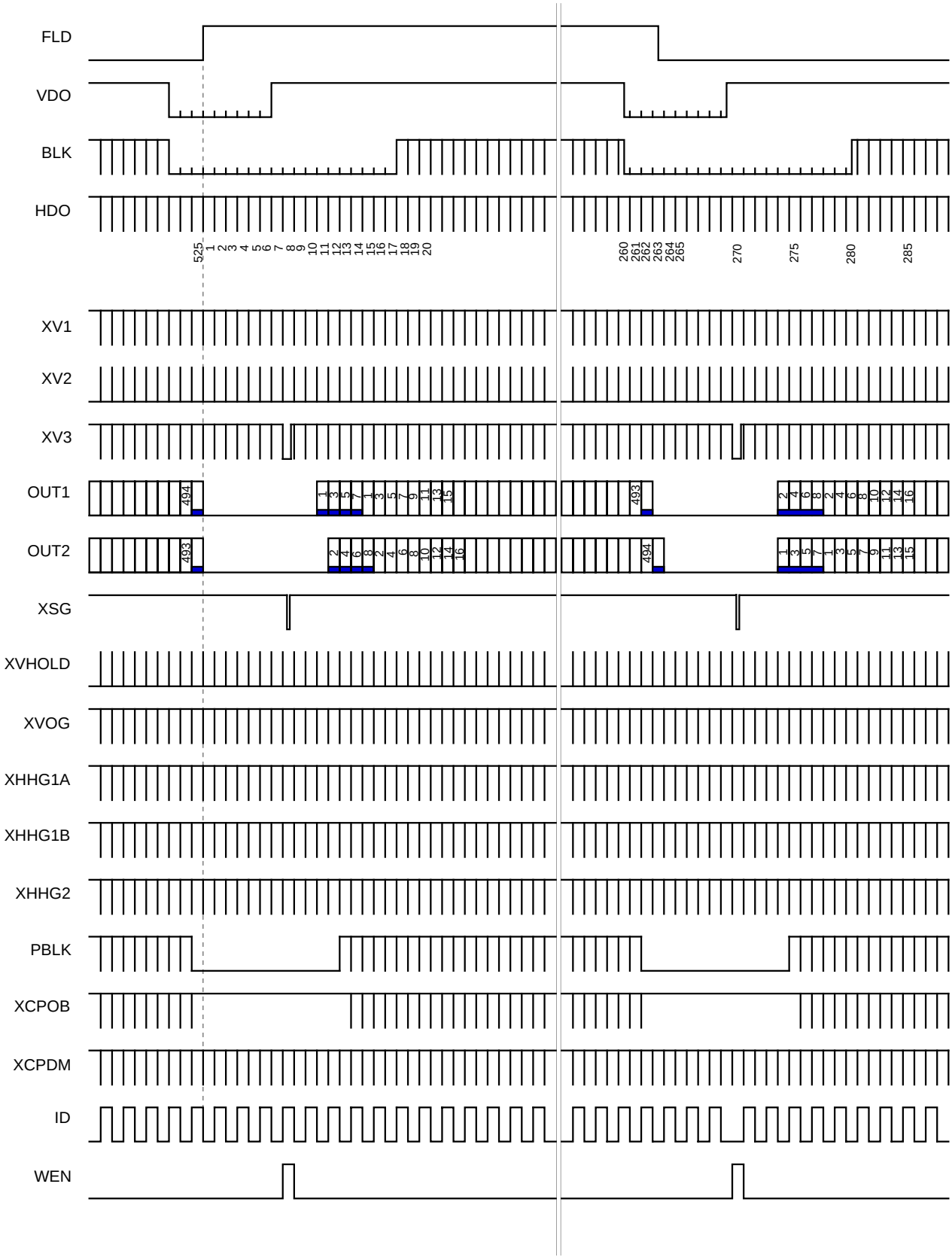
5-2-2. HV reset (1/60s interlaced readout mode)



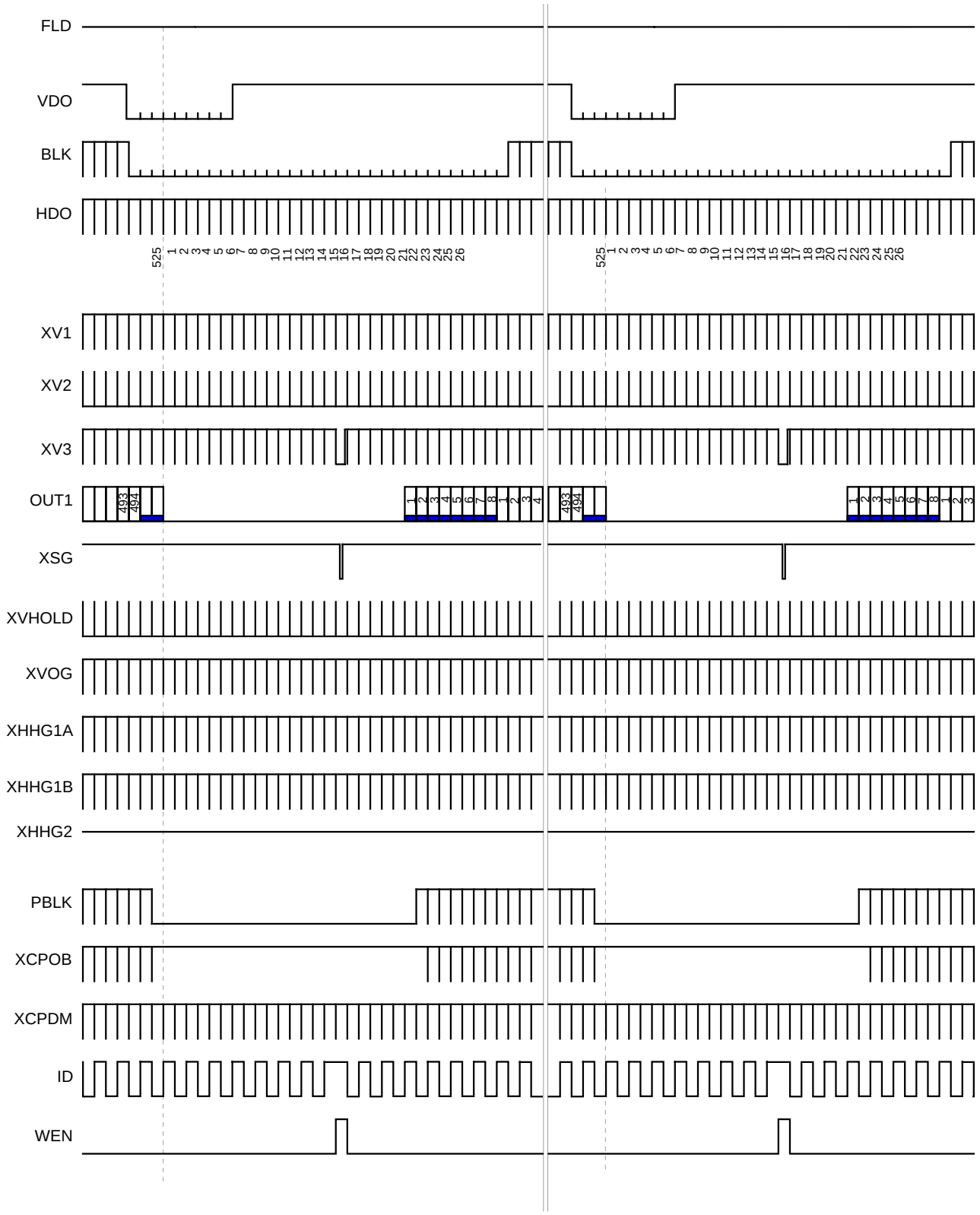
5-2-3. HV reset (1/30s non-interlaced readout mode)



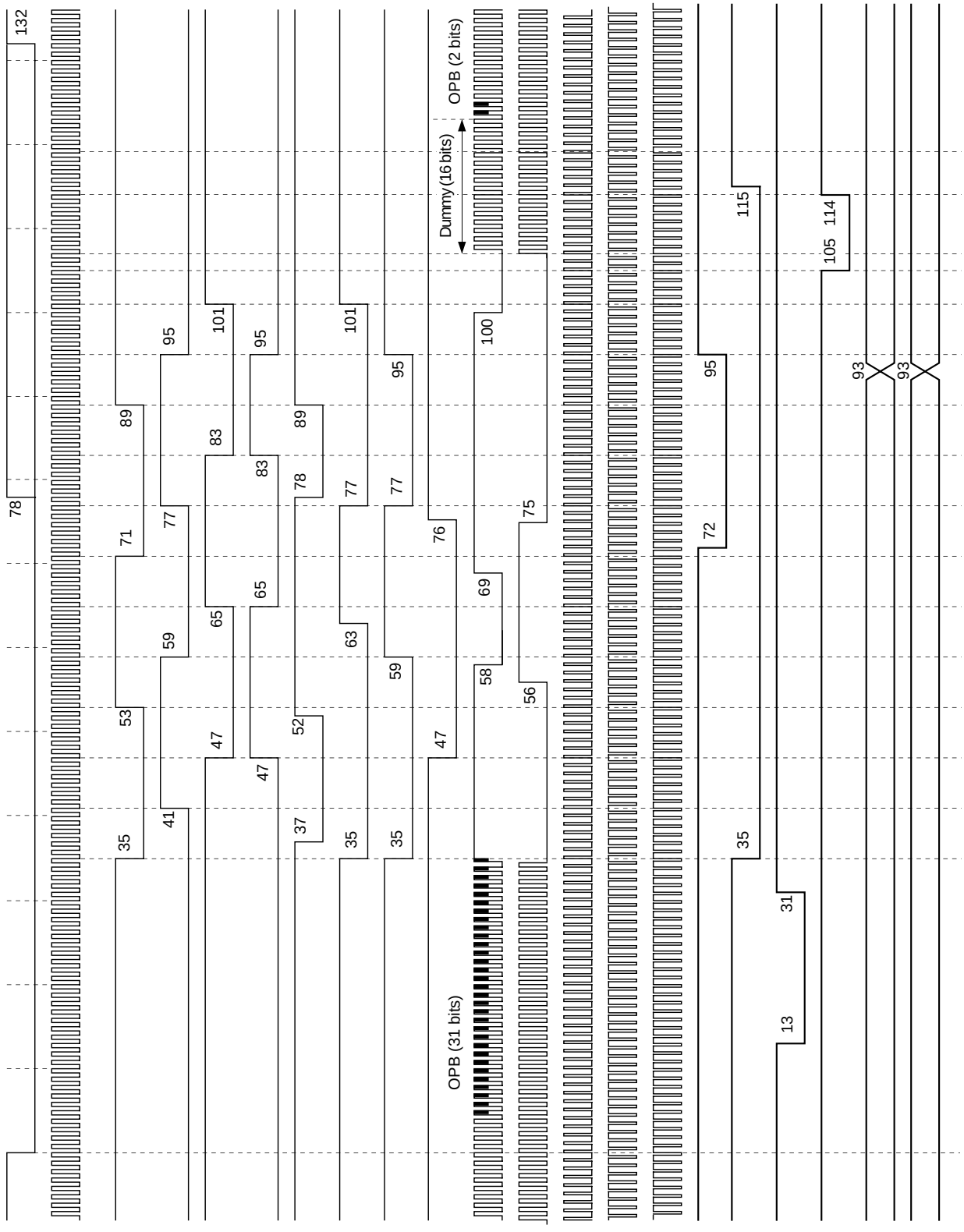
Timing Chart (1) <Vertical direction> 1/60s interlaced readout (RM = High)



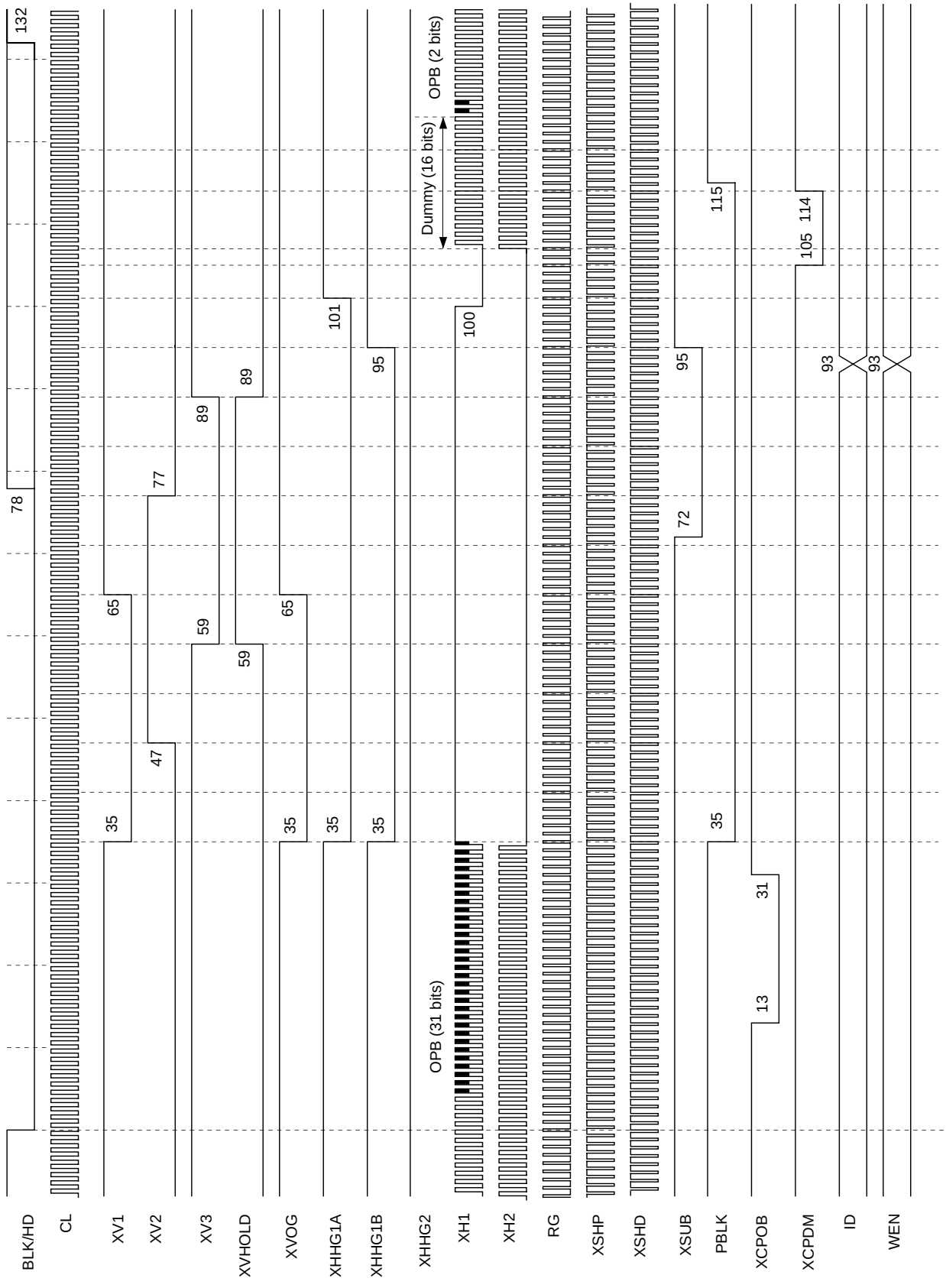
Timing Chart (2) <Vertical direction> 1/30s non-interlaced readout (RM = Low)



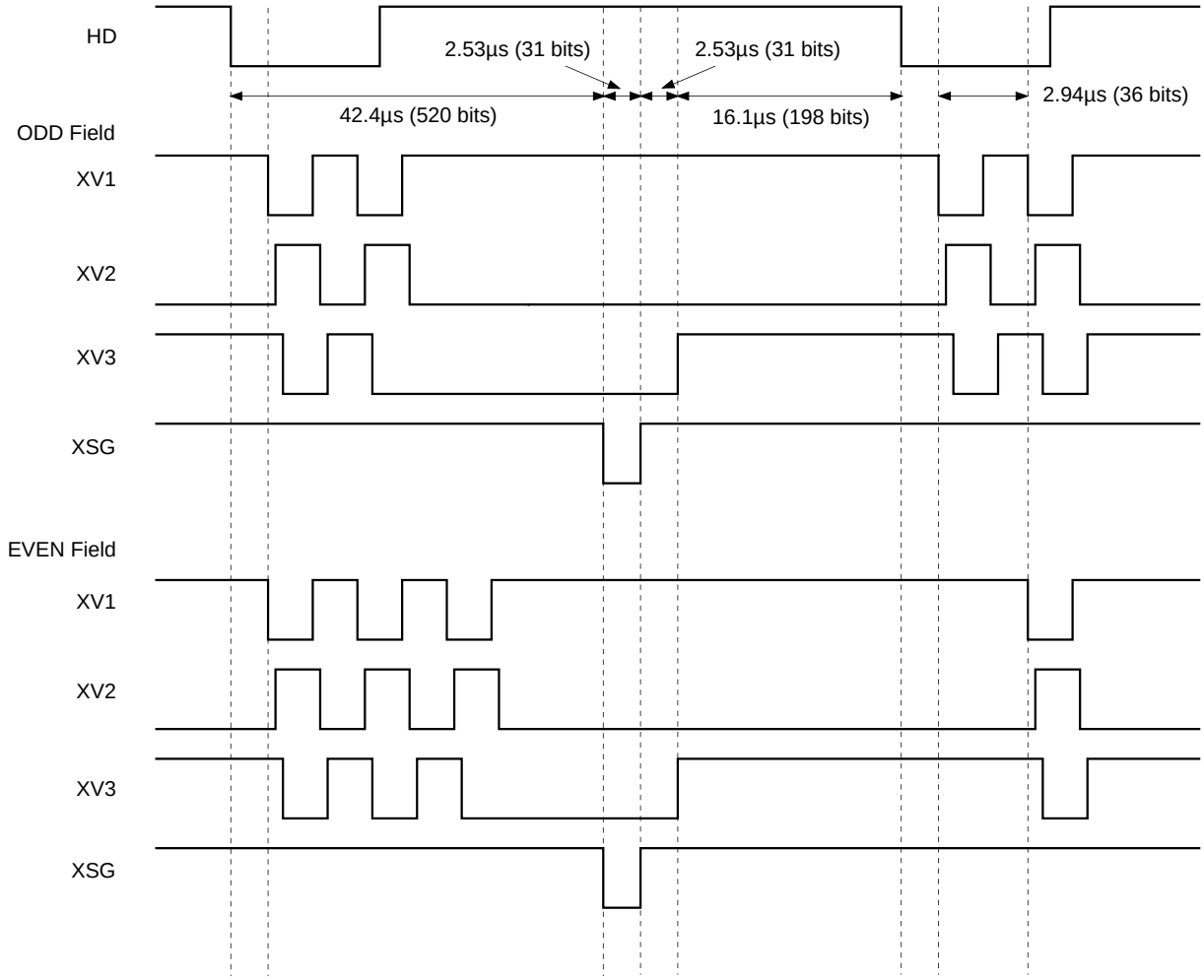
Timing Chart (3) <Horizontal direction> 1/60s interlaced readout (RM = High)



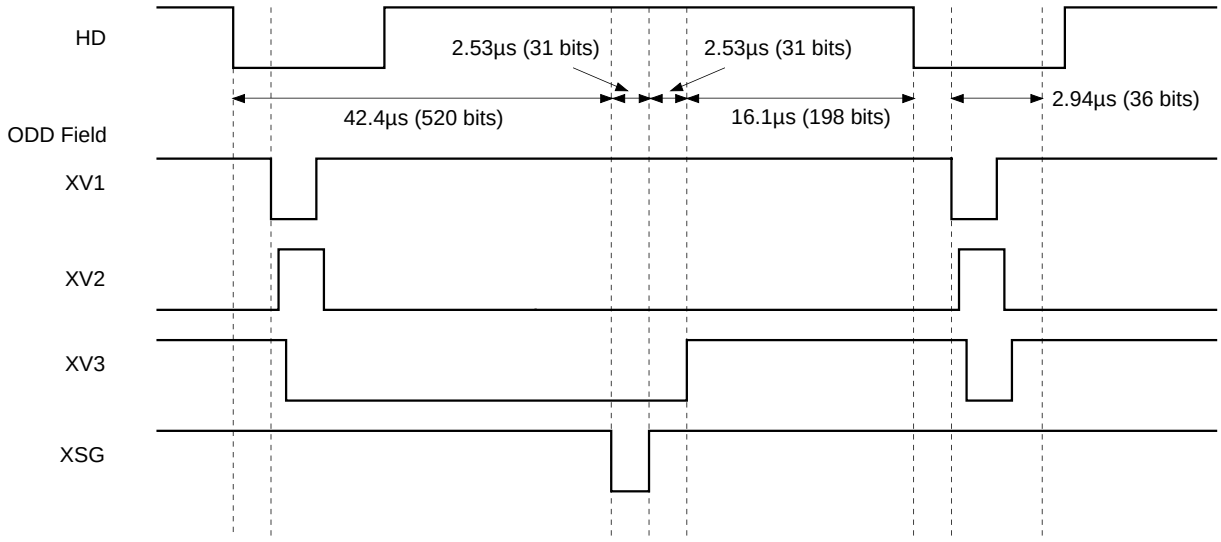
Timing Chart (4) <Horizontal direction> 1/30s non-interlaced readout (RM = Low)



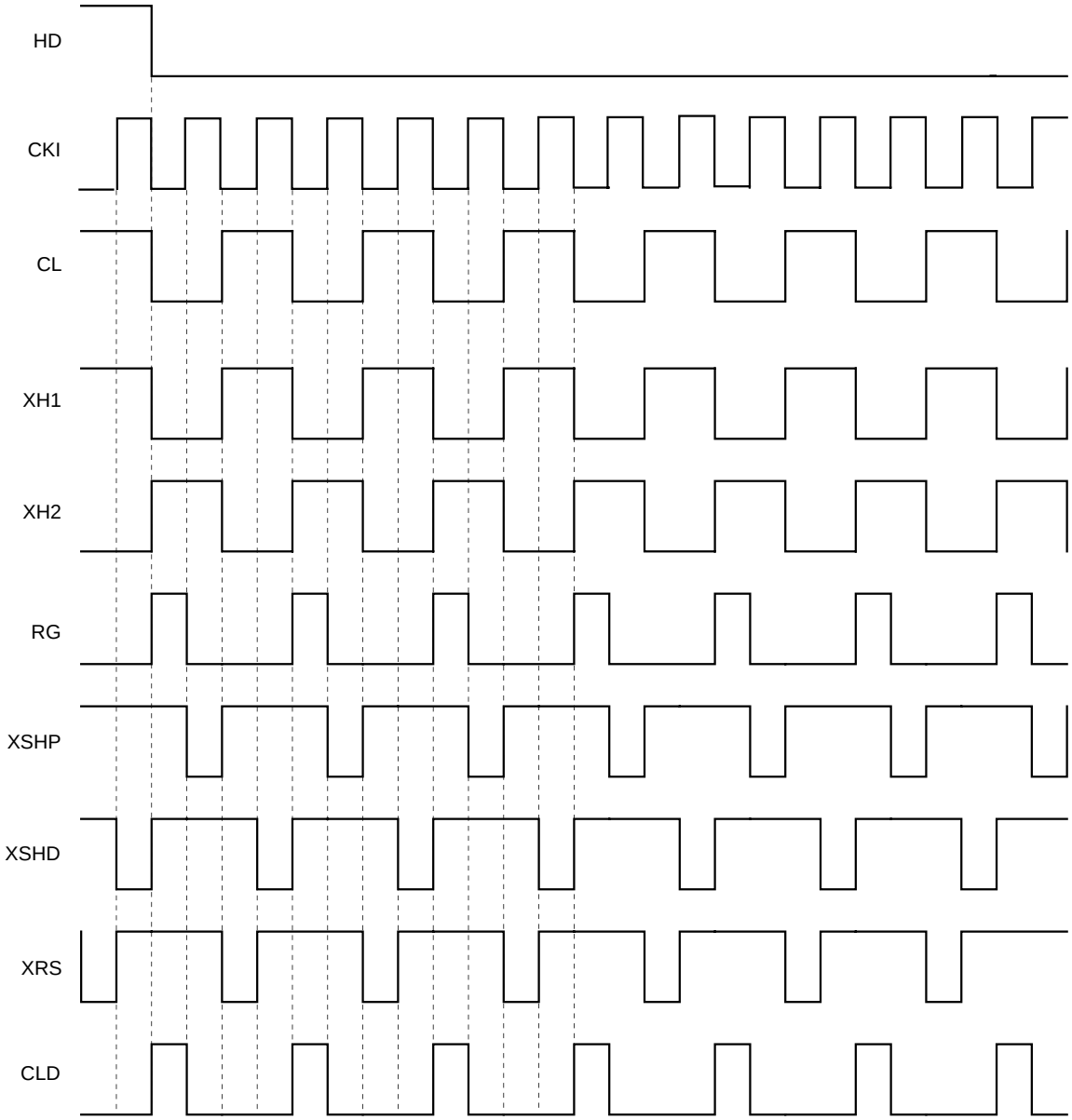
Timing Chart (5) <V2/V3 simultaneous readout timing> 1/60s interlaced (RM = High)



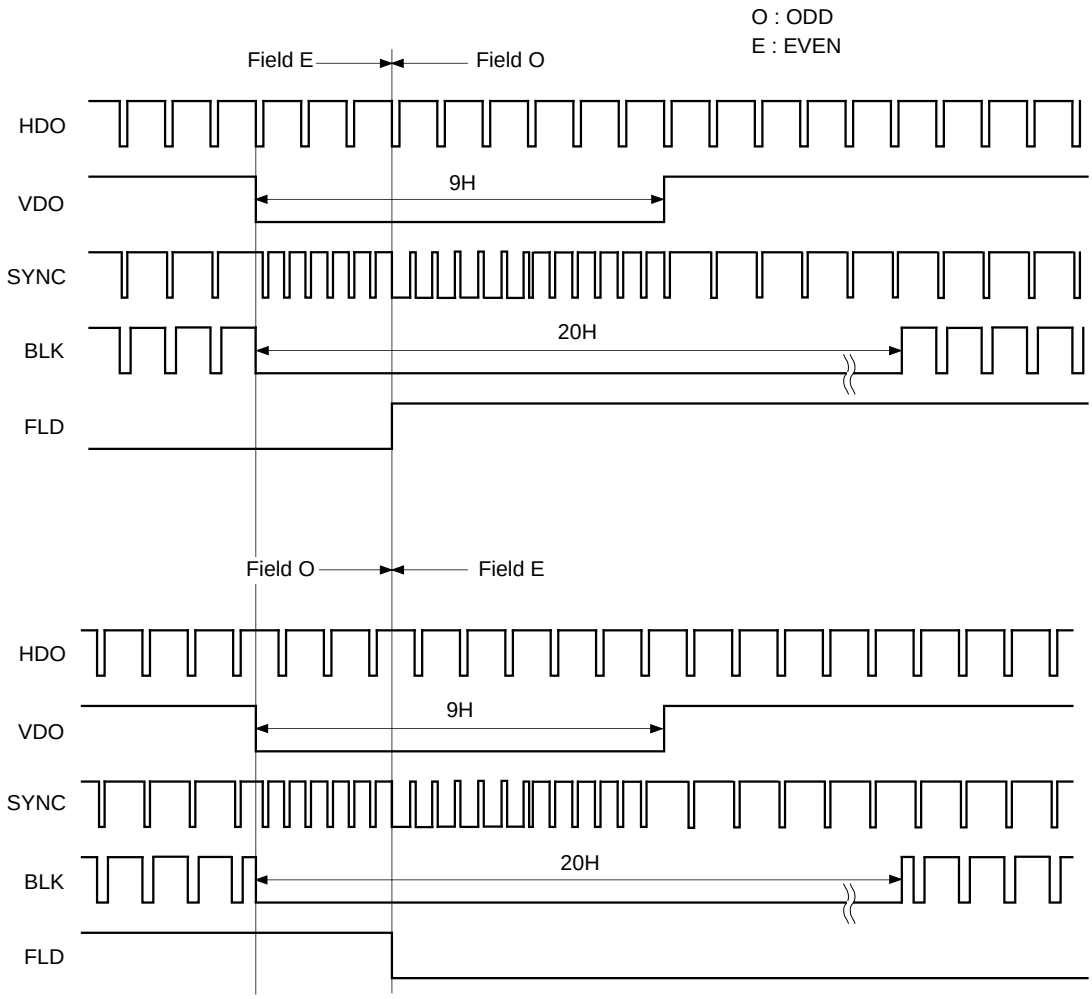
Timing Chart (6) <V2/V3 simultaneous readout timing> 1/30s non-interlaced (RM = Low)



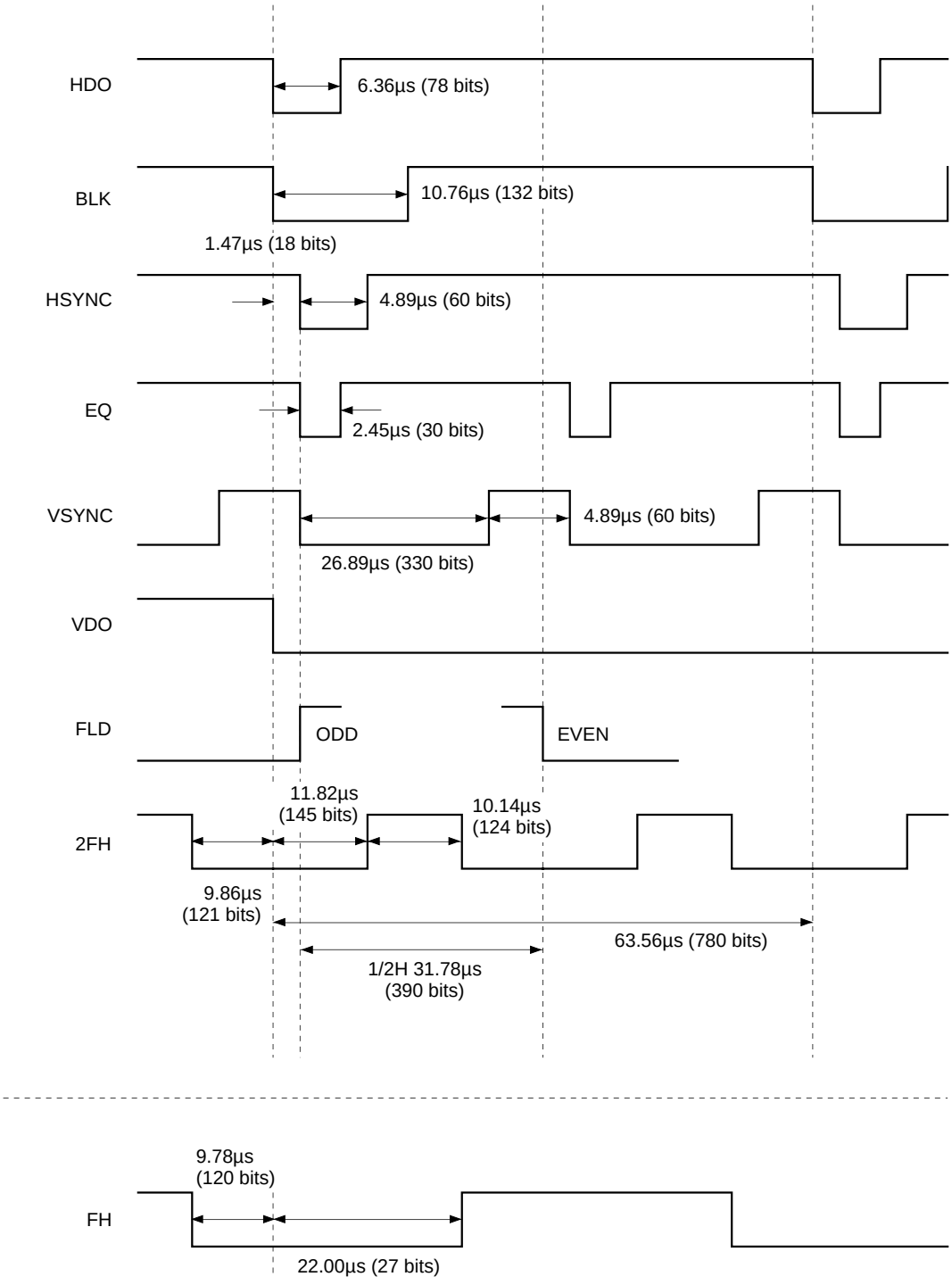
Timing Chart (7) <High-speed phase>



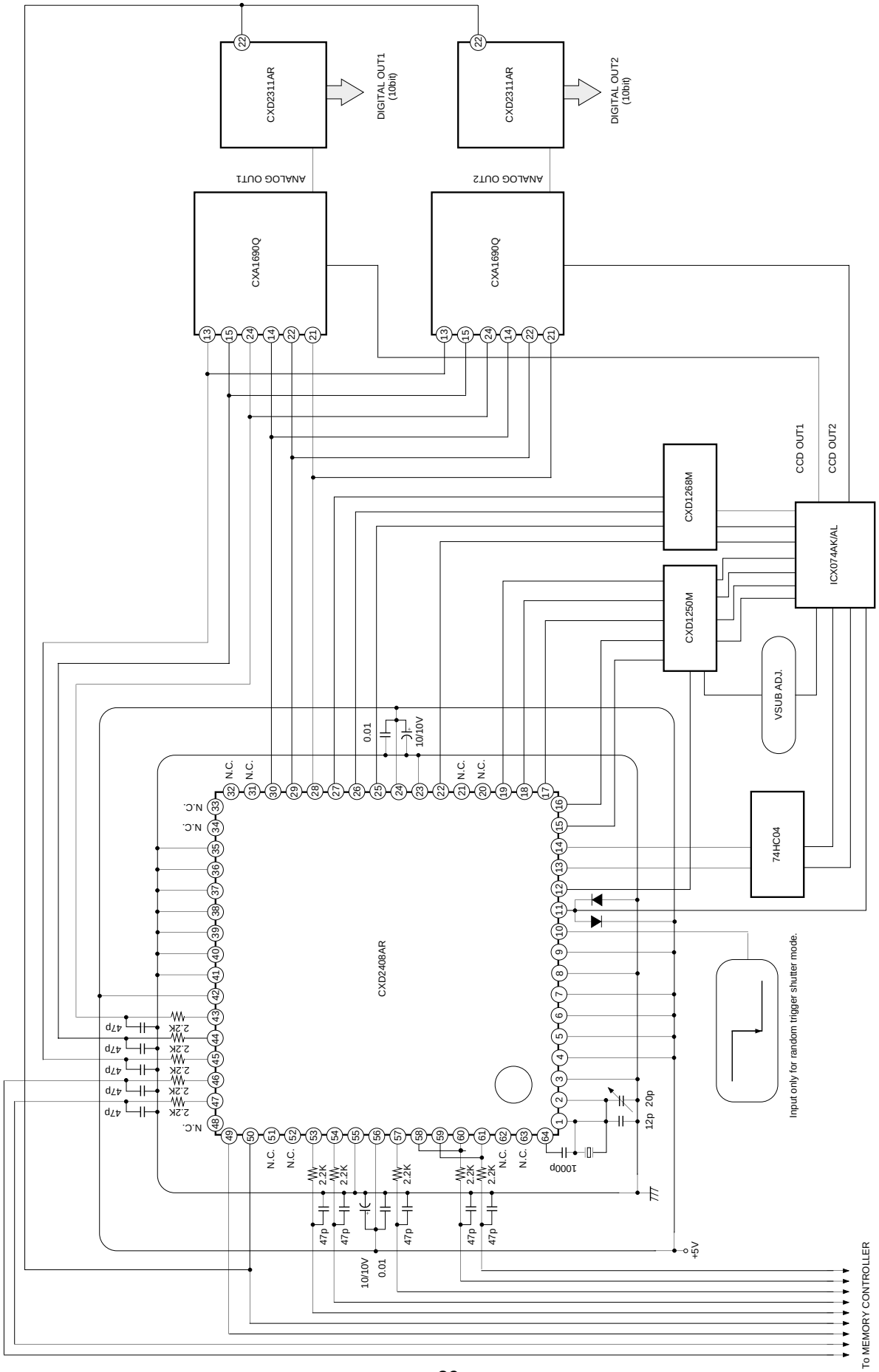
Timing Chart (8) <SG vertical direction>



Timing Chart (9) <SG horizontal direction>



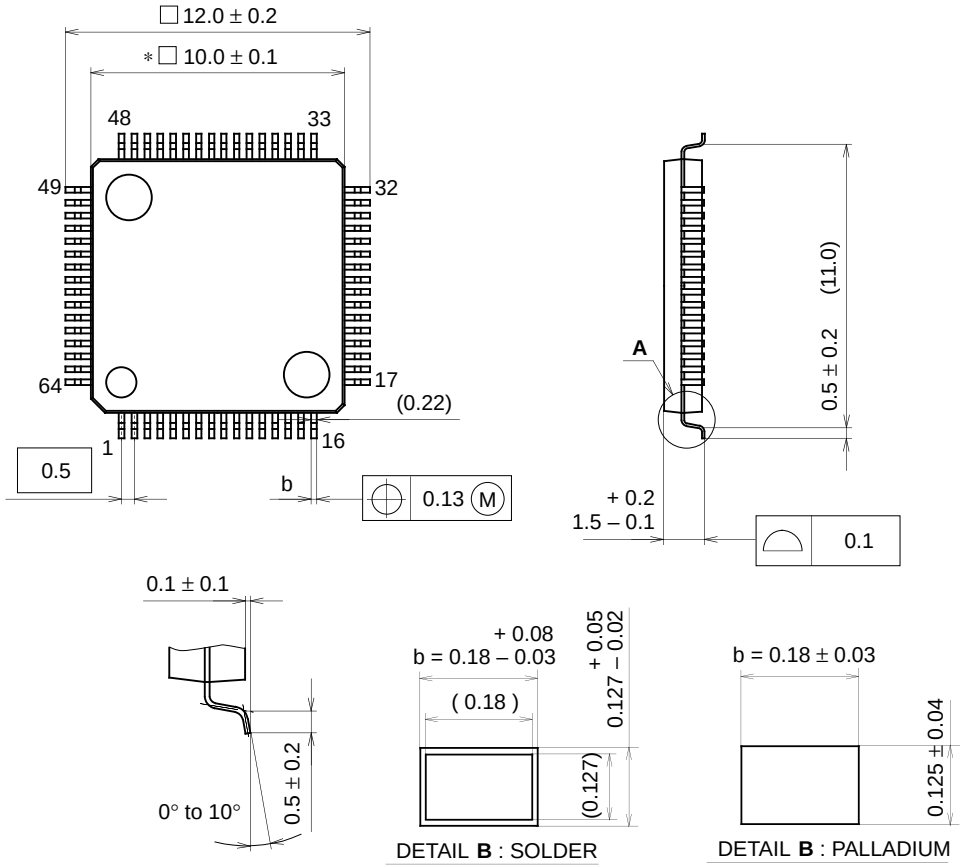
Application Circuit (1/60s interlaced, internal synchronization, normal continuous operation)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g