CMOS 8–Bit Microcontrollers

TMP90CH44N/TMP90CH44F

1. Outline and Characteristics

The TMP90CH44 is a high-speed, high performance 8-bit microcontroller developed for application in the control of various devices.

TMP90CH44, CMOS 8-bit microcontroller, integrates an 8-bit CPU, ROM, RAM, A/D converter, multi-function timer/event counter, general-purpose serial interface and slave functions in a single chip, and with which external program memory and data memory can be extended up to 48KB.

TMP90CH44N is a device with a 64-pin shrink DIP.
TMP90CH44F is a device with a 64-pin flat package.
The following are the features of TMP90CH44:

(1) Highly efficient instructions: 163 types of basic instructions, including
Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions
(2) Minimum instruction executing time: 250ns (at 16MHz oscillation frequency)
(3) Built-in ROM: 16KB
(4) Built-in RAM: 512 bytes
(5) Memory expansion
External program memory: 48KB
External data memory: 48KB
(6) Highly accurate 8-bit A/D converter (4 channels)
(7) General-purpose serial interface (1 channel)
With asynchronous mode and I/O interface mode
(8) Multi-function 16-bit timer/event counter (1 channel)
(9) 8-bit timer (4 channels)
(10) Stepping motor control and pattern generation ports (2 channels)
(11) Input/Output ports: 54 pins
(12) Slave function
(13) Interrupt function: 12 internal, 3 external
(14) Micro Direct Memory Access (DMA) function (4 channels)
(15) Watchdog timer function
(16) Standby function (3 HALT modes)

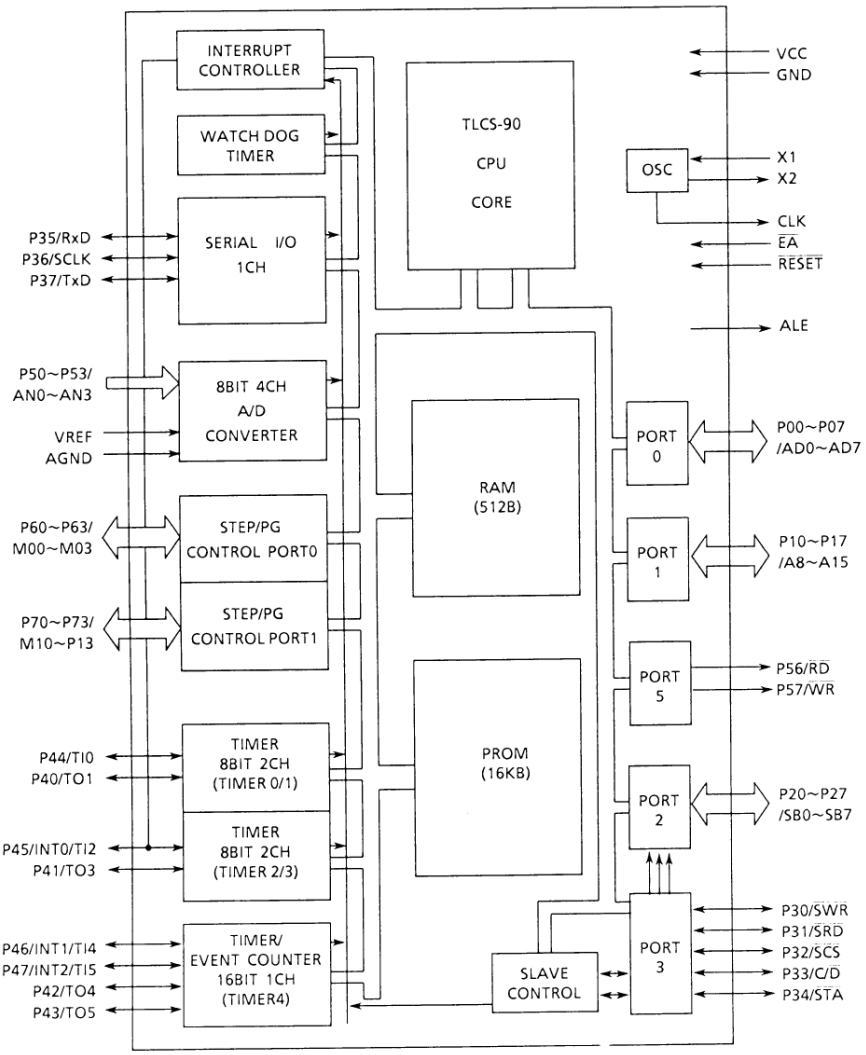


Figure 1. TMP90C844 Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for TMP90C844, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1 (1) shows pin assignment of the TMP90C844N.

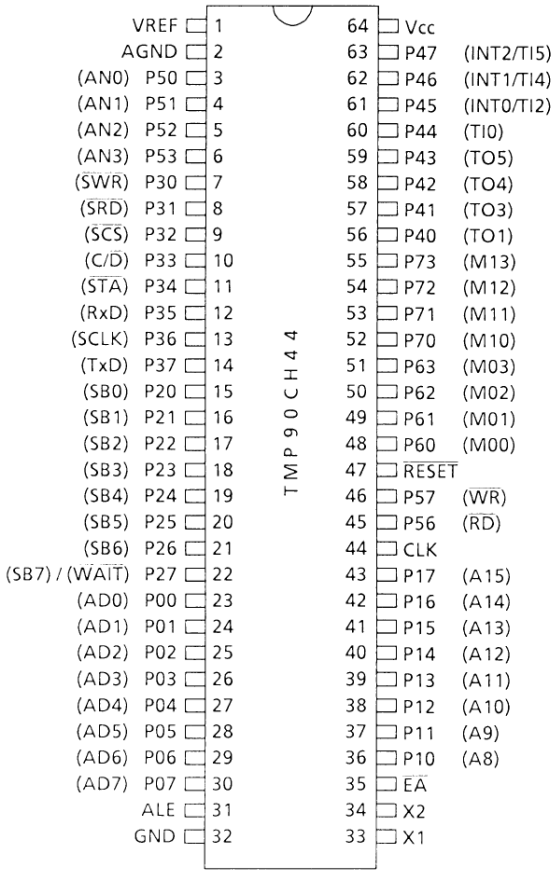


Figure 2.1 (1). Pin Assignment (Shrink DIP)

Figure 2.1 (2) shows the pin assignment of TMP90CH44F.

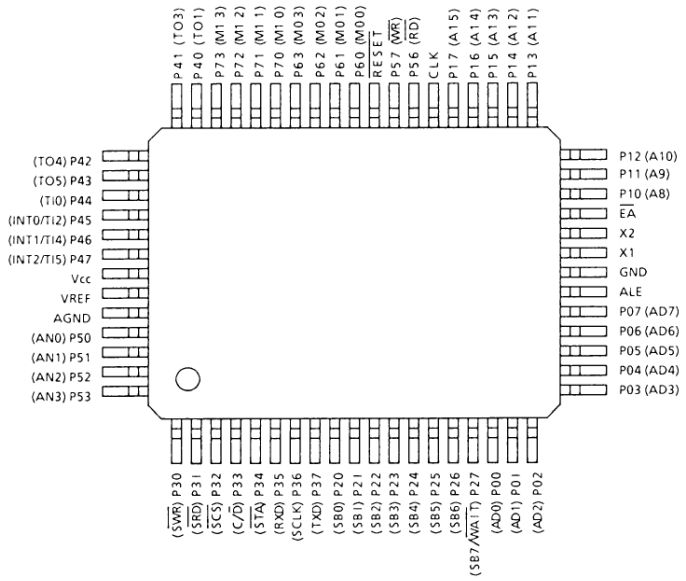


Figure 2.1 (2). Pin Assignment (Flat Package)

2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 (1/2)

Pin Name	No. of pins	I/O or tristate	Function
P00 ~ P07 /AD0 ~ AD7	8	I/O	Port 0: Each bit can be set for input or output
		/Tristate	Address/Data bus: Operates as an 8-bit bidirectional address bus or data bus when using external memory.
P10 ~ P17 /A8 ~ A15	8	I/O	Port 1: An 8-bit I/O port. Each bit can be set for input or output.
		/Output	Address bus: Operates as an address bus (upper 8 bits) when using external memory.
P20 ~ P27	8	I/O	Port 2: Each bit can be set for input or output.
/SB0 ~ SB7	(8)		Address bus: The upper 8 bits address bus for external memory.
/$\overline{\text{WAIT}}$	(1)	/Input	Wait: Input pin for connecting a memory or peripheral LSI with delayed access time.
P30 ~ P37	8	I/O	Port 3: 8-bit I/O port which allows I/O selection on bit basis (with programmable pull-up resistor).
/$\overline{\text{SWR}}$	(1)	/Input	Slave write: The strobe signal input to write data from the master processor.
/$\overline{\text{SRD}}$	(1)	/Input	Slave read: The strobe signal used by the master processor to read data.
/$\overline{\text{SCS}}$	(1)	/Input	Slave chip select: The chip select signal input from the master processor.
C/$\overline{\text{D}}$	(1)	Input	Command/data: The command/data select signal input from the master processor.
/$\overline{\text{STA}}$	(1)	/Output	Status output: Used to report the slave bus status to the master processor.
RxD	(1)	Input	Receiver of serial data
/SCLK	(1)	/I/O	Serial clock
/TxD	(1)	/Output	Transmitter of serial data
P40 ~ P47	8	I/O	Port 4: 8-bit I/O port which allows I/O selection on bit basis (with programmable pull-up resistor).
/TO1, 3, 4, 5	(4)	/Output	Timer outputs 1, 3,4, and 5: Output ports for timer 0, or timer 1, timer 2, timer 3 and timer 4 (2 lines).
/TI0, 2, 4, 5	(4)	/Input	Timer inputs 0, 2, 4, and 5: Input ports for timer 0, or timer 1, timer 2 and timer 4 (2 lines).
/INT0	(1)	/Input	Interrupt request terminal 0: Interrupt request pin 0: Level/rise edge programmable interrupt request pin.
/INT1	(1)	/Input	Interrupt request terminal 1: Interrupt request pin 1: Rise/fall edge programmable interrupt request pin.
/INT2	(1)	/Input	Interrupt request terminal 2: Interrupt request pin 2: Rise edge interrupt request pin.
P50 ~ P53 /AN0 ~ AN3	4	Input	Port 50 ~ 53: 1-bit output ports.
			Analog input: 4 analog inputs to A/D converter.
P56 /$\overline{\text{RD}}$	1	Output	Port 56: A 1-bit output port.
			Read: Strobe signal output for reading external memory.

Table 2.2 (2/2)

Pin name	No. of pins	I/O or tristate	Function
P57 /$\overline{WR}$	1	Output	Port 57: A 1-bit output port. Write: Strobe signal output for writing external memory.
P60 ~ P63 /M00 ~ M03	4	I/O /Output	Port 6: 4 bit I/O port which allows I/O selection on bit basis. Stepping motor control port 0 or pattern generation port 0.
P70 ~ P73 /M10 ~ M13	4	I/O Output	Port 7: 4 bit I/O port which allows I/O selection on bit basis. Stepping motor control port 0 or pattern generation port 1.
ALE	1	Output	Address latch enable
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is pulled up internally during resetting.
$\overline{EA}$	1	Input	External access: Connects with V_{CC} pin in the TMP90C844 built ROM is used.
$\overline{RESET}$	1	Input	Reset: Initializes the TMP90C844. (pull-up resistance is built-in).
X1, X2	2	I/O	Crystal oscillator connection pin
VREF	1	–	Input of reference voltage to A/D converter
AGND	1	–	GND pin for A/D converter
V_{CC}	1	–	Power supply (+5V +/- 10%)
GND	1	–	GND pin (0V)

3. Operation

The following explains the TMP90CH44 functions and basic operations. The CPU functions and internal I/O functions of the TMP90CH44 are the same as the TMP90C844.

Refer to the “TMP90C844” section concerning functions which are not explained in the following.

3.1 CPU

The TMP90CH44 has an internal high performance 8-bit CPU.

Refer to the book TLCS 90 Series CPU Core Architecture section concerning the CPU operation.

3.2 Memory Map

The TMP90CH44 can provide a maximum 48K byte program and data memory.

The program and data memories may be allocated to the address 0000H ~ FFFFH.

(1) Built-in ROM

The TMP90CH44 has an internal 16K-byte ROM. This ROM is located at addresses 0000H ~ 3FFFH. Program execution starts from address 0000H after a reset operation.

Addresses 0008H ~ 0078H in the internal ROM area are used as the interrupt processing entry area.

(2) Built-in RAM

The MP90CH44 contains a 512-byte built-in RAM which is allocated to the addresses FFC0H ~ FFBFH. The CPU can also access some portions of the RAM (192 byte area FF00H ~ FFBFH) using short instruction codes in the direct addressing mode.

Addresses of FF18H ~ FF78H this RAM area can be used as the parameter area for micro DMA processing. (This area can freely be used when the micro DMA function is not used.)

(3) Built-in I/O

The TMP90CH44 uses 56 bytes of the address space as a built-in I/O area. The area is allocated to the addresses FFC0H ~ FFF7H. The CPU can access the built-in I/O using short instruction codes in the direct addressing mode.

Figure 3.2 shows the memory map and the access ranges of the CPU for each addressing mode.

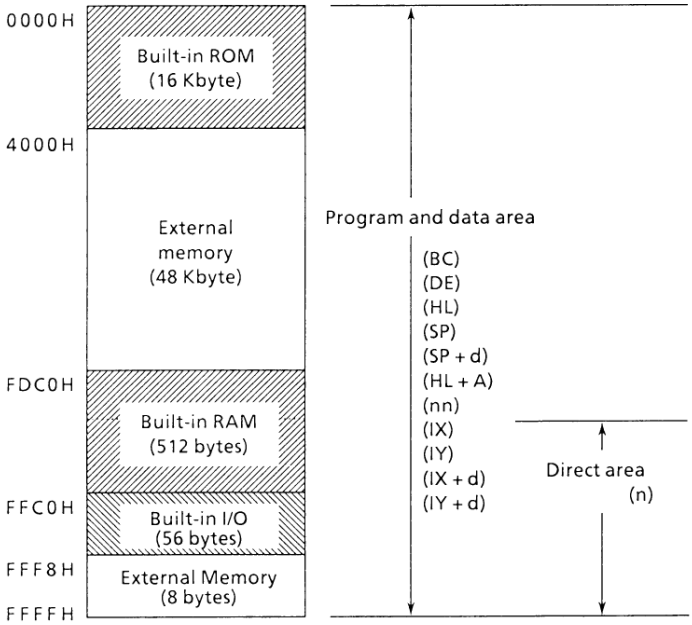


Figure 3.2. Memory Map

4. Electrical Characteristics

TMP90CH44N/TMP90CH44F

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply voltage	-0.5 ~ + 7	V
V_{IN}	Input voltage	-0.5 ~ V_{CC} + 0.5	V
P_D	Power dissipation (Ta = 85°C)	F 500	mW
		N 600	
T_{SOLDER}	Soldering temperature (10s)	260	°C
T_{STG}	Storage temperature	-65 ~ 150	°C
T_{OPR}	Operating temperature	-40 ~ 85	°C

4.2 DC Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C (1 ~ 16MHz)
Typical values are for TA = 25°C and Vcc = 5V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (P0)	-0.3	0.8	V	–
V_{IL1}	P1, P2, P3, P4, P5, P6, P7	-0.3	$0.3V_{CC}$	V	–
V_{IL2}	$\overline{RESET}$, P45 (INTO)	-0.3	$0.25V_{CC}$	V	–
V_{IL3}	$\overline{EA}$	-0.3	0.3	V	–
V_{IL4}	X1	-0.3	$0.2V_{CC}$	V	–
V_{IH}	Input High Voltage (P0)	2.2	V_{CC} + 0.3	V	–
V_{IH1}	P1, P2, P3, P4, P5, P6, P7	$0.7V_{CC}$	V_{CC} + 0.3	V	–
V_{IH2}	$\overline{RESET}$, P45 (INTO)	$0.75V_{CC}$	V_{CC} + 0.3	V	–
V_{IH3}	$\overline{EA}$	V_{CC} - 0.3	V_{CC} + 0.3	V	–
V_{IH4}	X1	$0.8V_{CC}$	V_{CC} + 0.3	V	–
V_{OL}	Output Low Voltage	–	0.45	V	I_{OL} = 1.6mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 $0.75V_{CC}$ $0.9V_{CC}$	–	V V V	I_{OH} = -400μA I_{OH} = -100μA I_{OH} = -20μA
I_{DAR}	Darlington Drive Current (8 I/O pins) (Note)	-0.1	-3.5	mA	V_{EXT} = 1.5V R_{EXT} = 1.1kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ Vin ≤ V_{CC}
I_{LO}	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
I_{CC}	Operating Current (RUN) Idle 1	35 (Typ) 1.5 (Typ)	50 5	mA mA	tosc = 16MHz
	STOP (TA = -20 ~ 70°C) STOP (TA = 0 ~ 50°C)	0.2 (Typ)	40 10	μA μA	0.2 ≤ Vin ≤ V_{CC} - 0.2
V_{STOP}	Power Down Voltage (@STOP)	2.0	6.0	V	V_{IL2} = $0.2V_{CC}$, V_{IH2} = $0.8V_{CC}$
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	KΩ	–
CIO	Pin Capacitance	–	10	pF	testfreq = 1MHz
V_{TH}	Schmitt width $\overline{RESET}$, P45)	0.4	1.0 (Typ)	V	–

4.3 AC Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C (1 ~ 16MHz)

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	Oscillation cycle (= x)	80	1000	80	–	62.5	–	ns
t_{CYC}	CLK Period	4x	4x	320	–	250	–	ns
t_{WH}	CLK High width	2x - 40	–	120	–	85	–	ns
t_{WL}	CLK Low width	2x - 40	–	120	–	85	–	ns
t_{AL}	A0 ~ 7 effective address→ALE fall	0.5x - 15	–	25	–	16	–	ns
t_{LA}	ALE fall →A0 ~ 7 hold	0.5x - 15	–	25	–	16	–	ns
t_{LL}	ALE Pulse width	x - 40	–	40	–	23	–	ns
t_{LC}	ALE fall $\overline{RD}/\overline{WR}$ fall	0.5x - 30	–	10	–	1	–	ns
t_{CL}	$\overline{RD}/\overline{WR}$ →ALE rise	0.5x - 20	–	20	–	11	–	ns
t_{ACL}	A0 ~ 7 effective address →$\overline{RD}/\overline{WR}$ fall	x - 25	–	55	–	38	–	ns
t_{ACH}	Upper effective address →$\overline{RD}/\overline{WR}$ fall	1.5x - 50	–	70	–	44	–	ns
t_{CA}	$\overline{RD}/\overline{WR}$ fall →Upper address hold	0.5x - 20	–	20	–	11	–	ns
t_{ADL}	A0 ~ 7 effective address →Effective data input	–	3.0x - 35	–	205	–	153	ns
t_{ADH}	Upper effective address →Effective data input	–	3.5x - 55	–	225	164	164	ns
t_{RD}	$\overline{RD}$ fall →Effective data input	–	2.0x - 50	–	110	–	75	ns
t_{RR}	$\overline{RD}$ Pulse width	2.0x - 40	–	120	–	85	–	ns
t_{HR}	$\overline{RD}$ rise →Data hold	0	–	0	–	0	–	ns
t_{RAE}	$\overline{RD}$ rise→ Address enable	x - 15	–	65	–	48	–	ns
t_{WW}	$\overline{WR}$ pulse width	2.0x - 40	–	120	–	85	–	ns
t_{DW}	Effective data→$\overline{WR}$ rise	2.0x - 50	–	110	–	75	–	ns
t_{WD}	$\overline{WR}$ rise→Effective data hold	0.5x - 10	–	30	–	21	–	ns
t_{ACKH}	Upper address→CLK fall	2.5x - 50	–	150	–	106	–	ns
t_{ACKL}	Lower address →CLK fall	2.0x - 50	–	110	–	75	–	ns
t_{CKHA}	CLK fall→Upper address hold	1.5x - 80	–	40	–	13	–	ns
t_{CCK}	$\overline{RD}/\overline{WR}$→CLK fall	x - 25	–	55	–	37	–	ns
t_{CKHC}	CLK fall→$\overline{RD}/\overline{WR}$ rise	x - 60	–	20	–	2	–	ns
t_{DCK}	Valid data CLK fall	x - 50	–	30	–	12	–	ns
t_{CWA}	$\overline{RD}/\overline{WR}$ fall→Valid $\overline{WAIT}$	–	x - 40	–	40	–	22	ns
t_{AWAL}	Lower address →Valid $\overline{WAIT}$	–	2.0x - 70	–	90	–	55	ns
t_{WAH}	CLK fall →Valid $\overline{WAIT}$ hold	0	–	0	–	0	–	ns
t_{AWAH}	Upper address →Valid $\overline{WAIT}$	–	2.5x - 70	–	130	–	86	ns
t_{CPW}	CLK fall →Port Data Output	–	x + 200	–	280	–	262	ns
t_{PRC}	Port Data Input →CLK fall	200	–	200	–	200	–	ns
t_{CPR}	CLK fall →Port Data hold	100	–	100	–	100	–	ns

AC Measuring Conditions

- Output level: High 2.2V/Low 0.8V, C_L = 50pF
  (However, CL = 100pF for AD0 ~ 7, A8 ~ 15, ALE, $\overline{RD}$, $\overline{WR}$)
- Input level: High 2.4V/Low 0.45V (AD0 ~ AD7)
  High 0.8V_{CC}/Low 0.2V_{CC} (excluding AD0 ~ AD7)

4.4 A/D Conversion Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Condition	Min	Max	Unit
V_{REF}	Analog reference voltage	Vcc - 1.5	Vcc	Vcc	V
A_{GND}	Analog reference voltage	Vss	Vss	Vss	
V_{AIN}	Analog input voltage range	Vss	–	Vcc	
IREF	Supply current for analog reference voltage	–	0.5	1.0	mA
Error (Quantize error of ±0.5 LSB not included)	Total error (TA = 25°C, Vcc = V_{REF} = 5.0V)	–	–	1.0	LSB
	Total error	–	–	2.5	

4.5 Zero-Cross Characteristics

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Condition	Min	Max	Unit
V_{ZX}	Zero-cross detection input	AC coupling C = 0.1μF	1	1.8	$V_{AC\ P-P}$
A_{ZX}	Zero-cross accuracy	50/60Hz sine wave	–	135	mV
F_{ZX}	Zero-cross detection input frequency	–	0.04	1	kHz

4.6 Timer/ Counter Input Clock (TI0, TI2, and TI4)

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	8x + 100	–	740	–	600	–	ns
t_{VCKL}	Low clock pulse width	4x + 40	–	360	–	290	–	ns
t_{VCKH}	High clock pulse width	4x + 40	–	360	–	290	–	ns

4.7 Interrupt Operation

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	INT0 Low level pulse width 	4x	–	320	–	250	–	ns
t_{INTAH}	INT0 High level pulse width 	4x	–	320	–	250	–	ns
t_{INTBL}	INT1, INT2 Low level pulse width 	8x + 100	–	740	–	600	–	ns
t_{INTBH}	INT1, INT2 High level pulse width 	8x + 100	–	740	–	600	–	ns

4.8 Serial Channel Timing - I/O Interface Mode
(1) SCLK Input Mode

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16x	–	1.28	–	1	–	μs
t_{OSS}	Output Data →rising edge of SCLK	t_{SCY}/2 - 5x - 50	–	190	–	137	–	ns
t_{OHS}	SCLK Rising Edge→output data hold	5x - 100	–	300	–	212	–	ns
t_{HSR}	SCLK Rising Edge→input data hold	0	–	0	–	0	–	ns
t_{SRD}	SCLK Rising Edge→ effective data input	–	t_{SCY} - 5x -5 0	–	780	–	587	ns

(2) SCLK Output Mode

Symbol	Parameter	Variable		12.5MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16x	8192x	1.28	655.4	1	512	μs
t_{OSS}	Output data → SCLK rising edge	t_{SCY} - 2x - 50	–	970	–	725	–	ns
t_{OHS}	SCLK rising edge→output data hold	2x - 80	–	80	–	45	–	ns
t_{HSR}	SCLK rising edge→input data hold	0	–	0	–	0	–	ns
t_{SRD}	SCLK rising edge→ effective data input	–	t_{SCY} - 2x - 150	–	970	–	725	ns

4.9 Slave Bus Interface Timing: $\overline{RD}$, $\overline{WR}$ Bus Mode

V_{CC} = 5V ± 10% TA = -20 ~ 70°C
f = 1 ~ 16MHz

Symbol	Parameter	Min	Max	Unit
T_{SAR}	C/$\overline{D}$ setup →$\overline{SRD}$ fall	20	–	ns
T_{HRA}	$\overline{SRD}$ rise→ $\overline{C}$/D hold	5	–	ns
T_{SCR}	$\overline{SCS}$ setup →$\overline{SRD}$ fall	0	–	ns
T_{HRC}	$\overline{SRD}$ rise →$\overline{SCS}$ hold	0	–	ns
T_{WRD}	$\overline{SRD}$ pulse width	120	–	ns
T_{ARD}	$\overline{SRD}$ fall →effective data output	–	80	ns
T_{VRB}	$\overline{SRD}$ rise →effective data hold	10	85	ns
T_{SAW}	C/$\overline{D}$ setup →$\overline{SWR}$ fall	20	–	ns
T_{HWA}	$\overline{SWR}$ rise →$\overline{C}$/D hold	5	–	ns
T_{SCW}	$\overline{SCR}$ setup →$\overline{SWR}$ fall	0	–	ns
T_{HWC}	$\overline{SWR}$ rise →$\overline{SCS}$ hold	0	–	ns
T_{WWR}	$\overline{SWR}$ pulse width	120	–	ns
T_{SBW}	effective data input →$\overline{SWR}$ rise	80	–	ns
T_{HWB}	SWR rise →effective data hold	10	–	ns

Slave Bus Interface Timing: $\overline{DS}$, R/$\overline{W}$ Bus Mode

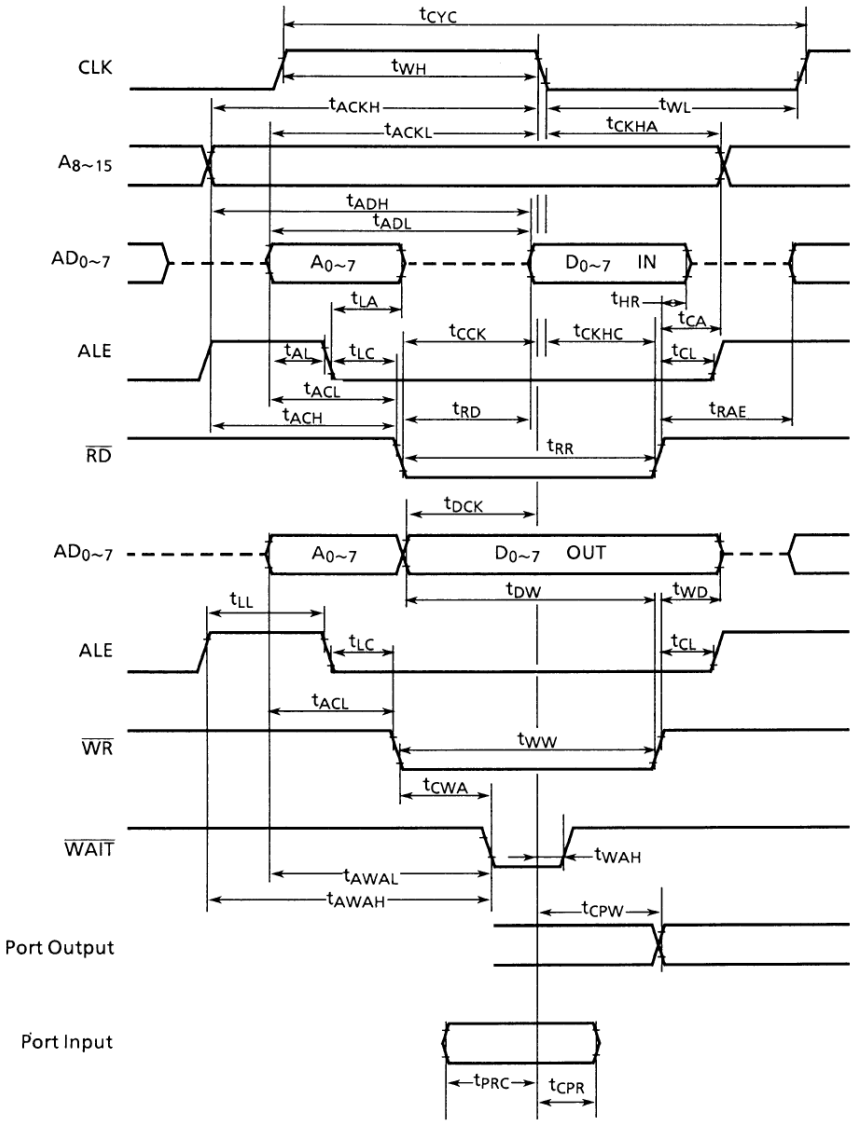
Symbol	Parameter	Min	Max	Unit
T_{SAD}	C/$\overline{D}$ setup →$\overline{DS}$ fall	20	–	ns
T_{HDA}	$\overline{DS}$rise→ C/$\overline{D}$ hold	5	–	ns
T_{SCD}	$\overline{SCS}$ setup →$\overline{DS}$ fall	0	–	ns
T_{HDC}	$\overline{DS}$ rise →$\overline{SCS}$ hold	0	–	ns
T_{SAD}	$\overline{SCS}$ setup →$\overline{DS}$ fall	20	–	ns
T_{HDA}	$\overline{DS}$ rise →R/$\overline{W}$ hold	5	–	ns
T_{WDS}	$\overline{DS}$ pulse width	120	–	ns
T_{ADS}	$\overline{DS}$ fall →effective data output	–	80	ns
T_{VDB}	$\overline{DS}$ rise →effective data hold	10	85	ns
T_{SBD}	Effective data input → $\overline{DS}$ rise	80	–	ns
T_{HDB}	$\overline{DS}$ rise →effective data hold	10	–	ns

$\overline{STA}$ Change Timing

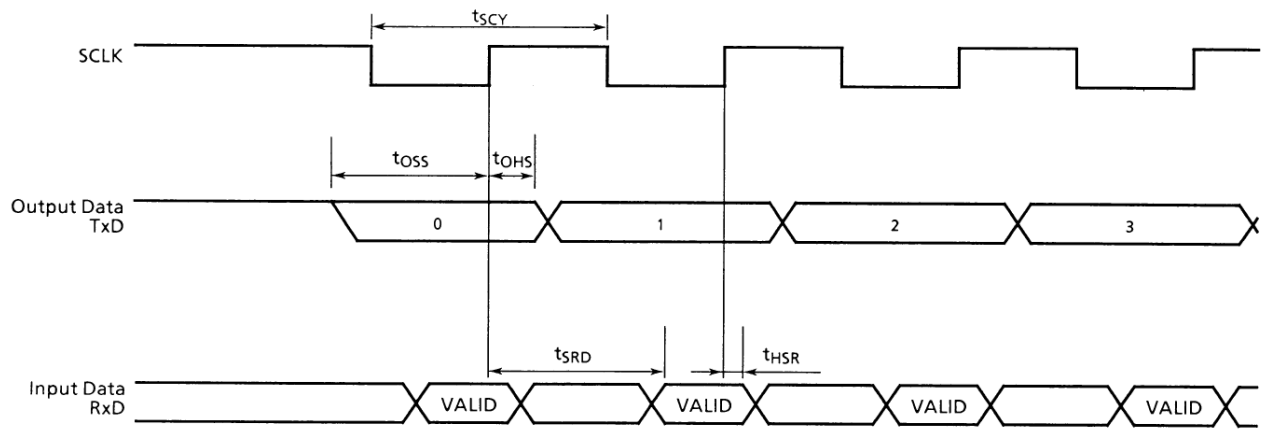
X = 1/fosc

Symbol	Parameter	Variable		16MHz Clock		Unit
		Min	Max	Min	Max	
t_{RPH}	$\overline{STA}$ fall after Output Buffer is read	–	2x + 50	–	175	ns
t_{WPH}	$\overline{STA}$ rise after Input Buffer is written	–	2x + 50	–	175	ns

4.10 Timing Chart

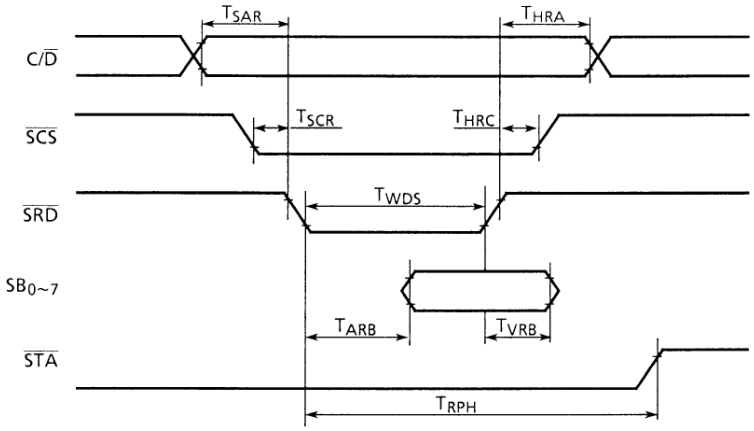


4.11 Timing Chart for I/O Interface Mode

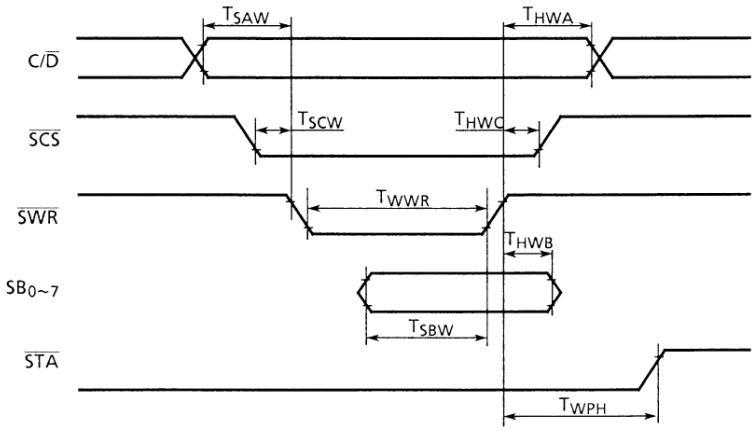


4.12 Timing Chart for Slave Bus Interface: $\overline{RD}$, $\overline{WR}$ Bus Mode

(1) Read Operation

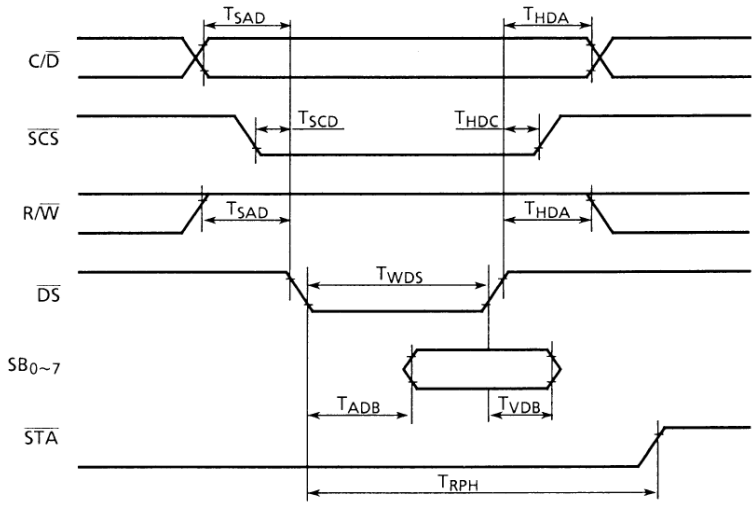


(2) Write Operation



4.13 Timing Chart for Slave Bus Interface: $\overline{DS}$, R/$\overline{W}$ Bus Mode

(1) Read Operation



(2) Write Operation