

25-common x 100-segment BITMAP LCD DRIVER

■ GENERAL DESCRIPTION

The **NJU6673** is a 25-common x 100-segment bit map LCD driver to display graphics or characters.

It contains 2,500 bits display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.

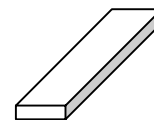
An image data from MPU through the serial or 8-bit parallel interface are stored into the 2,500 bits internal displayed on the LCD panel through the commons and segments drivers.

The **NJU6673** displays 25 x 100 dots graphics or 7-character 2-line by 12 x 13 dots character.

The **NJU6673** contains a built-in OSC circuit for reducing external components. And it features an electrical variable resistor. As result, it reduces the operating current.

The operating voltage from 2.4V to 5.5V and low operating current are suitable for small size battery operation items.

■ PACKAGE OUTLINE



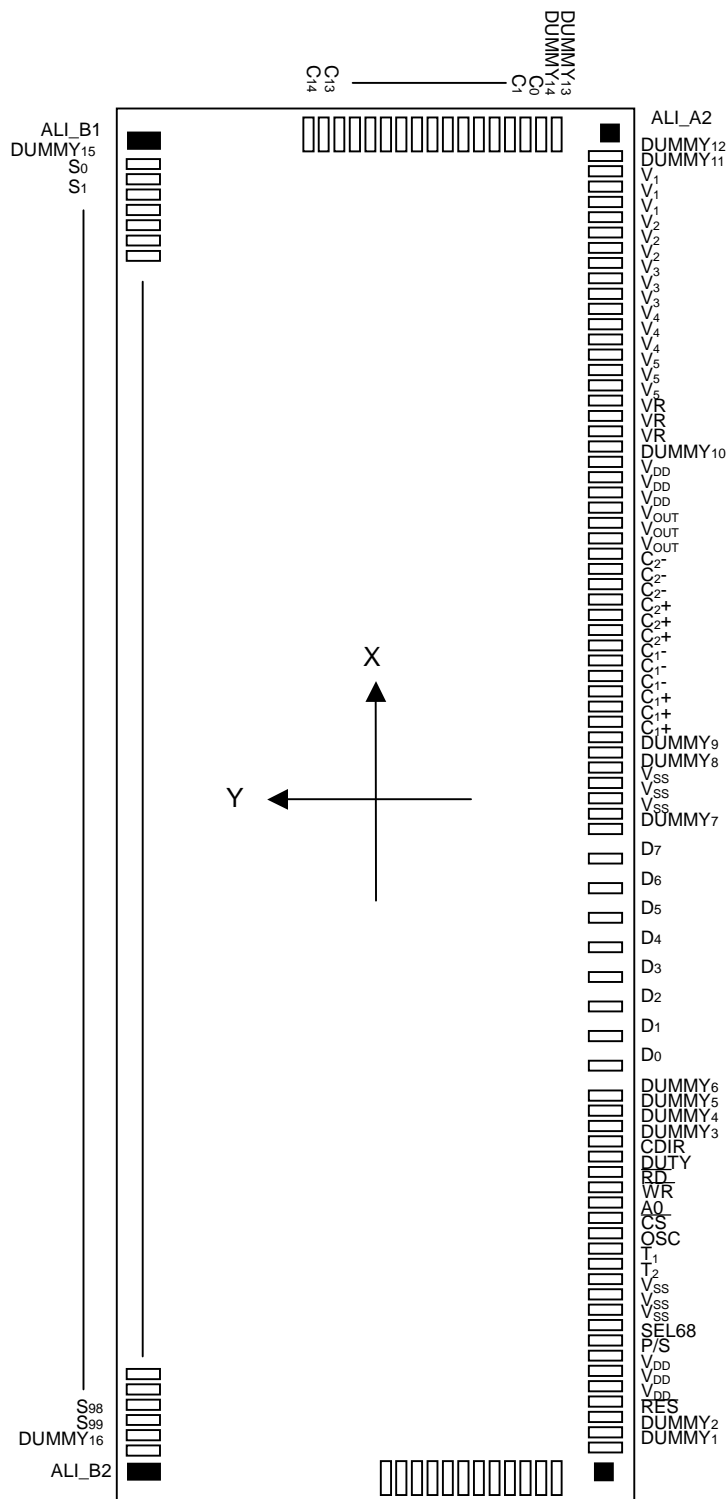
NJU6673CL

■ FEATURES

- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Data RAM 2,500 bits
- LCD Drivers 25-common and 100-segment
- Selectable Duty and Bias Ratio ; 1/25 Duty 1/6 Bias or 1/15 Duty 1/5 Bias
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface (SI, SCL, A0, CS)
- Useful instruction set
Display ON/OFF, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Write Display Data, Read Display Data, Normal or Inverse ON/OFF Set, Static Drive ON/Normal Display, EVR Register Set, Read Modify Write, End, Reset, Internal Power Supply ON/OFF, Driver Output ON/OFF, Power Save and ADC select.
- Power Supply Circuits for LCD;
Available attractive operation for small LCD panel without external capacitors for bias stabilization.
Booster Circuits(3 times maximum, Voltage boosting polarity : Negative (V_{DD} Common)), Regulator, Voltage Follower(x 4)
- Precision Electrical Variable Resistance (16 Steps)
- Low Power Consumption
- Operating Voltage 2.4V to 5.5V
- LCD Driving Voltage 4.0V to 10.0V
- Package Outline Bumped Chip
- C-MOS Technology (Substrate : N)

NJU6673

■ PAD LOCATION



- Chip Center : X=0 μ m, Y=0 μ m
- Chip Size : X=7.54mm, Y=2.09mm
- Chip Thickness : 400 μ m \pm 30 μ m
- Bump Size : 78.16 μ m x 48.10 μ m
- Pad Pitch : 70 μ m(Min.)
- Bump Height : 15 μ m(Typ.)
- Bump Material : Au
- Voltage boosting polarity : Negative Voltage(V_{DD} Common)
- Substrate : N

■ TERMINAL DESCRIPTION

Chip Size 7.54x2.09mm(Chip Center X=0 μ m, Y=0 μ m)

PAD No.	Terminal	X= μ m	Y= μ m
1	DUMMY ₁	-3536	-891
2	DUMMY ₂	-3466	-891
3	RES	-3396	-891
4	V _{DD}	-3326	-891
5	V _{DD}	-3256	-891
6	V _{DD}	-3186	-891
7	P/S	-3116	-891
8	SEL68	-3046	-891
9	V _{SS}	-2976	-891
10	V _{SS}	-2906	-891
11	V _{SS}	-2836	-891
12	T2	-2766	-891
13	T1	-2696	-891
14	OSC ₁	-2626	-891
15	$\overline{\text{CS}}$	-2556	-891
16	A0	-2486	-891
17	$\overline{\text{WR}}$	-2416	-891
18	$\overline{\text{RD}}$	-2346	-891
19	DUTY	-2276	-891
20	CDIR	-2206	-891
21	DUMMY ₃	-2136	-891
22	DUMMY ₄	-2066	-891
23	DUMMY ₅	-1996	-891
24	DUMMY ₆	-1926	-891
25	D ₀	-1715	-891
26	D ₁	-1435	-891
27	D ₂	-1155	-891
28	D ₃	-875	-891
29	D ₄	-595	-891
30	D ₅	-315	-891
31	D ₆ (SCL)	-35	-891
32	D ₇ (SI)	245	-891
33	DUMMY ₇	455	-891
34	V _{SS}	525	-891
35	V _{SS}	595	-891
36	V _{SS}	665	-891
37	DUMMY ₈	735	-891
38	DUMMY ₉	805	-891
39	C1 ⁺	875	-891
40	C1 ⁺	945	-891
41	C1 ⁺	1015	-891
42	C1 ⁻	1085	-891
43	C1 ⁻	1155	-891
44	C1 ⁻	1225	-891
45	C2 ⁺	1295	-891
46	C2 ⁺	1365	-891
47	C2 ⁺	1435	-891
48	C2 ⁻	1505	-891
49	C2 ⁻	1575	-891
50	C2 ⁻	1645	-891

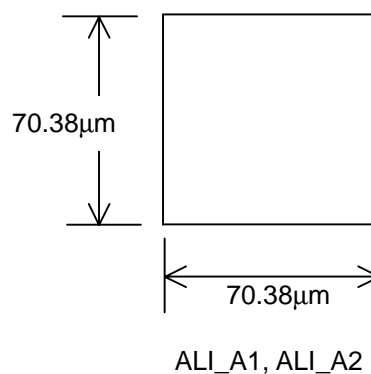
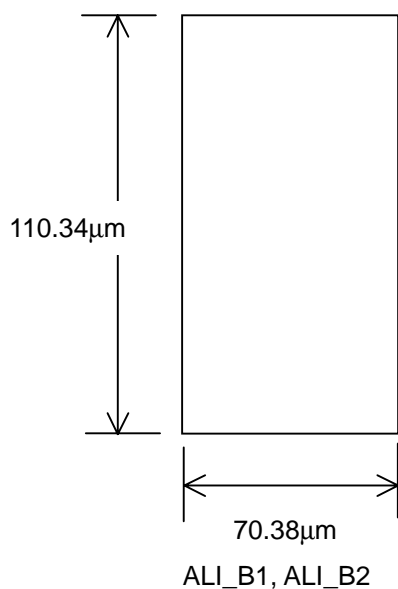
PAD No.	Terminal	X= μ m	Y= μ m
51	V _{OUT}	1715	-891
52	V _{OUT}	1786	-891
53	V _{OUT}	1856	-891
54	V _{DD}	1926	-891
55	V _{DD}	1996	-891
56	V _{DD}	2066	-891
57	DUMMY ₁₀	2136	-891
58	VR	2206	-891
59	VR	2276	-891
60	VR	2346	-891
61	V ₅	2416	-891
62	V ₅	2486	-891
63	V ₅	2556	-891
64	V ₄	2626	-891
65	V ₄	2696	-891
66	V ₄	2766	-891
67	V ₃	2836	-891
68	V ₃	2906	-891
69	V ₃	2976	-891
70	V ₂	3046	-891
71	V ₂	3116	-891
72	V ₂	3186	-891
73	V ₁	3256	-891
74	V ₁	3326	-891
75	V ₁	3396	-891
76	DUMMY ₁₁	3466	-891
77	DUMMY ₁₂	3536	-891
78	ALI_A2	3616	-891
79	DUMMY ₁₃	3616	-745
80	DUMMY ₁₄	3616	-675
81	C ₀	3616	-605
82	C ₁	3616	-535
83	C ₂	3616	-465
84	C ₃	3616	-395
85	C ₄	3616	-325
86	C ₅	3616	-255
87	C ₆	3616	-185
88	C ₇	3616	-115
89	C ₈	3616	-45
90	C ₉	3616	25
91	C ₁₀	3616	95
92	C ₁₁	3616	166
93	C ₁₂	3616	236
94	C ₁₃	3616	306
95	C ₁₄	3616	376
96	ALI_B1	3616	873
97	DUMMY ₁₅	3536	891
98	S ₀	3466	891
99	S ₁	3396	891
100	S ₂	3326	891

PAD No.	Terminal	X= μm	Y= μm
101	S ₃	3256	891
102	S ₄	3186	891
103	S ₅	3116	891
104	S ₆	3046	891
105	S ₇	2976	891
106	S ₈	2906	891
107	S ₉	2836	891
108	S ₁₀	2766	891
109	S ₁₁	2696	891
110	S ₁₂	2626	891
111	S ₁₃	2556	891
112	S ₁₄	2486	891
113	S ₁₅	2416	891
114	S ₁₆	2346	891
115	S ₁₇	2276	891
116	S ₁₈	2206	891
117	S ₁₉	2136	891
118	S ₂₀	2066	891
119	S ₂₁	1996	891
120	S ₂₂	1926	891
121	S ₂₃	1856	891
122	S ₂₄	1786	891
123	S ₂₅	1715	891
124	S ₂₆	1645	891
125	S ₂₇	1575	891
126	S ₂₈	1505	891
127	S ₂₉	1435	891
128	S ₃₀	1365	891
129	S ₃₁	1295	891
130	S ₃₂	1225	891
131	S ₃₃	1155	891
132	S ₃₄	1085	891
133	S ₃₅	1015	891
134	S ₃₆	945	891
135	S ₃₇	875	891
136	S ₃₈	805	891
137	S ₃₉	735	891
138	S ₄₀	665	891
139	S ₄₁	595	891
140	S ₄₂	525	891
141	S ₄₃	455	891
142	S ₄₄	385	891
143	S ₄₅	315	891
144	S ₄₆	245	891
145	S ₄₇	175	891
146	S ₄₈	105	891
147	S ₄₉	35	891
148	S ₅₀	-35	891
149	S ₅₁	-105	891
150	S ₅₂	-175	891

PAD No.	Terminal	X= μm	Y= μm
151	S ₅₃	-245	891
152	S ₅₄	-315	891
153	S ₅₅	-385	891
154	S ₅₆	-455	891
155	S ₅₇	-525	891
156	S ₅₈	-595	891
157	S ₅₉	-665	891
158	S ₆₀	-735	891
159	S ₆₁	-805	891
160	S ₆₂	-875	891
161	S ₆₃	-945	891
162	S ₆₄	-1015	891
163	S ₆₅	-1085	891
164	S ₆₆	-1155	891
165	S ₆₇	-1225	891
166	S ₆₈	-1295	891
167	S ₆₉	-1365	891
168	S ₇₀	-1435	891
169	S ₇₁	-1505	891
170	S ₇₂	-1575	891
171	S ₇₃	-1645	891
172	S ₇₄	-1715	891
173	S ₇₅	-1786	891
174	S ₇₆	-1856	891
175	S ₇₇	-1926	891
176	S ₇₈	-1996	891
177	S ₇₉	-2066	891
178	S ₈₀	-2136	891
179	S ₈₁	-2206	891
180	S ₈₂	-2276	891
181	S ₈₃	-2346	891
182	S ₈₄	-2416	891
183	S ₈₅	-2486	891
184	S ₈₆	-2556	891
185	S ₈₇	-2626	891
186	S ₈₈	-2696	891
187	S ₈₉	-2766	891
188	S ₉₀	-2836	891
189	S ₉₁	-2906	891
190	S ₉₂	-2976	891
191	S ₉₃	-3046	891
192	S ₉₄	-3116	891
193	S ₉₅	-3186	891
194	S ₉₆	-3256	891
195	S ₉₇	-3326	891
196	S ₉₈	-3396	891
197	S ₉₉	-3466	891
198	DUMMY ₁₆	-3536	891
199	ALI_B2	-3616	873
200	C ₂₄	-3616	25

PAD No.	Terminal	X= μm	Y= μm
201	C ₂₃	-3616	-45
202	C ₂₂	-3616	-115
203	C ₂₁	-3616	-185
204	C ₂₀	-3616	-255
205	C ₁₉	-3616	-325
206	C ₁₈	-3616	-395
207	C ₁₇	-3616	-465
208	C ₁₆	-3616	-535
209	C ₁₅	-3616	-605
210	DUMMY ₁₇	-3616	-675
211	DUMMY ₁₈	-3616	-745
212	ALI_A1	-3616	-891

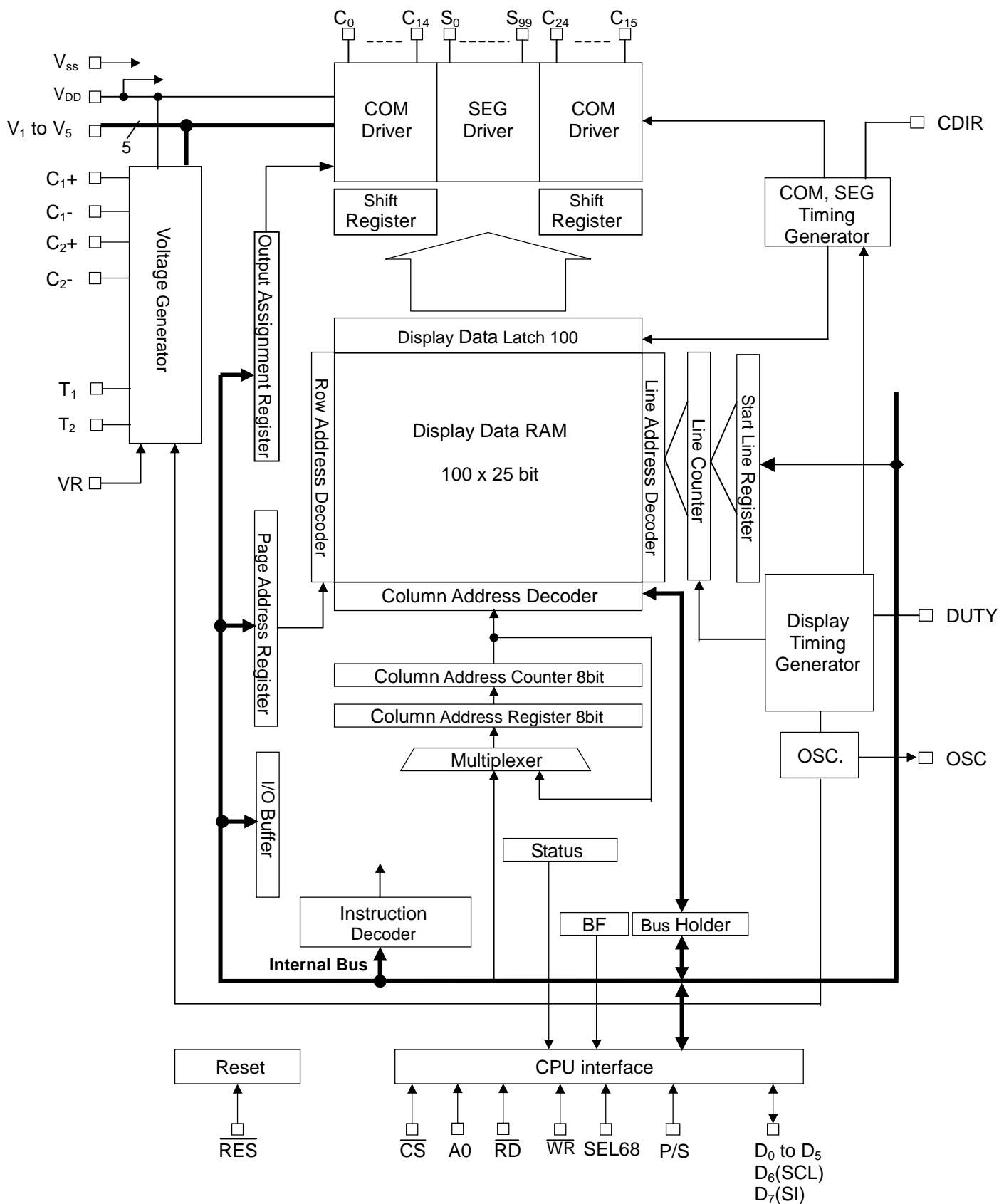
• Alignment marks



Note) Alignment Marks are not contains window.

NJU6673

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function																				
1, 2, 21- 24, 33, 37, 38, 57, 76, 77, 79, 80, 97, 198, 210, 211	DUMMY ₁ DUMMY ₂ DUMMY ₃ - DUMMY ₆ DUMMY ₇ DUMMY ₈ DUMMY ₉ DUMMY ₁₀ DUMMY ₁₁ DUMMY ₁₂ DUMMY ₁₃ DUMMY ₁₄ DUMMY ₁₅ DUMMY ₁₆ DUMMY ₁₇ DUMMY ₁₈		Dummy Terminal. These are open terminals electrically.																				
4,5,6, 54-56	V _{DD}	Power	Power supply terminal. (+2.4 to +5.5V)																				
9-11, 34-36	V _{SS}	GND	Ground terminal. (0V)																				
73-75 70-72 67-69 64-66 61-63	V ₁ V ₂ V ₃ V ₄ V ₅	Power	<p>LCD Driving Voltage Supplying Terminals.</p> <p>In case of external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation.</p> $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq V_{OUT}$ <p>In case of internal power supply, LCD driving voltages V₁ to V₄ depending on the bias selection are supplied as shown in follows;</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>Duty</th> <th>Bias</th> <th>V₁</th> <th>V₂</th> <th>V₃</th> <th>V₄</th> </tr> </thead> <tbody> <tr> <td>1/15 Duty</td> <td>1/5 Bias</td> <td>V₅+4/5 V_{LCD}</td> <td>V₅+3/5 V_{LCD}</td> <td>V₅+2/5 V_{LCD}</td> <td>V₅+1/5 V_{LCD}</td> </tr> <tr> <td>1/25 Duty</td> <td>1/6 Bias</td> <td>V₅+5/6 V_{LCD}</td> <td>V₅+4/6 V_{LCD}</td> <td>V₅+2/6 V_{LCD}</td> <td>V₅+1/6 V_{LCD}</td> </tr> </tbody> </table> <p style="text-align: center;">$V_{LCD} = V_{DD} - V_5$</p>	Duty	Bias	V ₁	V ₂	V ₃	V ₄	1/15 Duty	1/5 Bias	V ₅ +4/5 V _{LCD}	V ₅ +3/5 V _{LCD}	V ₅ +2/5 V _{LCD}	V ₅ +1/5 V _{LCD}	1/25 Duty	1/6 Bias	V ₅ +5/6 V _{LCD}	V ₅ +4/6 V _{LCD}	V ₅ +2/6 V _{LCD}	V ₅ +1/6 V _{LCD}		
Duty	Bias	V ₁	V ₂	V ₃	V ₄																		
1/15 Duty	1/5 Bias	V ₅ +4/5 V _{LCD}	V ₅ +3/5 V _{LCD}	V ₅ +2/5 V _{LCD}	V ₅ +1/5 V _{LCD}																		
1/25 Duty	1/6 Bias	V ₅ +5/6 V _{LCD}	V ₅ +4/6 V _{LCD}	V ₅ +2/6 V _{LCD}	V ₅ +1/6 V _{LCD}																		
39-41 42-44 45-47 48-50	C ₁₊ C ₁₋ C ₂₊ C ₂₋	O	<p>Condenser connecting terminals for internal Voltage Booster.</p> <p>Boosting time is selected by each connected condenser.</p> <p>In case of 3-time boost operation, connect the condenser between C₁₊ and C₁₋, C₂₊ and C₂₋.</p> <p>In case of 2-time boost operation, connect the condenser between C₂₊ and C₂₋, connect C₂₊ to C₁₊, and C₁₋ should be open.</p>																				
51-53	V _{OUT}	O	Boosted voltage output terminal. Connects the capacitor between V _{OUT} terminal and V _{SS} .																				
58-60	VR	I	V _{LCD} voltage adjustment terminal. The gain of V _{LCD} setup circuit for V ₅ level is adjusted by external resistor.																				
13 12	T ₁ , T ₂	I	<p>LCD bias voltage control terminals.</p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>T₁</th> <th>T₂</th> <th>Voltage booster circuit</th> <th>Voltage adjustor</th> <th>V/F circuit</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H/L</td> <td>Available</td> <td>Available</td> <td>Available</td> </tr> <tr> <td>H</td> <td>L</td> <td>Not available</td> <td>Available</td> <td>Available</td> </tr> <tr> <td>H</td> <td>H</td> <td>Not available</td> <td>Not available</td> <td>Available</td> </tr> </tbody> </table>	T ₁	T ₂	Voltage booster circuit	Voltage adjustor	V/F circuit	L	H/L	Available	Available	Available	H	L	Not available	Available	Available	H	H	Not available	Not available	Available
T ₁	T ₂	Voltage booster circuit	Voltage adjustor	V/F circuit																			
L	H/L	Available	Available	Available																			
H	L	Not available	Available	Available																			
H	H	Not available	Not available	Available																			
25 26 27 28 29 30 31 32	D ₀ D ₁ D ₂ D ₃ D ₄ D ₅ D ₆ (SCL) D ₇ (SI)	I/O	<p>Data input / output terminals.</p> <p>In parallel interface Mode (P/S="H") I/O terminals of 8-bit bus.</p> <p>In Serial interface Mode(P/S="L") D₇:Input terminal of serial data (SI). D₆:Input terminal of serial data clock (SCL). D₅ to D₀ terminals are High impedance.</p> <p>When CS="H", D₀ to D₇ terminals are high-impedance.</p>																				

No.	Symbol	I/O	Function																					
16	A0	I	Data discrimination signal input terminal. The signal from MPU discriminates transmitted data between Display data and Instruction. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>A0</td> <td>H</td> <td>L</td> </tr> <tr> <td>Discrimination</td> <td>Display Data</td> <td>Instruction</td> </tr> </table>	A0	H	L	Discrimination	Display Data	Instruction															
A0	H	L																						
Discrimination	Display Data	Instruction																						
3	$\overline{\text{RES}}$	I	Reset terminal. Reset operation is executing during "L" state of $\overline{\text{RES}}$.																					
15	$\overline{\text{CS}}$	I	Chip select signal input terminal. Data Input/Output are available during $\overline{\text{CS}} = "L"$.																					
18	$\overline{\text{RD}}$ (E)	I	$\overline{\text{RD}}$ (80 type) or E(68 type) signal input terminal. <In 80 type MPU mode>(SEL68="L") RD signal from 80 type MPU input terminal. Active "L". D ₀ to D ₇ terminals are output during "L" level. <In 68 type MPU mode>(SEL68="H") Enable signal from 68 type MPU input terminal. Active "H"																					
17	$\overline{\text{WR}}$ (R/W)	I	$\overline{\text{WR}}$ (80 type) or $\overline{\text{R/W}}$ (68 type) signal input terminal. <In 80 Type MPU mode>(SEL68="L") $\overline{\text{WR}}$ signal from 80 type MPU input . Active "L". The data transmitted during $\overline{\text{WR}} = "L"$ are fetched at the rising edge of $\overline{\text{WR}}$. <In 68 Type MPU mode> R/w signal from 68 type MPU input terminal. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>$\overline{\text{R/W}}$</td> <td>H</td> <td>L</td> </tr> <tr> <td>State</td> <td>Read</td> <td>Write</td> </tr> </table>	$\overline{\text{R/W}}$	H	L	State	Read	Write															
$\overline{\text{R/W}}$	H	L																						
State	Read	Write																						
8	SEL68	I	MPU interface type selection terminal. This terminal must connect to V _{DD} or V _{SS} <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>SEL68</td> <td>H</td> <td>L</td> </tr> <tr> <td>State</td> <td>68 type</td> <td>80 type</td> </tr> </table>	SEL68	H	L	State	68 type	80 type															
SEL68	H	L																						
State	68 type	80 type																						
7	P/S	I	Parallel or Serial interface selection signal input terminal. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>P/S</th> <th>Inter face</th> <th>Chip Select</th> <th>Data /Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial CLK</th> </tr> <tr> <td>"H"</td> <td>Parallel</td> <td>$\overline{\text{CS}}$</td> <td>A0</td> <td>D₀-D₇</td> <td>$\overline{\text{RD}}$, $\overline{\text{WR}}$</td> <td>-</td> </tr> <tr> <td>"L"</td> <td>Serial</td> <td>$\overline{\text{CS}}$</td> <td>A0</td> <td>SI(D₇)</td> <td>-</td> <td>SCL(D₆)</td> </tr> </table> In case of the serial interface (P/S="L") RAM data and status read operation do not work in mode of the serial interface. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ terminals must fix to "H" or "L". D ₀ to D ₅ terminals are high impedance.	P/S	Inter face	Chip Select	Data /Command	Data	Read/Write	Serial CLK	"H"	Parallel	$\overline{\text{CS}}$	A0	D ₀ -D ₇	$\overline{\text{RD}}$, $\overline{\text{WR}}$	-	"L"	Serial	$\overline{\text{CS}}$	A0	SI(D ₇)	-	SCL(D ₆)
P/S	Inter face	Chip Select	Data /Command	Data	Read/Write	Serial CLK																		
"H"	Parallel	$\overline{\text{CS}}$	A0	D ₀ -D ₇	$\overline{\text{RD}}$, $\overline{\text{WR}}$	-																		
"L"	Serial	$\overline{\text{CS}}$	A0	SI(D ₇)	-	SCL(D ₆)																		
14	OSC	O	Maker Testing Clock output terminal. The terminal is recommended to open.																					

No.	Symbol	I/O	Function																				
81-95	C ₀ -C ₁₄	O	<p>LCD driving signal output terminals.</p> <ul style="list-style-type: none"> ● Common output terminals :C₀ to C₂₄ ● Segment output terminals :S₀ to S₉₉ <p>• Common Output Terminal Following output voltages is selected by the combination of alternating(FR) signal and Common scanning data.</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Scan data</th> <th>FR</th> <th>Output Voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V₅</td> </tr> <tr> <td>L</td> <td>V_{DD}</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₁</td> </tr> <tr> <td>L</td> <td>V₄</td> </tr> </tbody> </table>	Scan data	FR	Output Voltage	H	H	V ₅	L	V _{DD}	L	H	V ₁	L	V ₄							
Scan data	FR	Output Voltage																					
H	H	V ₅																					
	L	V _{DD}																					
L	H	V ₁																					
	L	V ₄																					
98-197	S ₀ -S ₉₉	O	<p>• Segment output terminal Following output voltages is selected by the combination of alternating(FR) signal and display data in the DD RAM.</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2">RAM data</th> <th rowspan="2">FR</th> <th colspan="2">Output Voltage</th> </tr> <tr> <th>Normal</th> <th>Reverse</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V_{DD}</td> <td>V₂</td> </tr> <tr> <td>L</td> <td>V₅</td> <td>V₃</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₂</td> <td>V_{DD}</td> </tr> <tr> <td>L</td> <td>V₃</td> <td>V₅</td> </tr> </tbody> </table>	RAM data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅
RAM data	FR	Output Voltage																					
		Normal	Reverse																				
H	H	V _{DD}	V ₂																				
	L	V ₅	V ₃																				
L	H	V ₂	V _{DD}																				
	L	V ₃	V ₅																				
200-209	C ₂₄ -C ₁₅	O	<table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th rowspan="2">RAM data</th> <th rowspan="2">FR</th> <th colspan="2">Output Voltage</th> </tr> <tr> <th>Normal</th> <th>Reverse</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td>H</td> <td>V_{DD}</td> <td>V₂</td> </tr> <tr> <td>L</td> <td>V₅</td> <td>V₃</td> </tr> <tr> <td rowspan="2">L</td> <td>H</td> <td>V₂</td> <td>V_{DD}</td> </tr> <tr> <td>L</td> <td>V₃</td> <td>V₅</td> </tr> </tbody> </table>	RAM data	FR	Output Voltage		Normal	Reverse	H	H	V _{DD}	V ₂	L	V ₅	V ₃	L	H	V ₂	V _{DD}	L	V ₃	V ₅
RAM data	FR	Output Voltage																					
		Normal	Reverse																				
H	H	V _{DD}	V ₂																				
	L	V ₅	V ₃																				
L	H	V ₂	V _{DD}																				
	L	V ₃	V ₅																				
19	DUTY	I	<p>Duty and Bias selection terminal.</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>DUTY</th> <th>Duty</th> <th>Bias</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>1/15</td> <td>1/5</td> </tr> <tr> <td>L</td> <td>1/25</td> <td>1/6</td> </tr> </tbody> </table>	DUTY	Duty	Bias	H	1/15	1/5	L	1/25	1/6											
DUTY	Duty	Bias																					
H	1/15	1/5																					
L	1/25	1/6																					
20	CDIR	I	<p>Common Driver Assignment selection terminal.</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>CDIR</th> <th>Common Output terminals</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Reverse (C₂₄→C₀)</td> </tr> <tr> <td>L</td> <td>Normal (C₀→C₂₄)</td> </tr> </tbody> </table>	CDIR	Common Output terminals	H	Reverse (C ₂₄ →C ₀)	L	Normal (C ₀ →C ₂₄)														
CDIR	Common Output terminals																						
H	Reverse (C ₂₄ →C ₀)																						
L	Normal (C ₀ →C ₂₄)																						

FUNCTIONAL DESCRIPTION

(1) Description for each blocks

(1-1) Busy Flag (BF)

The Busy Flag (BF) is set to logical "1" in busy of internal execution by an instruction, and any instruction excepting for the "Status Read" is disable at this time. Busy Flag is outputted through D₇ terminal by "Status Read" instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in ■ BUS TIMING CHARACTERISTICS is secured completely.

(1-2) Display Start Line Register

The Display Start Line Register is a register to set a display data RAM address corresponding to the COM₀ display line (the top line normally) for the vertical scroll on the LCD, Page address change and so forth. The Display Start Line Address set instruction sets the 8-bit display start address into this register.

(1-3) Line Counter

Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6673**.

(1-4) Column Address Counter

Column Address Counter is the 8-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Fig. 1. The counter is incremented automatically after the display data read/write instructions execution. When the Column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Page Address Register.

By the address inverse instruction (ADC select) as shown in Fig. 1, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Page Address Register

Page Address Register assigns the page address of the display data RAM as shown in Fig. 1. In case of accessing from the MPU with changing the page address, Page Address Set instruction is required.

(1-6) Display Data RAM

The Display data RAM (DD RAM) is the bit map RAM consisting of 2,500 bits to store the display data corresponding to the LCD pixel on LCD panel.

In Normal Display : "1" Turn-On Display, "0"=Turn-Off Display

In Reverses Display: "1" Turn-Off Display, "0"=Turn-On Display

DD RAM output 100 bits parallel data addressed by line address counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the MPU and latch to the display data latch operation are done independently.

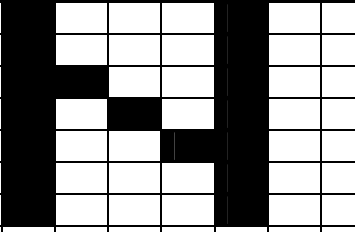
(1-7) Common Driver Assignment

The scanning order can be assigned by set Common Driver Assignment selection terminal as shown on Table 1.

Table 1 Common Driver Order Assignment

		COM Outputs Terminals			
PAD No.	81	95		200	209
Pin name	C ₀	C ₁₄		C ₂₄	C ₁₅
COM Driver Assignment selection terminal	"L"	COM ₀ →	COM ₁₄	COM ₂₄ ←	COM ₁₅
	"H"	COM ₂₄ ←	COM ₁₀	COM ₀ →	COM ₉

The duty ratio setting and output assignment register are so controlled to operate independently that duty ratio setting required to corresponding duty ratio for output assignment.

Page Address	Data	Display Pattern	Line Address														
D ₁ , D ₀ (0, 0)	D ₀		Page 0	00	COM output example 1												
	D ₁			01													
	D ₂			02													
	D ₃			03													
	D ₄			04													
	D ₅			05													
	D ₆			06													
	D ₇			07													
D ₁ , D ₀ (0, 1)	D ₀	Page 1	08	COM output example 2													
	D ₁		09														
	D ₂		0A														
	D ₃		0B														
	D ₄		0C														
	D ₅		0D														
	D ₆		0E														
	D ₇		0F														
D ₁ , D ₀ (1, 0)	D ₀	Page 2	10	C ₀													
	D ₁		11		C ₁												
	D ₂		12			C ₂											
	D ₃		13				C ₃										
	D ₄		14					C ₄									
	D ₅		15						C ₅								
	D ₆		16							C ₆							
	D ₇		17								C ₇						
D ₁ , D ₀ (1, 1)	D ₀	Page 3	18	C ₈													
Column		D ₀ =0	00		01							02	03	04	05	62
Address(ADC)		D ₀ =1	63		62	61						60	5F	5E	01	00
Segment output		S ₀	S ₁		S ₂	S ₃	S ₄					S ₅	S ₉₈	S ₉₉		

COM output example1 : 1/25Duty, set Display Start Line 08_H

COM output example2 : 1/15Duty, set Display Start Line 08_H

Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit

Reset circuit operates the following initializations when the condition of $\overline{\text{RES}}$ terminal goes to "L" level.

• Initialization

1. Display Off
2. Normal Display (Non-inverse display)
3. ADC Select : Normal (ADC Instruction $D_0="0"$)
4. Read Modify Write Mode Off
5. Voltage Booster off, Voltage Regulator off, Voltage follower off
6. Clear the serial interface register
7. Driver Output Off
8. Set the Display Start Line Register to 00_H
9. Set the Column Address Counter to 00_H
10. Set the Page Address Register to page "0"
11. Set the EVR register to 00_H

The $\overline{\text{RES}}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in "the MPU interface" in the Application Circuit section. The "L" level input signal as reset signal must keep the period over than $10\mu\text{s}$ as shown in DC Characteristics. The **NJU6673** takes $1\mu\text{s}$ for the reset operation after the rising edge of the $\overline{\text{RES}}$ signal.

The reset operation by $\text{RES}="L"$ initializes each register setting as above reset status, but the internal oscillation circuit and output terminals (D_0 to D_7) are not affected.

To avoid the lock-up, the reset operation by the $\overline{\text{RES}}$ terminal must be required every time when power turns on. The reset operation by the reset instruction, function 8 to 11 operations mentioned above is performed.

The $\overline{\text{RES}}$ terminal must be keep "L" level when the power turns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving

(a) LCD Driving Circuits

LCD driver is 125 sets of multiplexer consisting of 100 segments and 25 commons drivers to output LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in ■ LCD DRIVING WAVEFORM.

(b) Display Data Latch Circuits

Display Data Latch Circuit latches the 100 bits display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display, Display On/Off, Static drive On/Off instruction processes only stored data in this Display Data Latch Circuit.

(c) Line Counter and Latch signal of Latch Circuits

The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 100 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to LCD driving circuits.

The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(d) Display Timing Generator Circuit

The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

(e) Common Timing Generation

The Common Timing Generator generates the common timing signal from the display clock (CL).

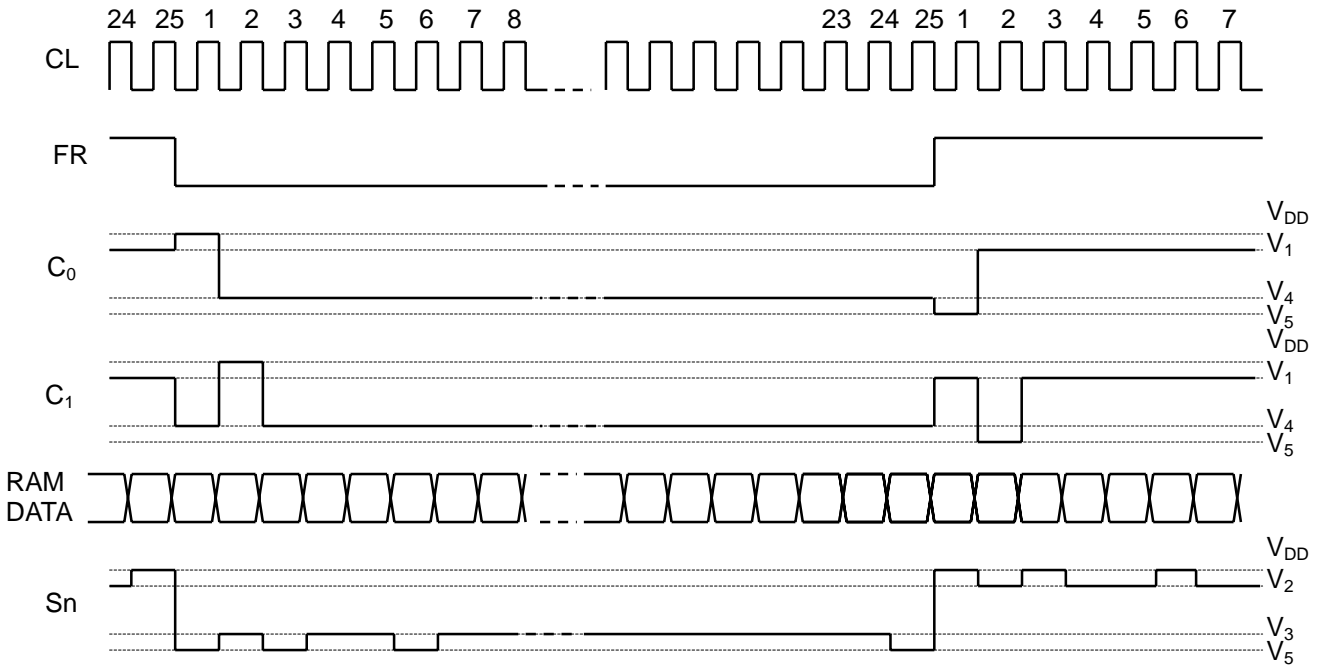


Fig. 2

(f) Oscillation Circuit

The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

Table 2 The relation between duty and divide

Duty	1/15	1/25
Divide	1/10	1/6

(g) Power Supply Circuit

The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (3-Time maximum), voltage regulator circuits, and voltage followers.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1 , V_2 , V_3 , V_4 , V_5 and V_{OUT} for the LCD should be supplied from outside, terminals C_{1+} , C_{1-} , C_{2+} , C_{2-} and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminals. Furthermore the external power supply operates with some of internal power supply function.

Table3 The Relation Between Power Supply Circuit And T_1 , T_2 Terminal

T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Power Supply	C_{1+} , C_{1-} , C_{2+} , C_{2-}	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5 , V_{OUT}	Open	Open

When (T_1 , T_2)=(H, L), C_{1+} , C_{1-} , C_{2+} , C_{2-} terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

When (T_1 , T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

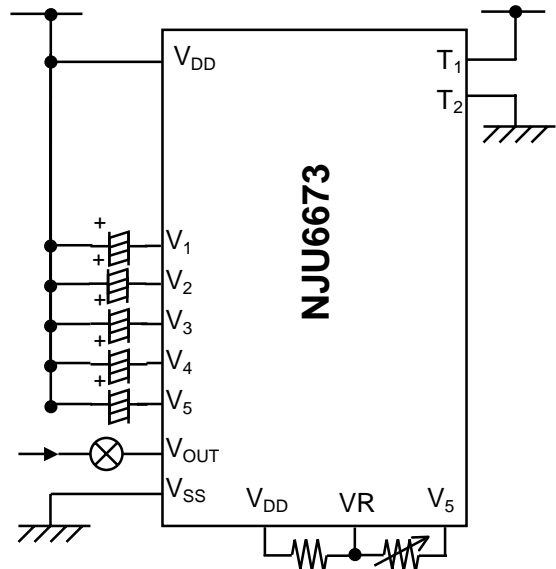
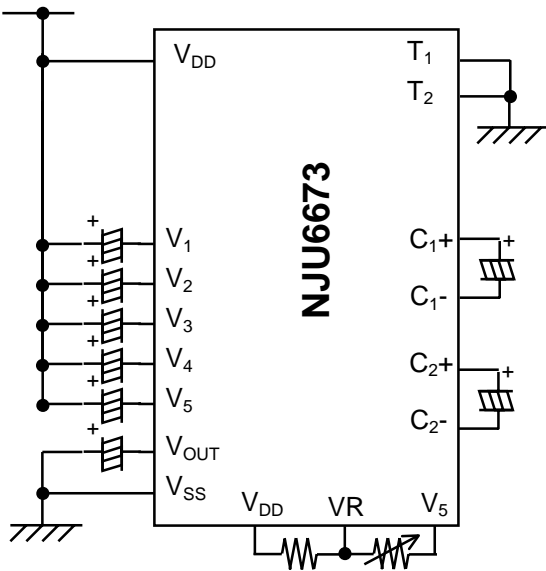
The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6673** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition.

The external capacitors to V_1 to V_5 for Bias voltage stabilization may be removed in use of small size LCD panel. The equivalent load of LCD panel may be changed depending on display patterns. Therefore, it require display quality check on various display patterns actually without external capacitors. If the display quality is not so good, external capacitors should connects as show in (3-4)LCD Driving Voltage Generation Circuits -Fig. 4. (If no need external capacitors as result of experiment, the application patterns (wiring) should be prepared for recovery.)

○ Power Supply applications

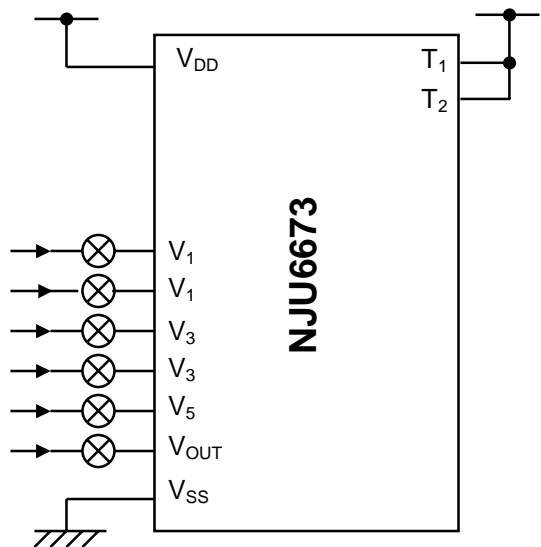
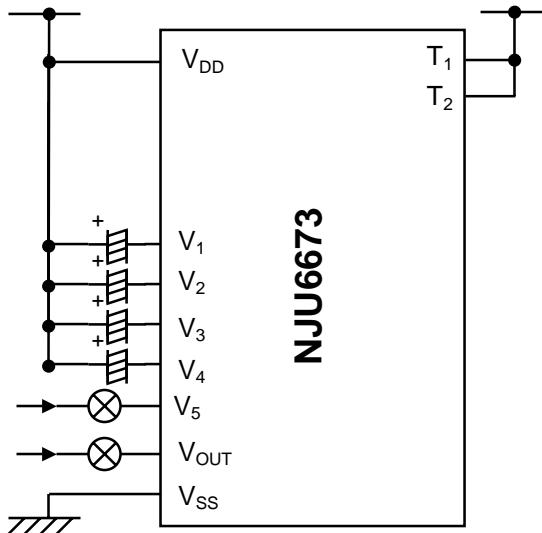
- (1) Internal power supply example.
 All of the Internal Booster, Voltage Regulator,
 Voltage Follower using.
 Internal power supply ON (instruction)
 (T₁, T₂)=(L, L)

- (2) Only V_{OUT} Supply from outside Example.
 Internal Voltage Regulator,
 Voltage Follower using
 Internal power supply ON (Instruction)
 (T₁, T₂)=(H, L)



- (3) V_{OUT} and V₅ supply from outside Example.
 Internal Voltage Follower using.
 Internal power supply (Instruction)
 (T₁, T₂)=(H, H)

- (4) External Power Supply Example.
 All of V₁ to V₅ and V_{OUT} supply from outside
 Internal power supply (Instruction)
 (T₁, T₂)=(H, H)



⊗: These switches should be open during the power save mode.

(2) Instruction

The **NJU6673** distinguishes the signal on the data bus D₀ to D₇ as an Instruction by combination of A0, RD and WR(R/W). The decode of the instruction and execution performs with only high speed Internal timing without relation to the external clock. Therefore no busy flag check required normally. In case of serial interface, the data input as MSB(D₇) first serially. The Table. 4 shows the instruction codes of the **NJU6673**.

Table 4 Instruction Code

(*:Don't Care)

Instruction		Code										Description	
		A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
(a)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display ON/OFF D ₀ =0:OFF D ₀ =1:ON
(b)	Display Start Line Set	0	1	0	0	1	*	Start address					Determine the Display Line of RAM to COM ₀
(c)	Page Address Set	0	1	0	1	0	1	*	*	Page Address			Set the page of DD RAM to the Page Address Register
(d)	Column Address Set High Order 3bits	0	1	0	0	0	0	1	0	High Order Column			Set the Higher order 3 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add			Set the Lower order 4 bits Column Address to the Reg.	
(e)	Status Read	0	0	1	Status			0	0	0	0		Read out the internal Status
(f)	Write Display Data	1	1	0	Write Data							Write the data into the Display Data RAM	
(g)	Read Display Data	1	0	1	Read Data							Read the data from the Display Data RAM	
(h)	Normal or Inverse of ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the ON and OFF Display
(i)	Static Drive ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns ON D ₀ =0: Normal D ₀ =1: Whole Disp. ON
(j)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V ₅ output level to the EVR register
(k)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address Register when writing but no-change when reading
(l)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify write Mode
(m)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the Internal Circuits
(n)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0/1	0: Int. Power Supply OFF 1: Int. Power Supply ON
(o)	Driver Outputs ON/OFF	0	1	0	1	0	1	0	1	0	1	0/1	D ₀ =0: LCD Driver Outputs OFF D ₀ =1: LCD Driver Outputs ON
(p)	Power Save (Complex command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power Save Mode (LCD Display OFF + Static Drive ON)
		0	1	0	1	0	1	0	0	1	0	1	
(q)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment D ₀ =0 :Normal D ₀ = 1:Inverse

(2-1) Explanation of Instruction Code

(a) Display On/Off

It executes the On/Off control of the whole display without relation to the DD RAM or any internal conditions.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
 1: Display On

(b) Display Start Line

It sets the DD RAM line address corresponding to the COM₀ terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	1	*	A ₄	A ₃	A ₂	A ₁	A ₀

A ₄	A ₃	A ₂	A ₁	A ₀	Line Address(HEX)
0	0	0	0	0	00
0	0	0	0	1	01
		⋮			⋮
		⋮			⋮
1	1	0	0	0	18

(c) Page Address Set

When MPU accesses to the DD RAM, a page address is set by page Address Set instruction before writing the data (Note:the change of page address is not affected to the display).

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	*:Don't Care
0	1	0	1	0	1	1	*	*	A ₁	A ₀	

A ₁	A ₀	Page
0	0	0
0	1	1
1	0	2
1	1	3

(d) Column Address

When MPU accesses to the DD RAM, row address set by Page Address Set instruction is required with the column address before writing the data. The column address set requires twice address set which are higher order 3 bits address set and lower order 4 bits. When the MPU accesses to the DDRAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of the column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	\overline{RD}	\overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0		
0	1	0	0	0	0	1	0	A ₆	A ₅	A ₄	Higher Order	
0	1	0	0	0	0	0	0	A ₃	A ₂	A ₁	A ₀	Lower Order

A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Column Address (HEX)
0	0	0	0	0	0	0	00
0	0	0	0	0	0	1	01
			⋮				⋮
			⋮				⋮
1	1	0	0	0	1	1	63

(e) Status Read

This instruction reads out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET" as follows.

A0	\overline{RD}	\overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.

0: Counterclockwise Output (Inverse)

1: Clockwise Output (Normal)

Note) The data "0=Inverse" and "1=Normal" of ADC status is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF: Indicate the whole display On/Off status.

0: Whole Display "On"

1: Whole Display "Off"

Note) The data "0=On" and "1=Off" of Display On/Off status is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET :Indicate the initializing by \overline{RES} signal or reset instruction.

0: Not Reset status

1: In the Reset status

(f) Write Display Data

It writes the data on the data bus into the DD RAM column address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuously without the address setting at every writing time once the starting address is set.

A0	\overline{RD}	\overline{WR}	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

(g) Read Display Data

This instruction reads out the 8-bit data from DD RAM addressed by the column and the page address. The column address automatically increments after the 8-bit read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see“(4-4)Access to the DD RAM and the Internal Register”). In the serial interface mode, the display data is unable to read out.

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	Read Data							

(h) Normal or Inverse On/Off Set

It changes the display condition of normal or reverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data “1” correspond to “On”
 1: Inverse RAM data “0” correspond to “On”

(i) Static Drive

This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the “Normal or Inverse On/Off Set” instruction.

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
 1: Whole Display turns On

(j) EVR Register Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage “V₅”. By data setting into the EVR register, the LCD driving voltage “V₅” selects out of 16 steps of regulated voltage. The voltage adjustable range of “D₅” is fixed by the external resistors. For details, refer the section“(3-2) Voltage Adjust Circuits”.

A0	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	0	0	A ₃	A ₂	A ₁	A ₀

A ₃	A ₂	A ₁	A ₀	V _{LCD}
0	0	0	0	Low
		⋮		⋮
1	1	1	1	High

$$V_{LCD} = V_{DD} - V_5$$

When EVR doesn't use, set the EVR register to (0,0,0,0).

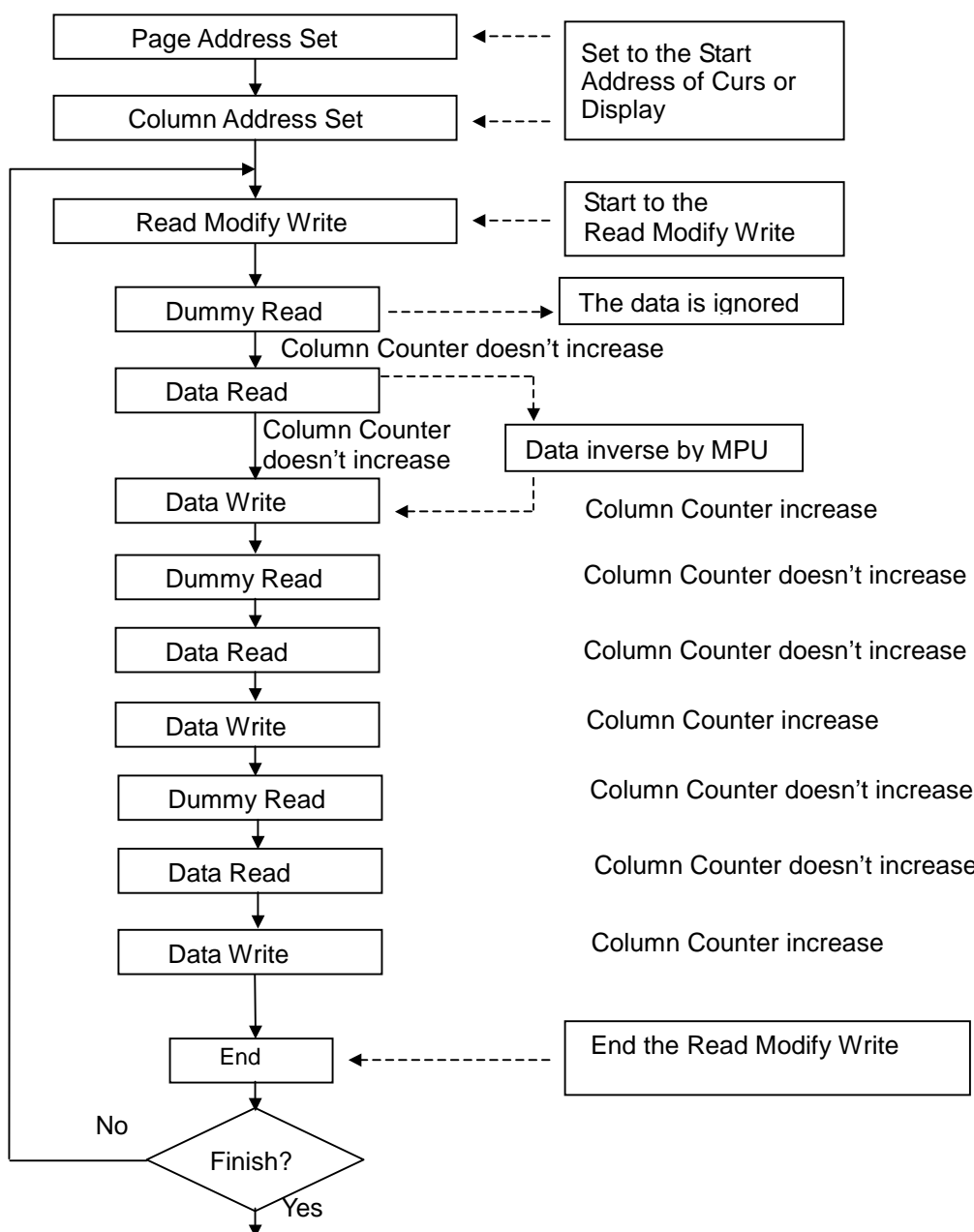
(k) Read Modify Write

This instruction sets the Read Modify Write controlling the page address increment. In this mode, the Column Address only increments when execute the display data "Write instruction; but no change when the display data "Read " Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Address goes back to the start address before the execution of this "Read Modify Write" instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink)

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	0	0

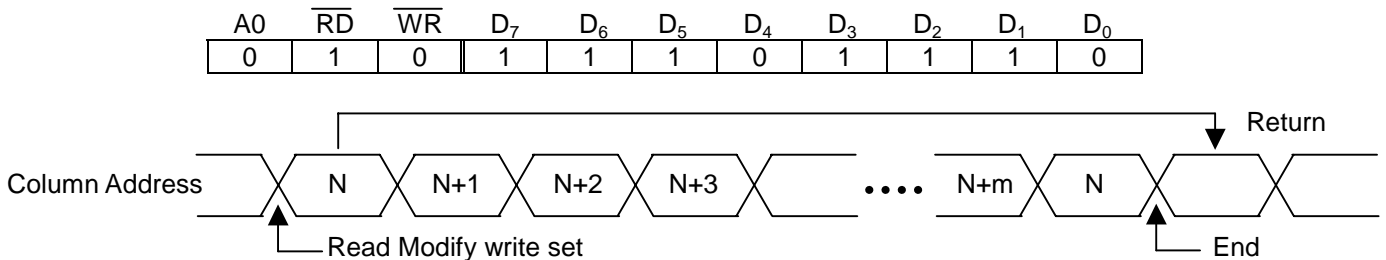
Note) In this "Read Modify Write" mode, out of display data "Read"/"Write", any instructions except "Column Address Set" can be executed.

● The Example of Read Modify Write Sequence



(l) End

This instruction releases the Read Modify Write mode and the column address back to the address where the read modify write mode setting.



(m) Reset

This instruction executes the following initialization. The reset by the reset signal input to the \overline{RES} terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

- 1) Set the Display Start Line Register to 00_H.
- 2) Set the Column Address Counter to 00_H.
- 3) Set the page Page Address Register to page "0".
- 4) Set the EVR Register to 0_H.

The DD RAM is not affected of this initialization.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	1	1	0	0	0	1	0

(n) Internal Power Supply ON/OFF

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
 1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, V_{DD} and V_{LCD} . Therefore it requires the actual evaluation using the LCD module to get the correct time.(Refer to the (3-4) Fig.4)

(o) Driver Outputs ON/OFF

This instruction controls ON/OFF of the LCD Driver Outputs.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	1	0	1	D

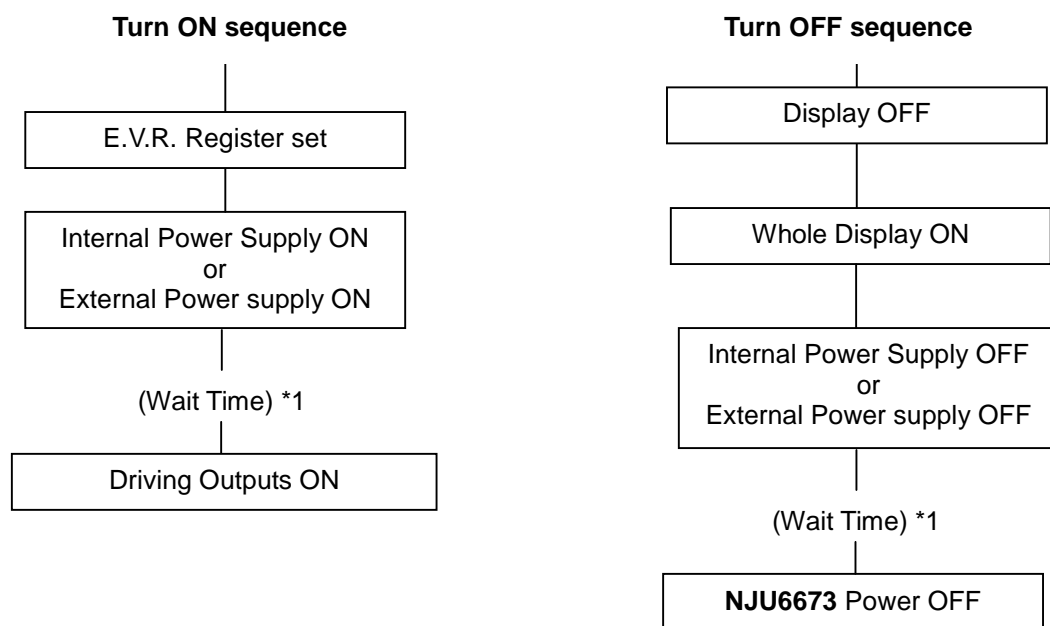
D 0: LCD driving waveform output Off

1: LCD driving waveform output On

The **NJU6673** implements low power LCD driving voltage generator circuit and requires the following Power supply ON/OFF sequence.

● LCD Driving power supply ON/OFF sequences

The sequences below are required when the power supply turns ON/OFF. For the power supply turning on operation after the power-save mode, refer the "power save release sequence" mentioned after.



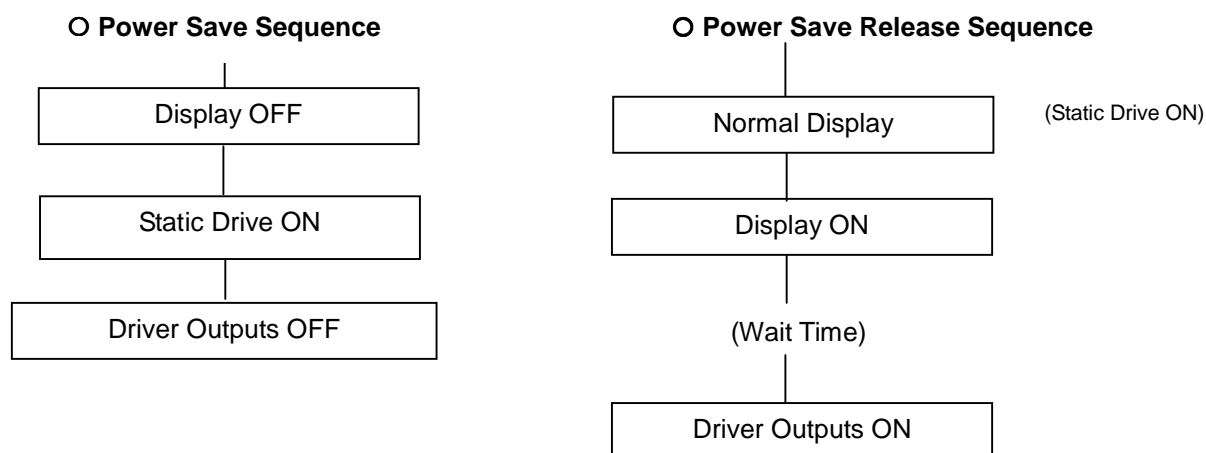
*1 : The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$ External Capacitor of Booster, and External Capacitor connected to V_1 to V_5 . To know the rise time correctly, test by using the actual LCD module.

(p) Power Save(complex command)

When Static Drive ON at the Display OFF status(inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current. The internal status in the Power Save Mode is shown as follows;

- 1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
- 2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
- 3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
- 4: All the LCD driving bias voltage(V_1 to V_5) is fixed to the V_{DD} level.

The power save and its release perform according to the following sequences.



The **NJU6673** constantly spends the current without the execution of the Driver Outputs OFF instruction. The LCD drive waveform is not output until the Driver Outputs ON instruction is executed.

- *1 : In the Power Save sequence, the Power Save Mode starts after the Static Drive ON bcommand is executed.
- *2 : In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
- *3 : The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V_5$, External Capacitor of Booster, and External Capacitor connected to V_1 to V_5 . To know the rise time correctry, test by using the actual LCD module.
- *4 : LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
- *5 : In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage of V_{OUT} terminal. In this time, V_{OUT} terminal also should be made codition like as disconnection to the lowest voltage of the system.

(q) ADC Select

This instruction determines the correspondence of Column in the DD RAM with the Segment Driver Outputs. Segment Driver Outout order is inverse when this instruction executes, therefore, the placement the **NJU6673** against the LCD panel becomes easy.

A0	\overline{RD}	\overline{WR}	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	0	1	0	0	0	0	0/1

D 0: Clokwise Output(Normal)
 1: Counterclockwise Output(Inverse)

(3) Internal Power Supply

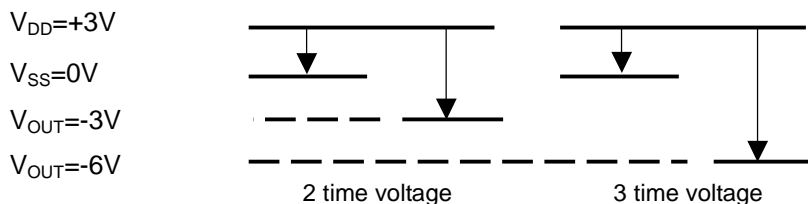
(3-1) Voltage tripler

The 3-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 3 times of $V_{DD}-V_{SS}$ from the V_{OUT} terminal with connecting the five capacitors between C_{1+} and C_{1-} , C_{2+} and C_{2-} , and V_{SS} and V_{OUT} . In case of the 2-time voltage booster operation, connect the two capacitor between C_{2+} and C_{2-} , V_{SS} and V_{OUT} , then connect the C_{1+} and C_{2+} terminals. Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal. therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.

The boosted voltage of $V_{DD}-V_{OUT}$ must be 10V or less.

The boost voltage and the capacitor connection are shown below.

● The boosted voltage and V_{DD} , V_{SS}



(3-2) Voltage Adjust Circuits

The boosted voltage of V_{OUT} outputs V_5 for LCD driving through the voltage adjust circuits. The output voltage of V_5 is adjusted by R_a and R_b within the range of $|V_5| < |V_{OUT}|$.

The output is calculated by the following formula(1).

$$V_{LCD} = V_{DD}-V_5 = (1+R_b/R_a)V_{REG} \dots \dots \dots (1)$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder resistance. V_{REG} is adjustable by EVR functions (see section 3-3).

For minor adjustment of V_5 , it is recommended that the R_a and R_b is composed of R_2 as variable resistor and R_1 and R_3 as fixed resistors, constant should be connected to V_{DD} terminal, V_R and V_5 , as shown below.

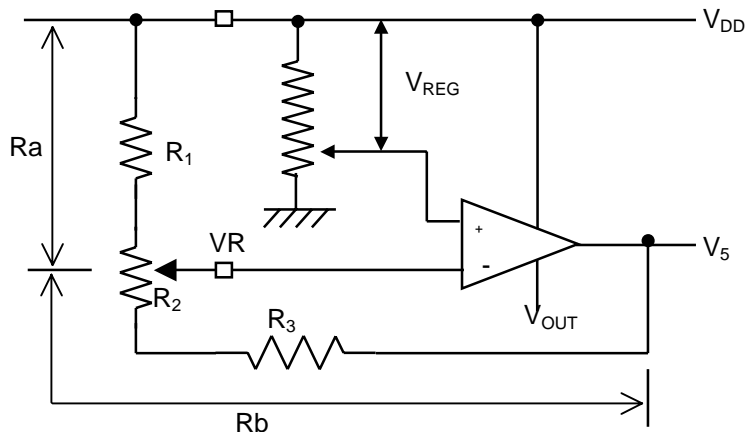


Fig-3 Voltage Adjust Circuit

<Design example for R_1 , R_2 and R_3 / Reference>

- $R_1+R_2+R_3=3.1M\Omega$
(Determined by the current flown between $V_{DD}-V_5$)
- Variable voltage range by the R_2 . -3.2V to -6.3V ($V_{LCD}=V_{DD}-V_5=6.2V$ to 9.3V)
(Determined by the LCD electrical characteristics)
- $V_{REG}=3V$ (In case of $EVR=(F)_H$)
- R_1 , R_2 and R_3 are calculated by above conditions and the formula of (1) to mentioned below;
 $R_1=1.0M\Omega$, $R_2=0.5M\Omega$, $R_3=1.6M\Omega$

Note) V_5 voltage is generated referencing with V_{REG} voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above figure. Therefore, V_{LCD} ($V_{DD}-V_5$) is affected including the gain (R_b/R_a) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V_5 stable operation.

(3-3) Contrast Adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 16 conditions by setting 4-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V_5 .

A step with EVR is set like table shown below.

EVR register		V_{REG} [V]	V_{LCD}
0 _H	(0, 0, 0, 0)	$(135/150)(V_{DD}-V_{SS})$	Low
1 _H	(0, 0, 0, 1)	$(136/150)(V_{DD}-V_{SS})$	⋮
2 _H	(0, 0, 1, 0)	$(137/150)(V_{DD}-V_{SS})$	⋮
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
E _H	(1, 1, 1, 0)	$(149/150)(V_{DD}-V_{SS})$	⋮
F _H	(1, 1, 1, 1)	$(150/150)(V_{DD}-V_{SS})$	High

* In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

- Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition $V_{DD}=3.0V$, $V_{SS}=0V$

$R_a=1M\Omega$, $R_b=1M\Omega$ ($R_a:R_b=1:1$)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting 00_H in the EVR register,

$$\begin{aligned} V_{LCD} &= ((R_a+R_b)/R_a) V_{REG} \\ &= (2/1)[(135/150)3.0] \\ &= 5.4V \end{aligned}$$

In case of setting 0F_H in the EVR register,

$$\begin{aligned} V_{LCD} &= ((R_a+R_b)/R_a) V_{REG} \\ &= (2/1)[(150/150)3.0] \\ &= 6.0V \end{aligned}$$

	(min.)0 _H	(max.)F _H
Adjustable Range	5.4	6.0 [V]
Step Voltage	40 [mV]	

(3-4) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated by dividing the V_5 voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedance conversion by the voltage follower.

The external capacitors to V_1 to V_5 for Bias voltage stabilization may be removed in use of small size LCD panel. The equivalent load of LCD panel may be changed depending on display patterns. Therefore, it require display quality check on various display patterns actually without external capacitors. If the display quality is not so good, external capacitors should connects as show in Fig. 4. (If no need external capacitors as result of experiment, the application patterns (wiring) should be prepared for recovery.)

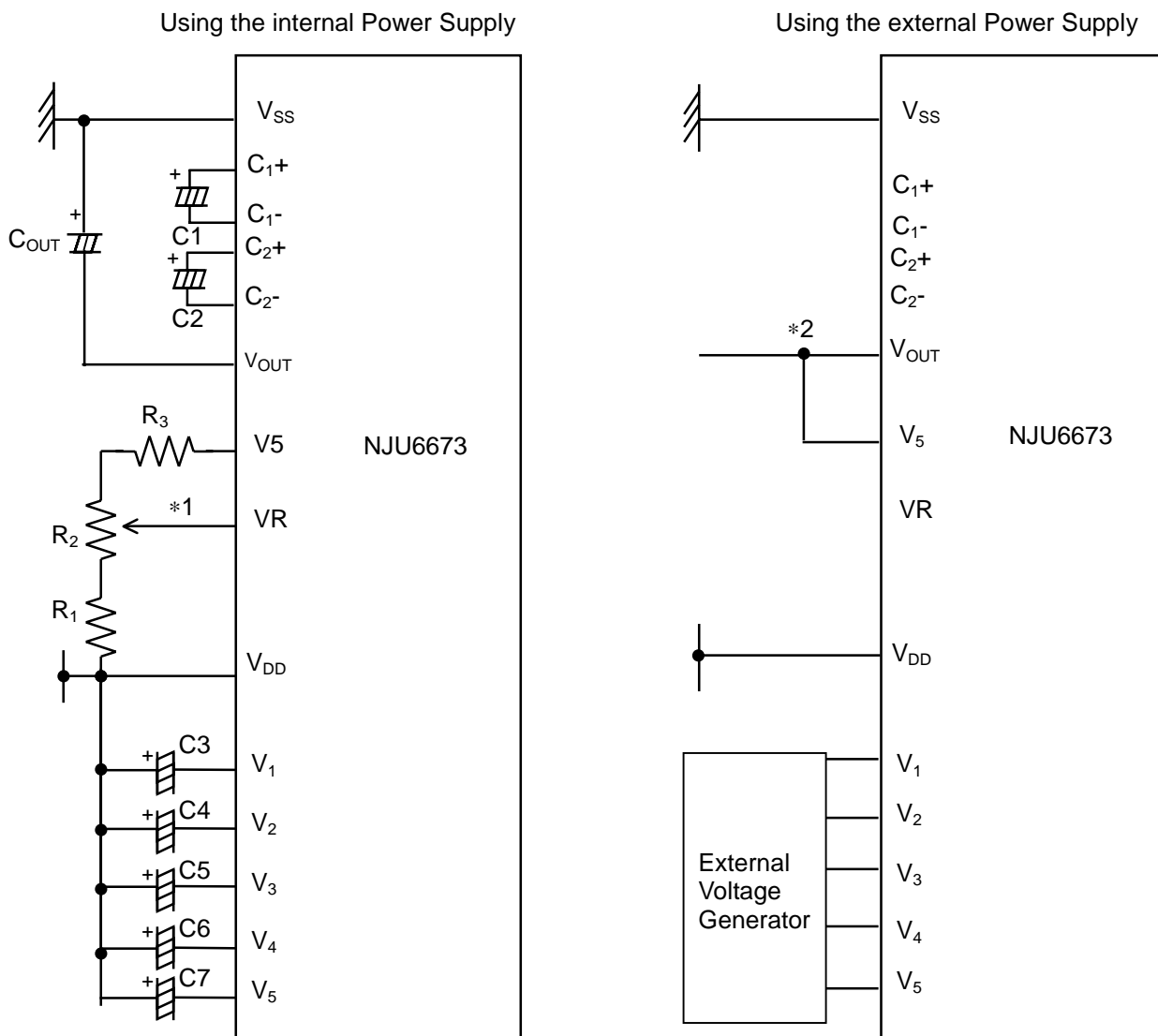


Fig.4

Reference set up value $V_{LCD} = V_{DD} - V_5 = 6.2-9.3V$

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.

*2 Following connection of V_{OUT} is required when external power supply using.

When $V_{SS} > V_5$, $V_{OUT} = V_5$

When $V_{SS} \leq V_5$, $V_{OUT} = V_{SS}$

C_{OUT}	to 1.0 μF
C_1, C_2	to 1.0 μF
C_3-C_7	0.1 to 0.47 μF
R_1	1M Ω
R_2	500k Ω
R_3	1.6M Ω

(4) MPU Interface

(4-1) Interface type selection

Two MPU interface types are available in the **NJU6673**: by 1) 8-bit bi-directional data bus (D₇ to D₀), 2) serial data input (SI:D₇). The interface type (the 8 bit parallel or serial interface) is determined by the condition of the P/S terminals connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed..

Table 5

P/S	I/F type	\overline{CS}	A0	\overline{RD}	\overline{WR}	SEL68	D ₇	D ₆	D ₅ -D ₀
H	Parallel	\overline{CS}	A0	\overline{RD}	\overline{WR}	SEL68	D ₇	D ₆	D ₅ -D ₀
L	Serial	\overline{CS}	A0	-	-	-	SI	SCL	Hi-Z

Parallel Interface

The **NJU6673** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S="H") is selected.

The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	\overline{CS}	A0	\overline{RD}	\overline{WR}	D ₇ -D ₀
H	68 type MPU	\overline{CS}	A0	E	R/W	D ₇ -D ₀
L	80 type MPU	\overline{CS}	A0	\overline{RD}	\overline{WR}	D ₇ -D ₀

(4-2) Discrimination of Data Bus Signal

The **NJU6673** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and (RD, WR) signals as shown in Table 7.

Table 7

common	68 type	80 type		Function
A0	R/W	\overline{RD}	\overline{WR}	
H	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface.(P/S="L")

The serial interface of the **NJU6673** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($\overline{CS}=L$), the input to D_7 (SI) and D_6 (SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.

The data input from the terminal(SI) is MSB first like as the order of D_7, D_6, \dots, D_0 , by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.

It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0="H" and instruction by A0="L" A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.

However, in case of RES="H" to "L" or CS="L" to "H" with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.

The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

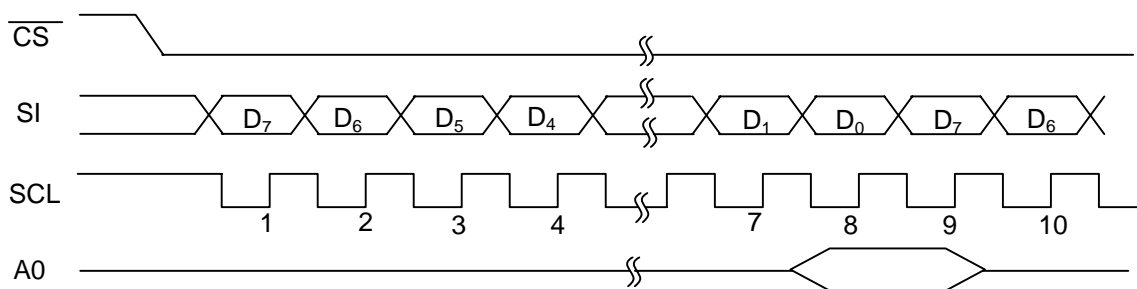


Fig.5

(4-4) Access to the Display Data RAM and Internal Register.

The **NJU6673** transfers data to the MPU through the bus holder with the internal data bus.

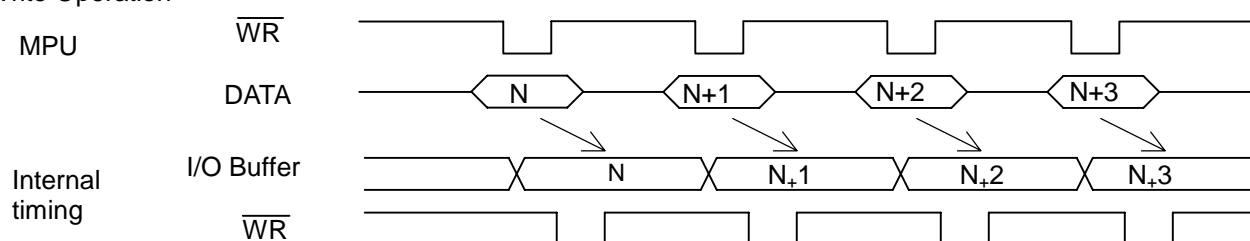
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6673** from MPU side is not access time (t_{ACC}, t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the satisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 6)

The example of Read Modify Write operation is mentioned in (2-1)Instruction -k)The sequence of Inverse Display.

● Write Operation



● Read Operation

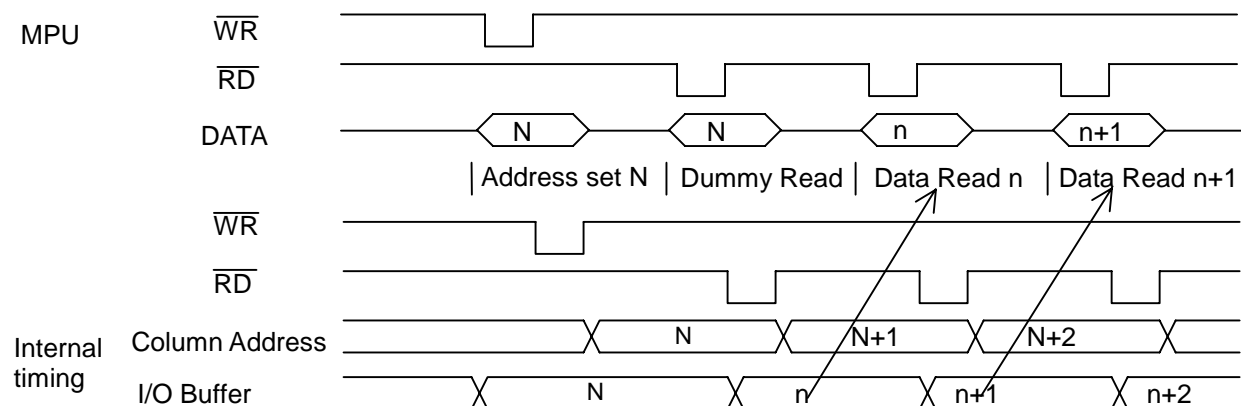


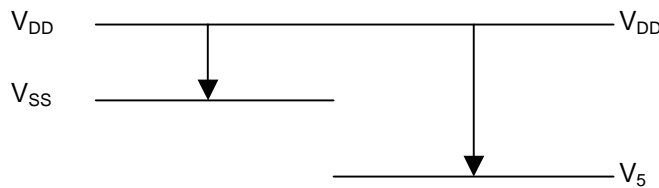
Fig.6

(4-5) Chip Select

\overline{CS} is Chip Select terminal. In case of $\overline{CS}="L"$, the interface with MPU is available. In case of $\overline{CS}="H"$, the D_0 to D_7 are high impedance and A_0 , \overline{RD} , \overline{WR} , SI and SCL inputs are ignored. If the serial interface is selected when $\overline{CS}="H"$ the shift register and counter are reset. However, the reset is always operated in any conditions of \overline{CS} .

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(1)	V_{DD}	-0.3 - +7.0	V
		-0.3 -+3.6(Used Tripler)	
Supply Voltage(2)	V_5	$V_{DD}-11.0 - V_{DD}+0.3$	V
Supply Voltage(3)	V_1, V_2, V_3, V_4	$V_5-V_{DD}+0.3$	V
Input Voltage	V_{IN}	$-0.3-V_{DD}+0.3$	V
Operating Temperature	T_{opr}	-30-+80	°C
Storage temperature	T_{stg}	-55-+125	°C



Note 1) All voltage values are specified as $V_{SS}=0V$.

Note 2) The relation of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 > V_{OUT}$; $V_{DD} > V_{SS} \geq V_{OUT}$ must be maintained.

In case of inputting external LCD driving voltage, the LCD drive voltage should start supplying to **NJU6673** at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .

In use of the voltage boost circuit, the condition that the supply voltage: $11.0V \geq V_{DD} - V_{OUT}$ is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.

Using LSI within electrical characteristics is strongly recommended for normal operation.

Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=2.4V-3.6V, V_{SS}=0V, Ta=-20 to 75°C)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating voltage(1)	Recommend	V _{DD}		2.4	3.0	3.6	V	1
	Available			2.4		5.5		
Operating voltage(2)	Recommend	V ₅	V _{LCD} =V _{DD} -V ₅	V _{DD} -10.0		V _{DD} -4.0	V	
	Available			V _{DD} -10.0				
	Available	V ₁ ;V ₂		V _{DD} -0.6V _{LCD}		V _{DD}		
	Available	V ₃ ;V ₄		V ₅		V _{DD} -0.4V _{LCD}		
Input Voltage	High Level	V _{IHC}	A0, D ₀ -D ₇ , \overline{RD} , \overline{WR} , \overline{RES} , \overline{CS}	0.8V _{DD}		V _{DD}	V	
	Low Level	V _{ILC}	P/S, SEL68, DUTY, CDIR Terminal	V _{SS}		0.2V _{DD}		
Output Voltage	High Level	V _{OHC}	D ₀ -D ₇ Terminal	I _{OH} =-0.5mA 0.8V _{DD}		V _{DD}	V	
	Low Level	V _{OLC}		I _{OL} = 0.5mA V _{SS}		0.2V _{DD}		
Input Leakage Current		I _{LI}	All input terminals	-1.0		1.0	μA	
		I _{LO}	D ₀ to D ₇ terminals, Hi-Z state	-3.0		3.0		
Driver On-resistance		R _{ON}	Ta=25°C, V _{LCD} =8.0V		3.0	4.5	kΩ	2
Stand-by Current		I _{DDQ}	During Power Save Mode		0.05	5.0	μA	3
Input Terminal Capacitance		C _{IN}	Ta=25°C		10		pF	4
Oscillation Frequency		f _{OSC}	V _{DD} = 3.0V Ta =25°C	9.3	11.4	13.5	kHz	
Reset Time		t _R	\overline{RES} terminal	1.0			μs	5
Reset "L" level pulse Width		t _{RW}		10			μs	6

Voltage booster	Input voltage	V _{DD1}		2.4		5.5	V	
		V _{DD2}	3-times boost	2.4		3.3	V	
	Output voltage	V _{OUT1}	3-times boost, V _{DD} =3.0V	-6.6		-5.5	V	
	On-resistance	R _{TRI}	3-times boost, V _{DD} =3.0V, C _{OUT} =1.0μF		1600	2600	Ω	
	Adjustment range LCD driving oltage	V _{OUT2}	Voltage boost operation off	V _{DD} -10.0V		V _{DD} -4.0V	V	8
	Voltage Follower	V ₅	Voltage adjustment circuit "OFF"	V _{DD} -10.0V		V _{DD} -4.0V	V	
Voltage Regulator	V _{REG%}	V _{DD} =3.0V; Ta =25°C			3.0	%		

Operating Current	I _{OUT1}	V _{DD} =3.0V, V _{LCD} =8V, Display Checkerd pattern		50	105	μA	9
	I _{OUT2}			16	25	μA	

Note 1) Although the **NJU6673** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.

Note 2) R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V₁,V₂,V₃,V₄) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).

Note 3) Apply no access from MPU.

Note 4) Apply A0, D₀ to D₇, \overline{RD} , \overline{WR} , \overline{CS} , \overline{RES} ,SEL68,P/S,T₁,T₂,DUTY,CDIR terminals.

Note 5) t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the \overline{RES} signal.

Note 6) Apply minimum pulse width of the \overline{RES} signal. To reset, the "L" pulse over t_{RW} shall be input. .

Note 7) Apply to the V_{DD} when using 3-times boost.

Note 8) The voltage adjustment circuit controls V₅ within the range of the voltage follower operating voltage.

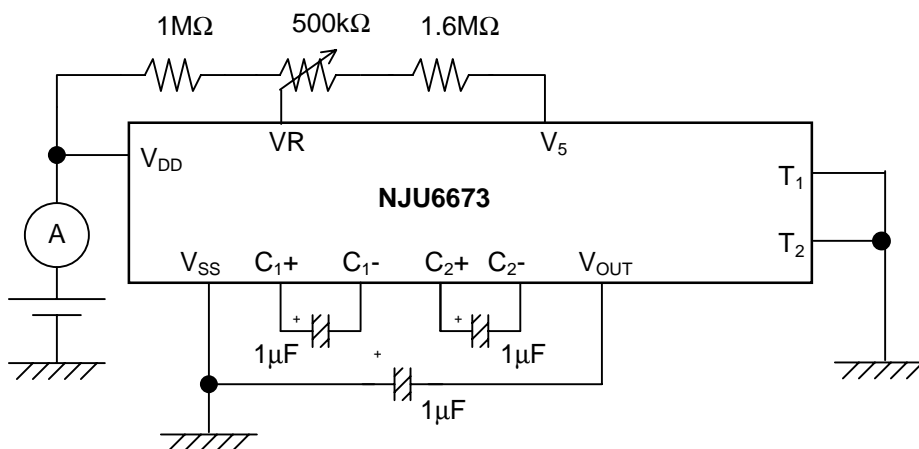
Note 9) Each operating current shall be defined as being measured in the following condition.

SYMBOL	Status		Operating Condition			External Voltage Supply (Input terminal)
	T ₁	T ₂	Voltage booster	Voltage adjustment	Voltage Follower	
I _{OUT1}	L	L/H	Validity	Validity	Validity	Unuse
I _{OUT2}	H	H	Invalidity	Invalidity	Invalidity	Use (V _{OUT} , V ₅)

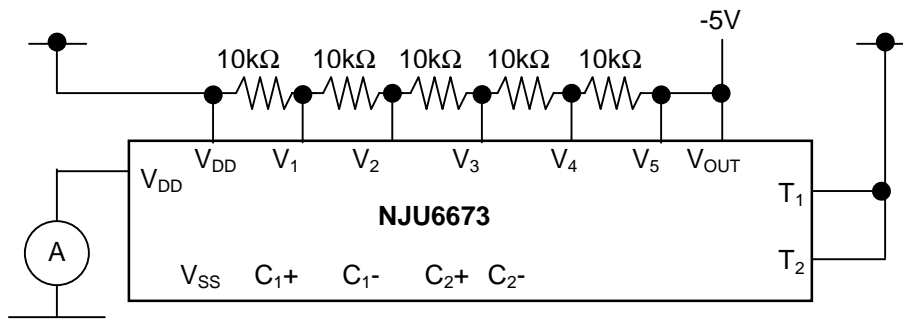
LCD output terminal Open.
 Display on, Display checered pattern, No access from MPU
 Set V_{LCD}=8V
 Internal Oscillator : Validity

MEASUREMENT BLOCK DIAGRAM

: I_{OUT1}

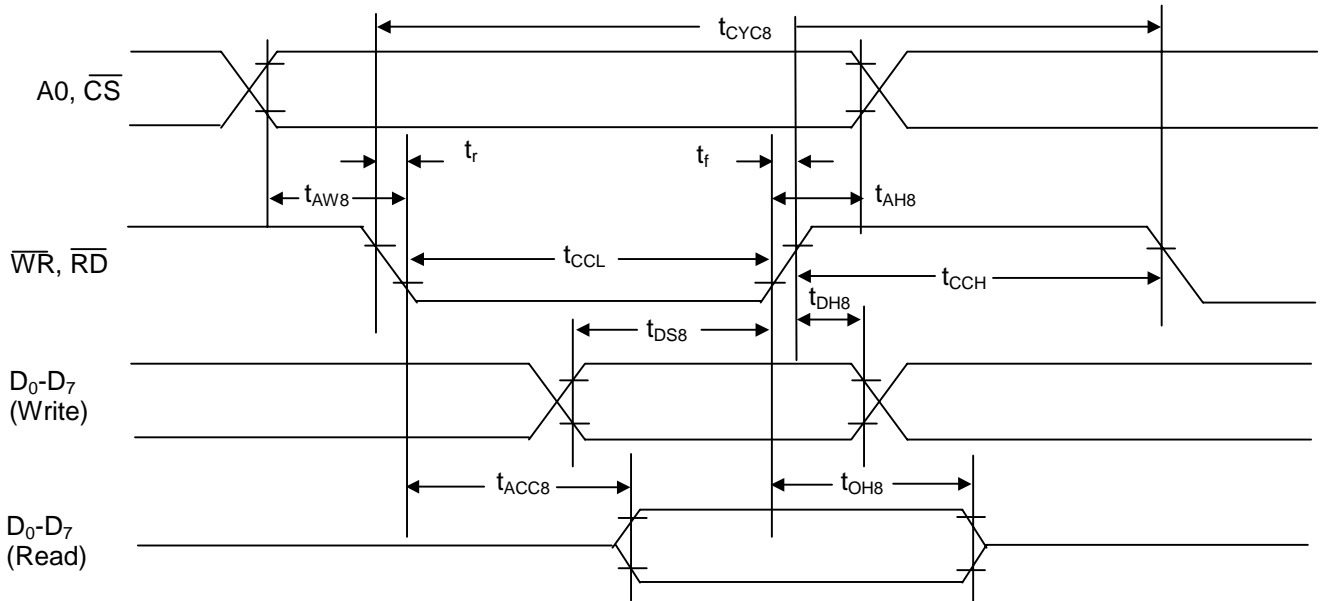


: I_{OUT2}



■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence(80 type MPU)

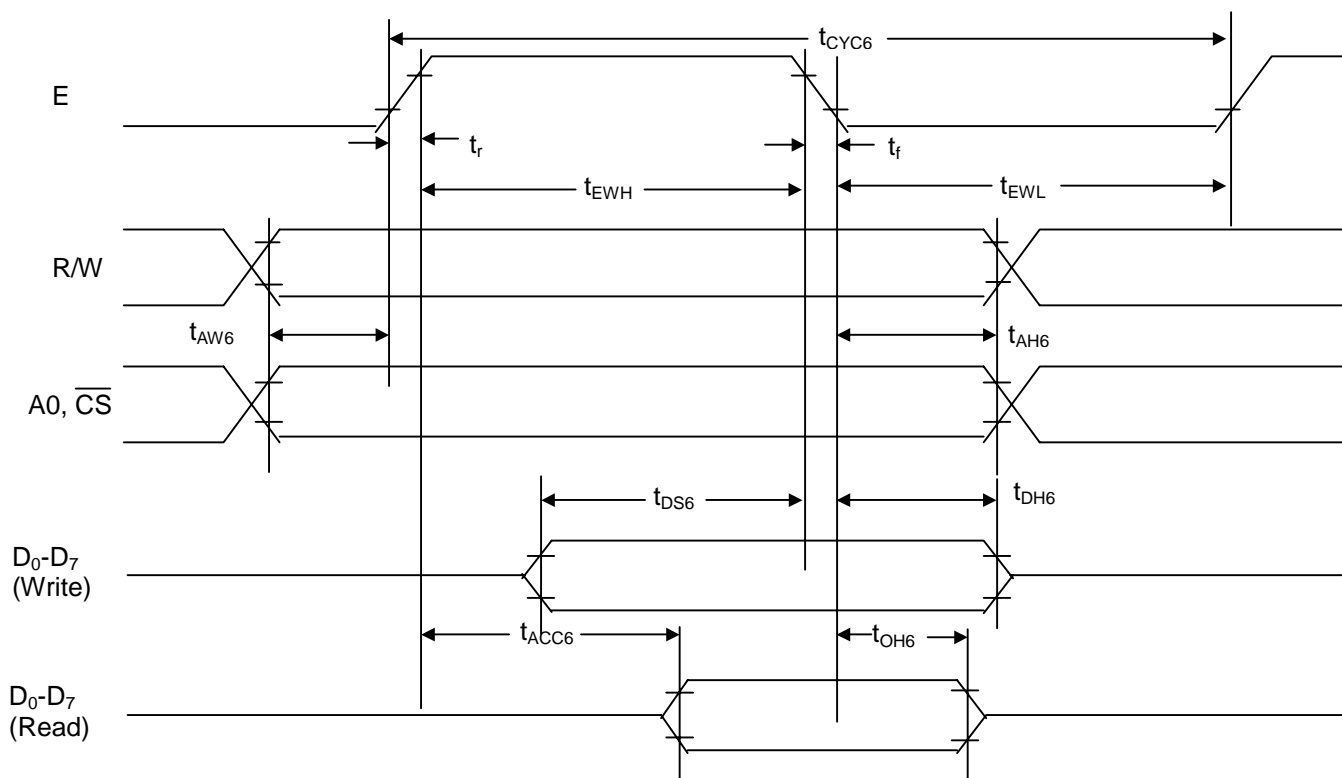


($V_{DD}=2.4V$ to $3.6V$, $T_a=-20$ to $75^{\circ}C$)

PARAMETER	SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Address Hold Time	t_{AH8}	A0, \overline{CS}		32			ns
Address Setup Time	t_{AW8}			0			
System Cycle Time	t_{CYC8}	\overline{WR} , \overline{RD}		560			
Control Pulse Width	\overline{WR} , "L"	$t_{CCL(W)}$		75			
	\overline{RD} , "L"	$t_{CCL(R)}$		250			
	"H"	t_{CCH}		275			
Data Setup Time	t_{DS8}	D_D-D_7		150			
Data Hold Time	t_{DH8}			30			
RD Access Time	t_{ACC8}		CL=100pF			175	
Output Disable Time	t_{OH8}			0		44	
Rise Time, Fall Time	t_r, t_f	$\overline{CS}, \overline{WR}, \overline{RD}$ A0, D_0-D_7				15	

Note 1) All timing based on 20% and 80% of V_{DD} voltage level.

Read/Write operation sequence(68 type MPU)



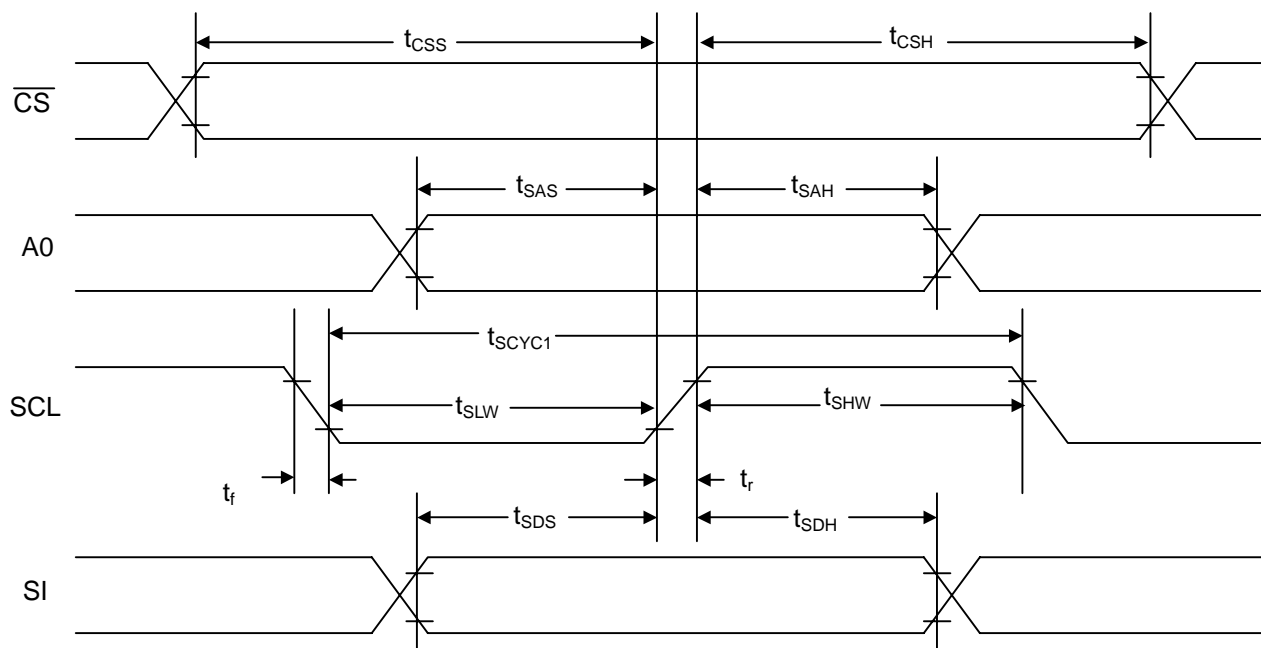
($V_{DD}=2.4V$ to $3.6V$, $T_a=-20$ to $75^{\circ}C$)

PARAMETER	SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Address Hold Time	t_{AH6}	A0, \overline{CS} R/W		32			ns
Address Setup Time	t_{AW6}			32			
System Cycle Time	t_{CYC6}	E		560			
Enable Pulse Width	t_{EWH}	E		250			
				62			
Data Setup Time	t_{DS6}	D ₀ -D ₇	CL=100pF	150			
Data Hold Time	t_{DH6}			50			
Access Time	t_{ACC6}			0		175	
Output Disable Time	t_{OH6}			0		56	
Rise Time, Fall Time	t_r, t_f	E, R/W, A0, D ₀ -D ₇				15	

Note 1) All timing based on 20% and 80% of V_{DD} voltage level.

Note 2) t_{CYC6} shows the cycle of the E signal in active \overline{CS} .

Write operation sequence(Serial Interface)

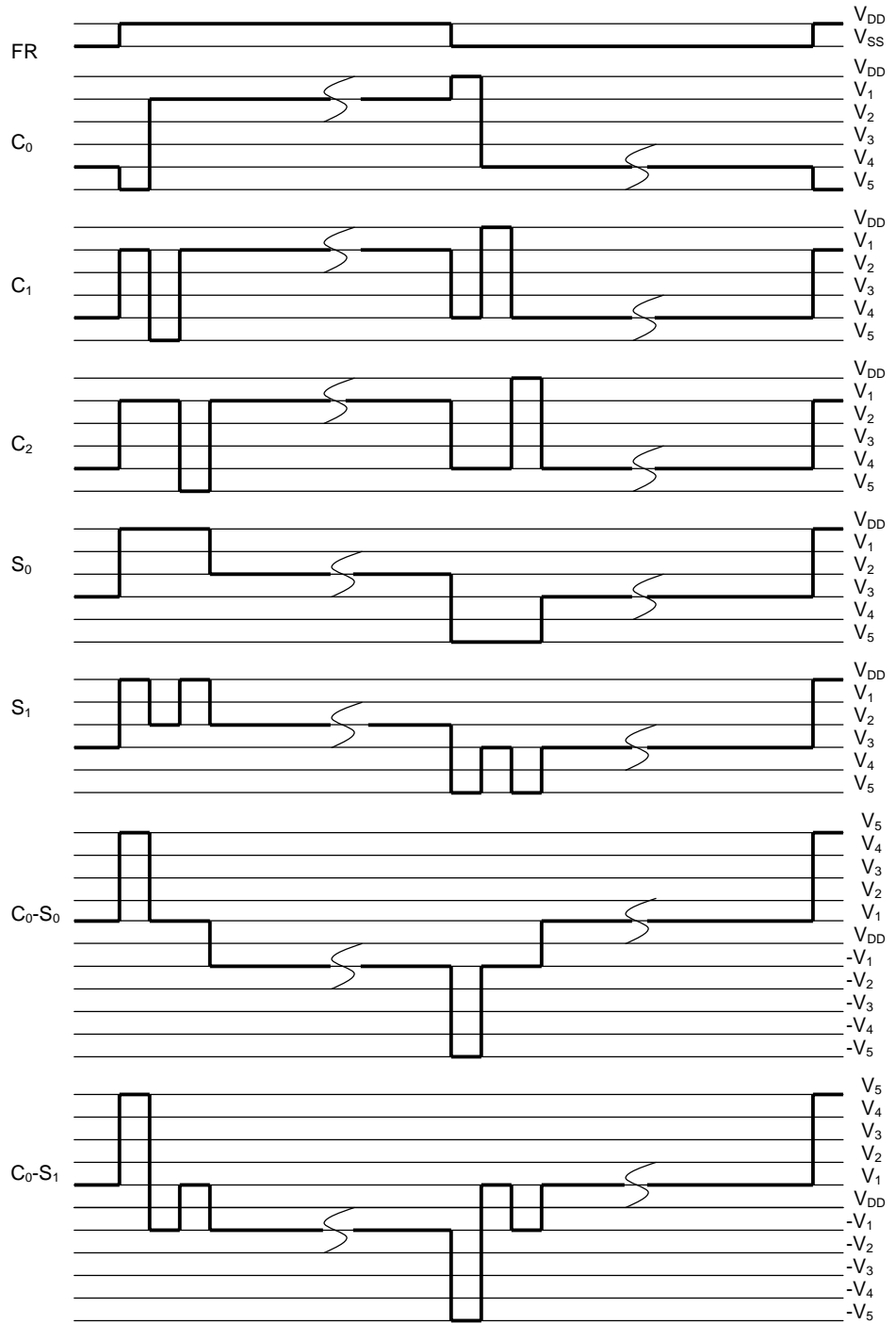
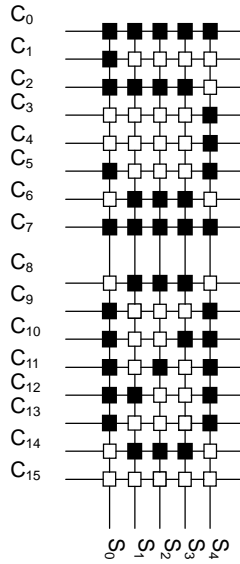


($V_{DD}=2.4V-3.6V$, $T_a=-20$ to $75^{\circ}C$)

PARAMETER	SYMBOL	SIGNAL	CONDITION	MIN	TYP	MAX	UNIT
Serial Clock cycle	t_{SCYC}	SCL		1000			ns
SCL "H" Pulse width	t_{SHW}			300			
SCL "L" Pulse width	t_{SLW}			300			
Address Setup Time	t_{SAS}	A0		250			
Address Hold Time	t_{SAH}			400			
Data Setup Time	t_{SDS}	SI		250			
Data Hold Time	t_{SDH}			100			
CS-SCL Time	t_{CSS}	\overline{CS}		60			
	t_{CSH}			800			
Rise time, Fall Time	t_r, t_f	CS, SCL SI, A0				15	

Note 1) All timing are based on 20% and 80% of V_{DD} voltage level.

■ LCD DRIVING WAVEFORM



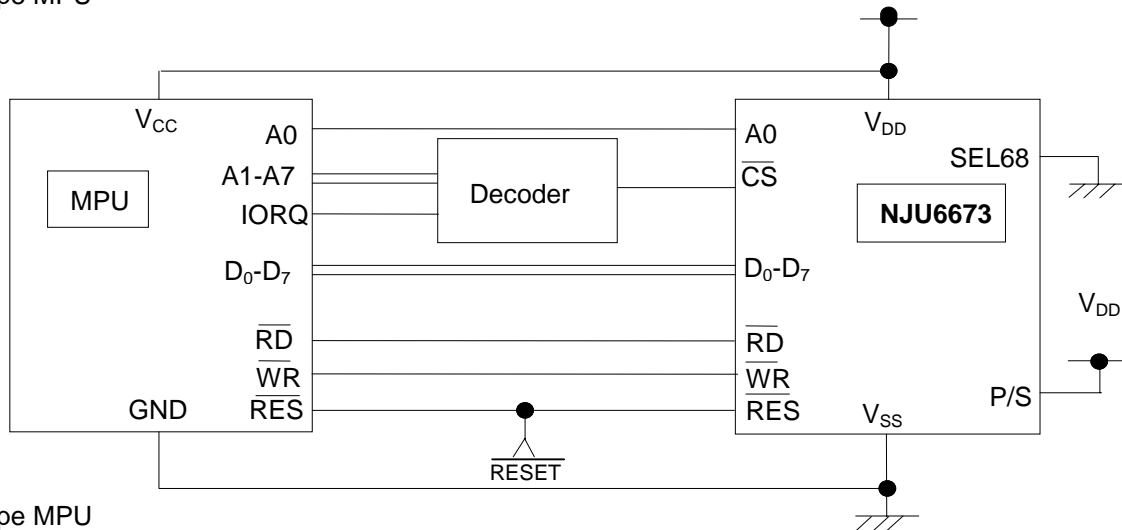
APPLICATION CIRCUIT

Microprocessor Interface Example

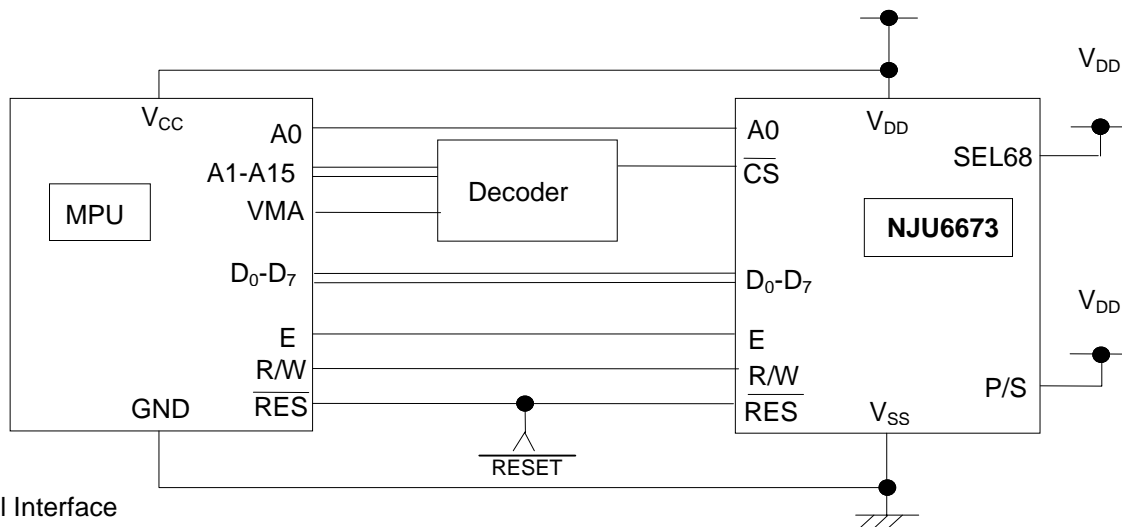
The **NJU6673** is connectable to 80-type MPU or 68-type. In use of Serial Interface, it is possible to be controlled by the signal line with the more small being.

*:SEL68 terminal shall be connected to V_{DD} or V_{SS} .

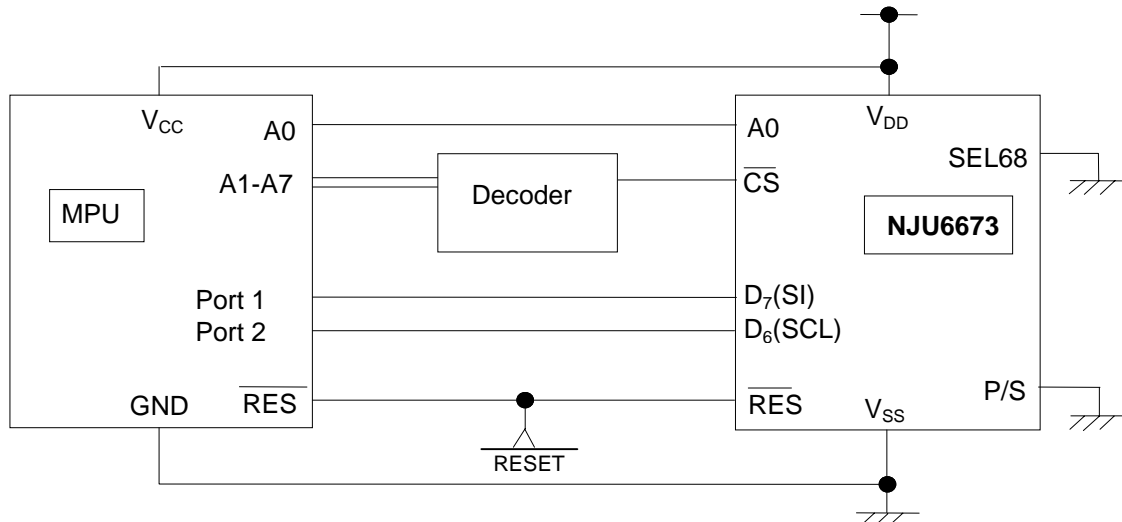
- 80 type MPU



- 68 type MPU



- Serial Interface



MEMO

[CAUTION]

The specifications on this databook are only given for information , without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.