FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13705-3E

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90595/595G Series

MB90598/F598/F598G/V595/V595G

■ DESCRIPTION

The MB90595/595G series with FULL-CAN*1 interface and FLASH ROM is especially designed for automotive and industrial applications. Its main features are two on board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach.

The instruction set of F²MC-16LX CPU core inherits an AT architecture of the F²MC*2 family with additional instruction sets for high-level languages, extended addressing mode, enhanced multiplication/division instructions, and enhanced bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word data.

The MB90595/595G series has peripheral resources of 8/10-bit A/D converters, UART (SCI), extended I/O serial interface, 8/16-bit PPG timer, I/O timer (input capture (ICU), output compare (OCU)) and stepping motor controller.

*1: Controller Area Network (CAN) - License of Robert Bosch GmbH

*2: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock

  Embedded PLL clock multiplication circuit

  Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz, 4 MHz to 16 MHz).

  Minimum instruction execution time: 62.5 ns (operation at oscillation of 4 MHz, four times the oscillation clock, V_{CC} of 5.0 V)

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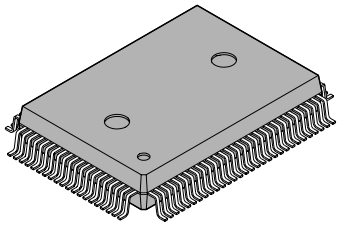
■ PACKAGE

100-pin Plastic QFP



(FPT-100P-M06)

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- Instruction set to optimize controller applications
  Rich data types (bit, byte, word, long word)
  Rich addressing mode (23 types)
  Enhanced signed multiplication/division instruction and RETI instruction functions
  Enhanced precision calculation realized by the 32-bit accumulator
- Instruction set designed for high level language (C language) and multi-task operations
  Adoption of system stack pointer
  Enhanced pointer indirect instructions
  Barrel shift instructions
- Program patch function (for two address pointers)
- Enhanced execution speed: 4-byte instruction queue
- Enhanced interrupt function: 8 levels, 34 factors
- Automatic data transmission function independent of CPU operation
  Extended intelligent I/O service function (EI^{2}OS): Up to 10 channels
- Embedded ROM size and types
  Mask ROM: 128 Kbytes
  Flash ROM: 128 Kbytes
  Embedded RAM size: 4 Kbytes (MB90V595/595G : 6 Kbytes)
- Flash ROM
  Supports automatic programming, Embedded Algorithm ™*
  Write/Erase/Erase-Suspend/Resume commands
  A flag indicating completion of the algorithm
  Hard-wired reset vector available in order to point to a fixed boot sector
  Erase can be performed on each block
  Block protection with external programming voltage
- Low-power consumption (stand-by) mode
  Sleep mode (mode in which CPU operating clock is stopped)
  Stop mode (mode in which oscillation is stopped)
  CPU intermittent operation mode
  Hardware stand-by mode
- Process: 0.5 μm CMOS technology
- I/O port
  General-purpose I/O ports: 78 ports
  Push-pull output and Schmitt trigger input.
  Programmable on each bit as I/O or signal for peripherals.
- Timer
  Watchdog timer: 1 channel
  8/16-bit PPG timer: 8/16-bit × 6 channels
  16-bit re-load timer: 2 channels
- 16-bit I/O timer
  Input capture: 4 channels
  Output compare: 4 channels
- Extended I/O serial interface: 1 channel
- UART0
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized (with start/stop bit) transmission can be selectively used.

- UART1 (SCI)
  With full-duplex double buffer (8-bit length)
  Clock asynchronized or clock synchronized serial transmission (I/O extended transmission) can be selectively used.
- Stepping motor controller (4 channels)
- External interrupt circuit (8 channels)
  A module for starting an extended intelligent I/O service (EI^{2}OS) and generating an external interrupt which is triggered by an external input.
- Delayed interrupt generation module: Generates an interrupt request for switching tasks.
- 8/10-bit A/D converter (8 channels)
  8/10-bit resolution can be selectively used.
  Starting by an external trigger input.
- FULL-CAN interface: 1 channel
  Conforming to Version 2.0 Part A and Part B
  Flexible message buffering (mailbox and FIFO buffering can be mixed)
- 18-bit Time-base counter
- External bus interface: Maximum address space 16 Mbytes

*: Embedded Algorithm is a trademark of Advanced Micro Devices Inc.

■ PRODUCT LINEUP

Features		MB90598	MB90F598/F598G	MB90V595/V595G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None
RAM size		4 Kbytes	4 Kbytes	6 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 µs (at machine clock frequency of 16 MHz, minimum value)		
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/ slave connection.		
UART1(SCI)		Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronized transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/ slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 (fsys = system clock frequency) 128µs (fosc = 4MHz : oscillation clock frequency)		
16-bit Reload timer		Number of channels: 2 Operation clock frequency: fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)		

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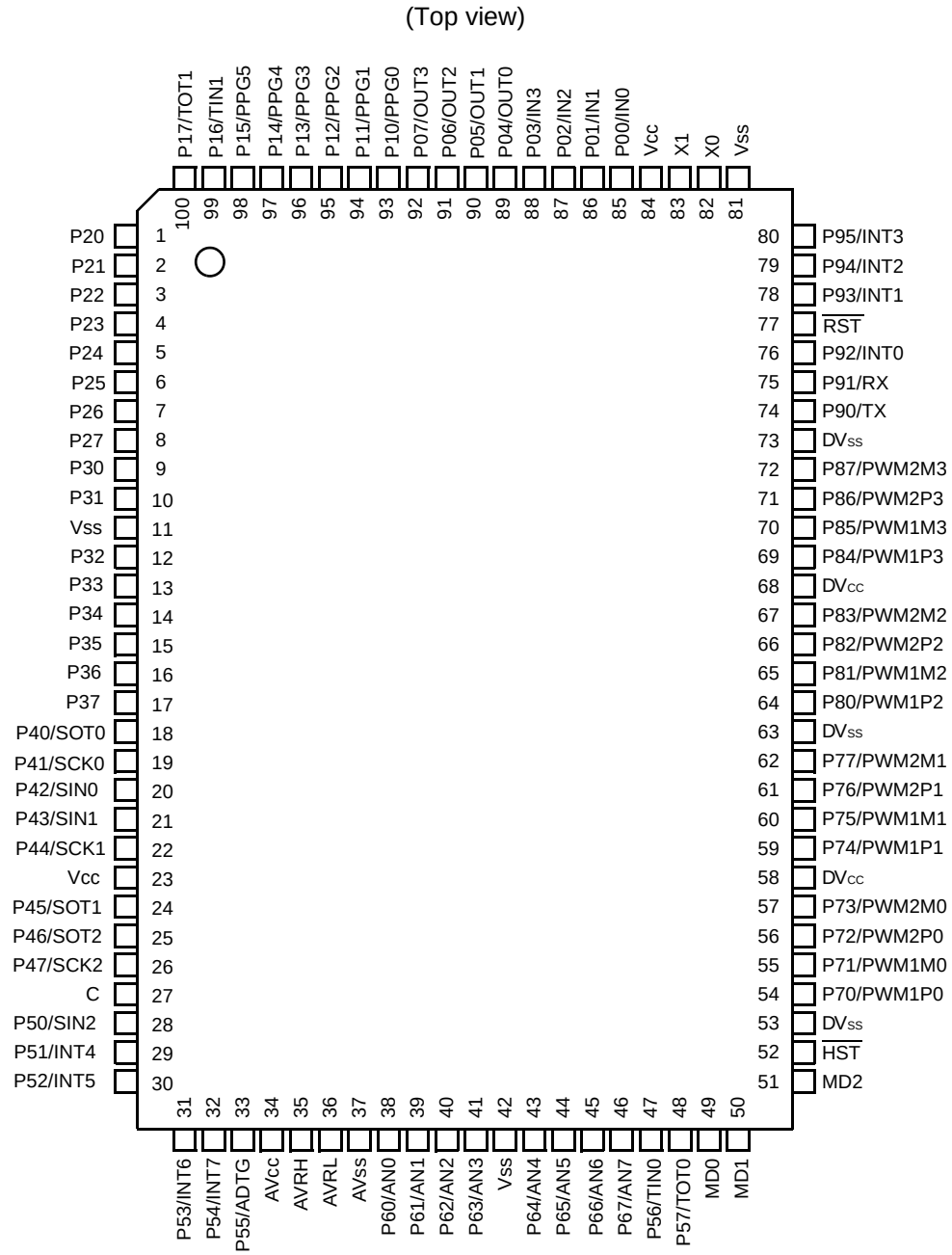
Features	MB90598	MB90F598/F598G	MB90V595/V595G
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90xxx:TSEG2 ≥ RSJW+2TQ MB90xxxG:TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm ™ and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/clock timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	+5 V±10 %		
Package	QFP-100		PGA-256

*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")

■ PIN ASSIGNMENT



(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{RST}$	B	Reset input
52	$\overline{HST}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

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Pin no.	Pin name	Circuit type	Function
28	P50	D	General purpose IO
	SIN2		SIN Input for the Serial IO
29 to 32	P51 to P54	D	General purpose IO
	INT4 to INT7		External interrupt input for INT4 to INT7
33	P55	D	General purpose IO
	ADTG		Input for the external trigger of the A/D Converter
38 to 41	P60 to P63	E	General purpose IO
	AN0 to AN3		Inputs for the A/D Converter
43 to 46	P64 to P67	E	General purpose IO
	AN4 to AN7		Inputs for the A/D Converter
47	P56	D	General purpose IO
	TIN0		TIN input for the 16-bit Reload Timer 0
48	P57	D	General purpose IO
	TOT0		TOT output for the 16-bit Reload Timer 0
54 to 57	P70 to P73	F	General purpose IO
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepper Motor Controller channel 0
59 to 62	P74 to P77	F	General purpose IO
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepper Motor Controller channel 1
64 to 67	P80 to P83	F	General purpose IO
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepper Motor Controller channel 2
69 to 72	P84 to P87	F	General purpose IO
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepper Motor Controller channel 3
74	P90	D	General purpose IO
	TX		TX output for CAN Interface
75	P91	D	General purpose IO
	RX		RX input for CAN Interface

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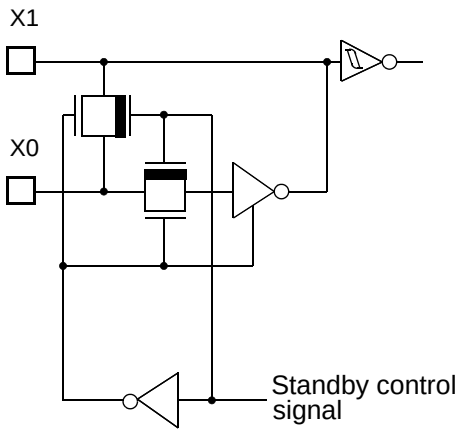
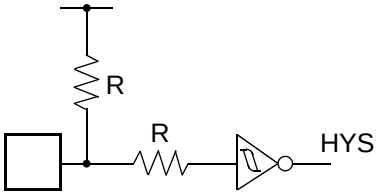
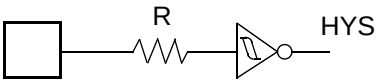
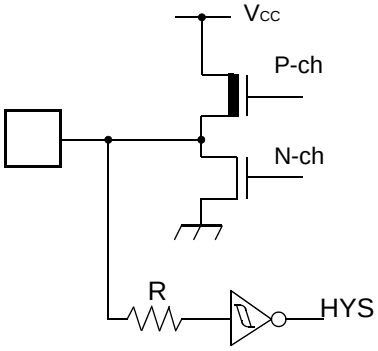
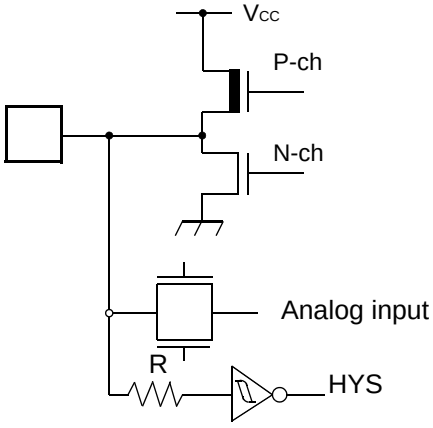
Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V_{CC} or V_{SS}.
51	MD2	H	Operating mode selection input pin. This pin should be connected to V_{CC} or V_{SS}.
27	C	—	External capacitor pin. A capacitor of 0.1µF should be connected to this pin and V_{SS}.
23, 84	V_{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V_{SS}	Power supply	Ground pins (0.0 V).

■ I/O CIRCUIT TYPE

Circuit Type	Circuit	Remarks
A		• Oscillation feedback resistor: 1 MΩ approx.
B		• Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		• Hysteresis input
D		• CMOS output • CMOS Hysteresis input
E		• CMOS output • CMOS Hysteresis input • Analog input

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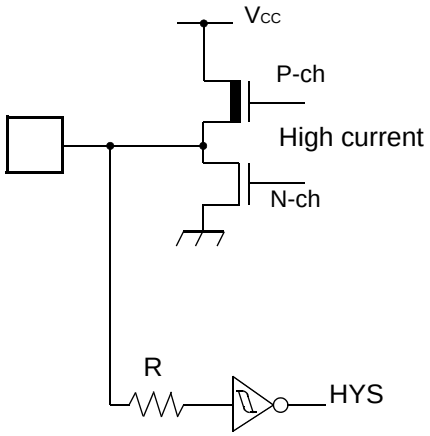
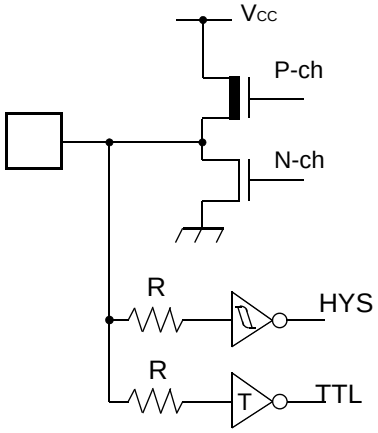
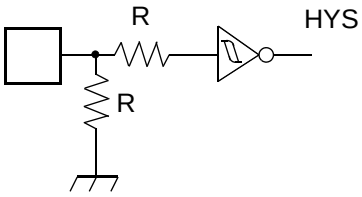
Circuit Type	Circuit	Remarks
F		• CMOS high current output • CMOS Hysteresis input
G		• CMOS output • CMOS Hysteresis input • TTL input (MB90F598/F598G, only in Flash mode)
H		• Hysteresis input Pull-down Resistor: 50 Ω approx. (except MB90F598/F598G)

■ HANDLING DEVICES

(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.
When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.
In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

(2) Treatment of Unused Pins

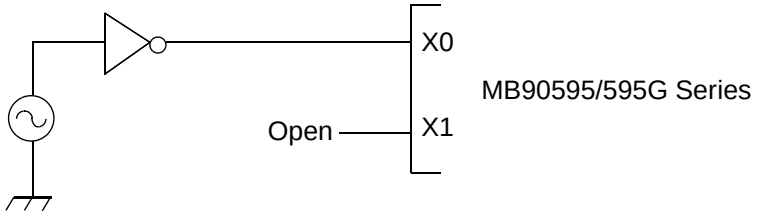
Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

Using external clock

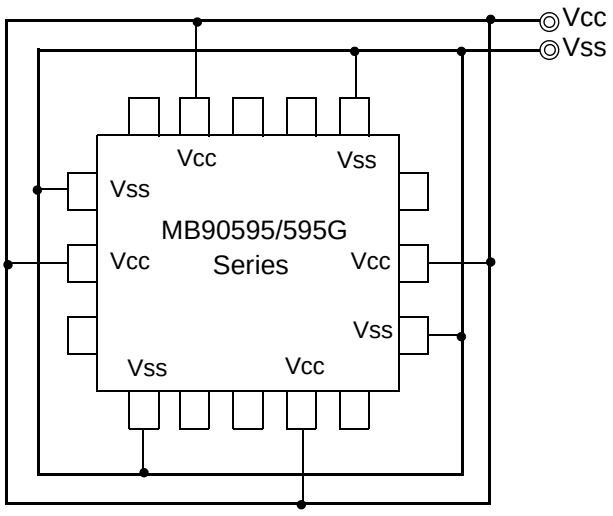


(4) Power supply pins (Vcc/Vss)

In products with multiple V_{cc} or V_{ss} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect V_{cc} and V_{ss} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 µF between V_{cc} and V_{ss} pins near the device.



(5) Pull-up/down resistors

The MB90595 Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(10) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

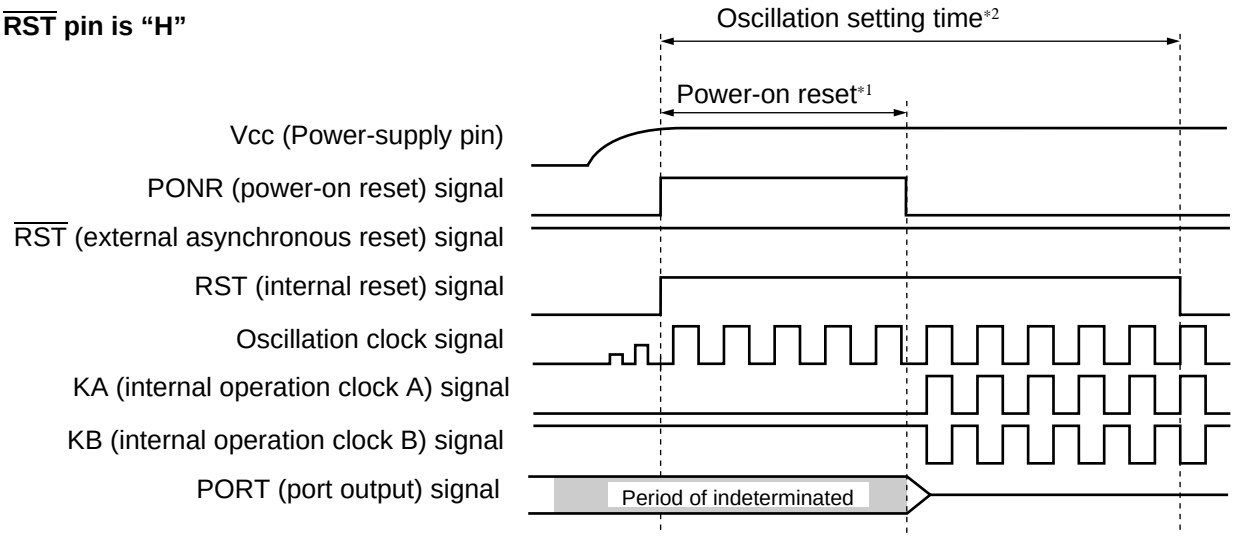
(11) Indeterminate outputs from ports 0 and 1

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

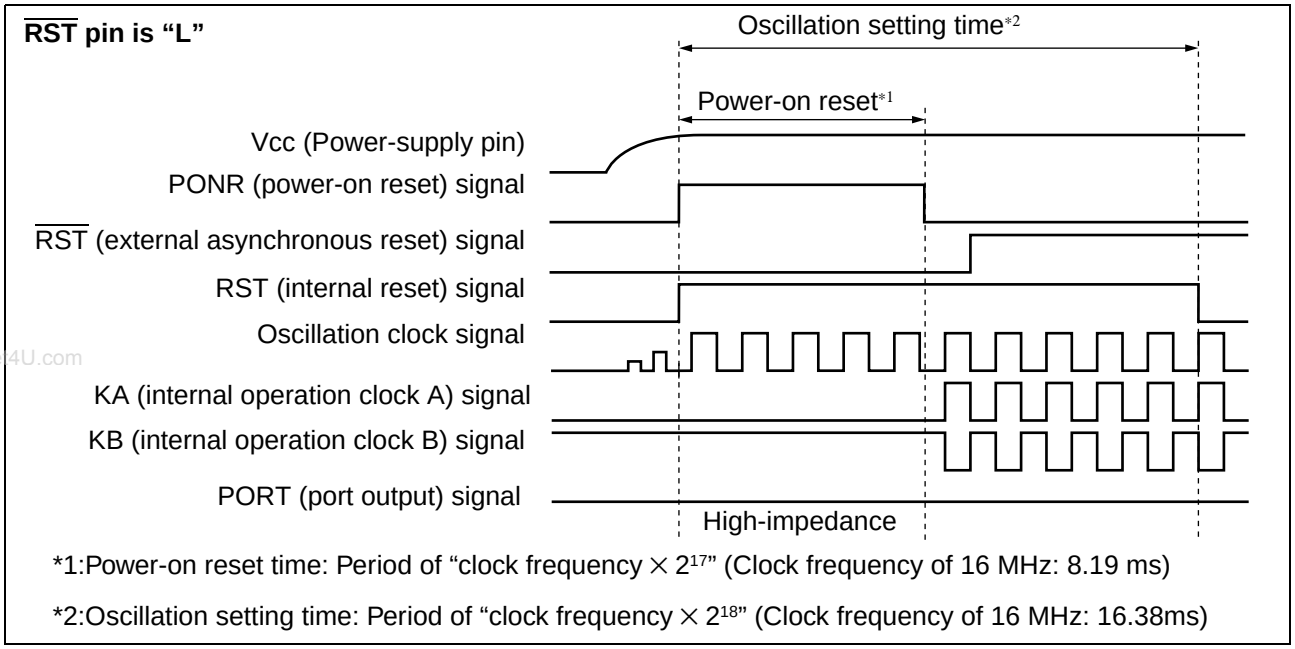
Pay attention to the port output timing shown as follow.

$\overline{RST}$ pin is “H”



*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)



*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

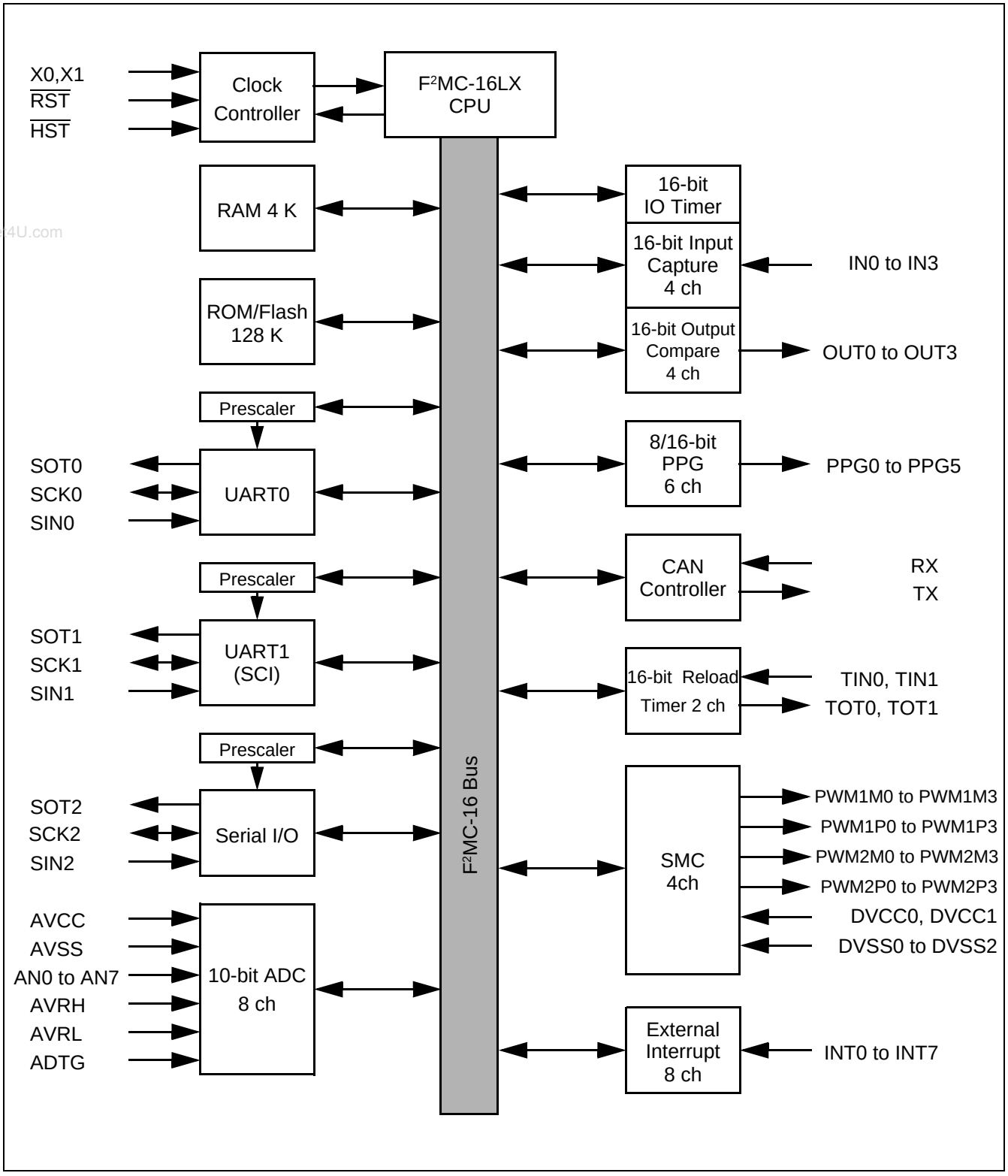
In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

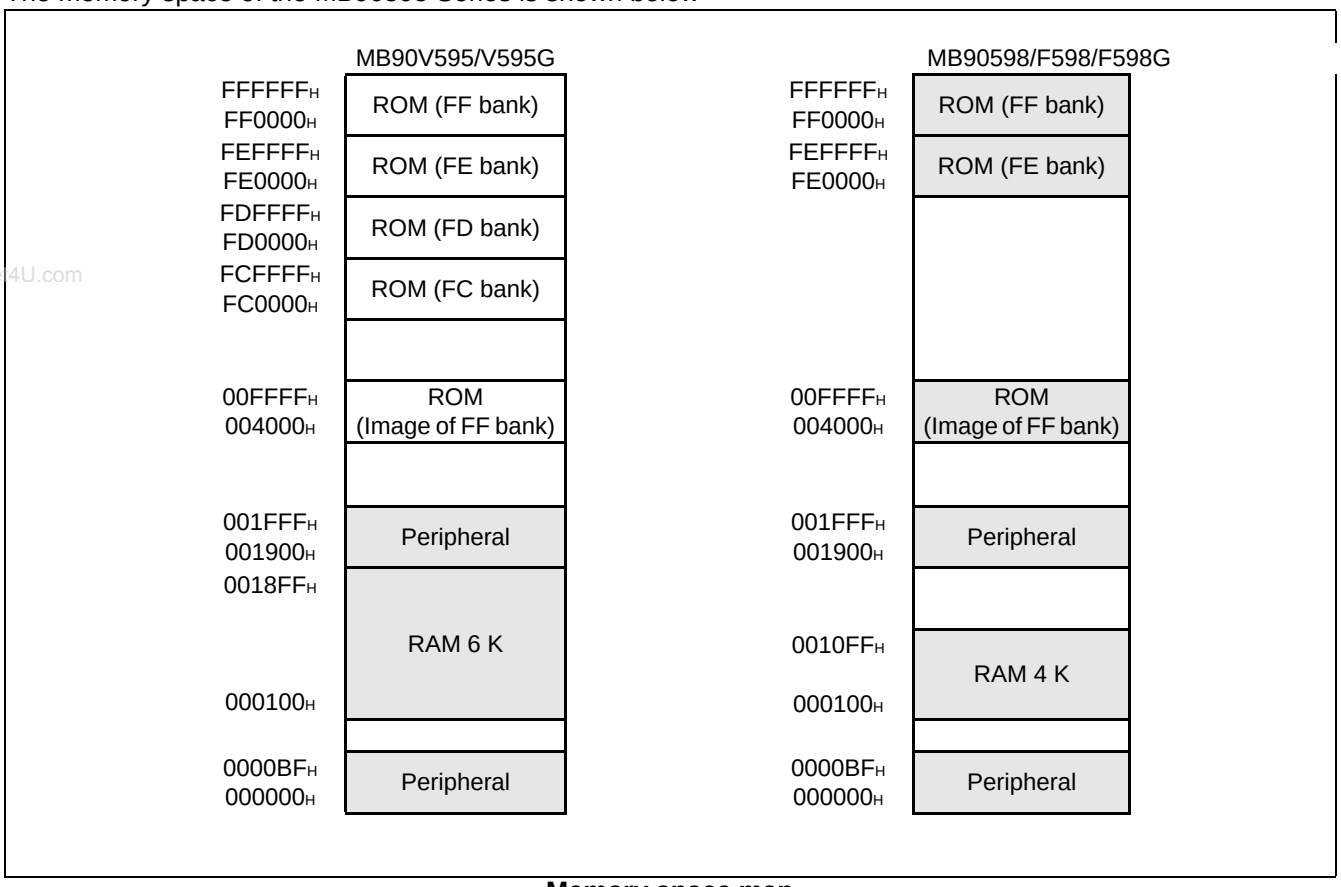
The use of EI^2OS is not possible with the REALOS real time operating system.

■ BLOCK DIAGRAM



■ MEMORY SPACE

The memory space of the MB90595 Series is shown below



Memory space map

Note: The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access $00C000_H$, the contents of the ROM at $FFC000_H$ are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at $FF4000_H$ to $FFFFFF_H$ looks, therefore, as if it were the image for 004000_H to $00FFFF_H$. Thus, it is recommended that the ROM data table be stored in the area of $FF4000_H$ to $FFFFFF_H$.

■ I/O MAP

Address	Register	Abbreviation	Access	Peripheral	Initial value
00H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
01H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
02H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
03H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
04H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
05H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
06H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
07H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
08H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
09H	Port 9 Data Register	PDR9	R/W	Port 9	_ _ XXXXXXB
0AH to 0FH	Reserved				
10H	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0B
11H	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0B
12H	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0B
13H	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0B
14H	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0B
15H	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0B
16H	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0B
17H	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0B
18H	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0B
19H	Port 9 Direction Register	DDR9	R/W	Port 9	_ _ 0 0 0 0 0 0B
1AH	Reserved				
1BH	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1B
1CH to 1FH	Reserved				
20H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0B
21H	Serial status Register 0	USR0	R/W		0 0 0 1 0 0 0 0B
22H	Serial Input/Output Data Register 0	UIDR0/ UODR0	R/W		XXXXXXXXB
23H	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 0 XB
24H	Serial Mode Register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0B
25H	Serial Control Register 1	SCR1	R/W		0 0 0 0 0 1 0 0B
26H	Serial Input/Output Data Register 1	SIDR1/ SODR1	R/W		XXXXXXXXB
27H	Serial Status Register 1	SSR1	R/W		0 0 0 0 1 _ 0 0B
28H	UART1 Prescaler Control Register	U1CDCR	R/W		0 _ _ _ 1 1 1 1B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
29H to 2AH	Reserved				
2BH	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1B
2CH	Serial Mode Control Register (low-order)	SMCS	R/W		_ _ _ _ 0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector	SES	R/W		_ _ _ _ _ _ _ 0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _B
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _B
4BH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
4C$_H$	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1$_B$
4D$_H$	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 0 1$_B$
4E$_H$	PPGA, B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 _ _$_B$
4F$_H$	Reserved				
50$_H$	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0$_B$
51$_H$	Timer Control Status Register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0$_B$
52$_H$	Timer 0/Reload Register 0	TMR0/ TMRLR0	R/W		XXXXXXXX$_B$
53$_H$	Timer 0/Reload Register 0	TMR0/ TMRLR0	R/W		XXXXXXXX$_B$
54$_H$	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0$_B$
55$_H$	Timer Control Status Register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0$_B$
56$_H$	Timer Register 1/Reload Register 1	TMR1/ TMRLR1	R/W		XXXXXXXX$_B$
57$_H$	Timer Register 1/Reload Register 1	TMR1/ TMRLR1	R/W		XXXXXXXX$_B$
58$_H$	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0$_B$
59$_H$	Output Compare Control Status Register 1	OCS1	R/W		_ _ _ 0 0 0 0 0$_B$
5A$_H$	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0$_B$
5B$_H$	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0$_B$
5C$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0$_B$
5D$_H$	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0$_B$
5E$_H$	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0$_B$
5F$_H$	Reserved				
60$_H$	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0$_B$
61$_H$	Reserved				
62$_H$	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0$_B$
63$_H$	Reserved				
64$_H$	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0$_B$
65$_H$	Reserved				
66$_H$	Timer Data Register (low-order)	TCDT	R/W	IO Timer	0 0 0 0 0 0 0 0$_B$
67$_H$	Timer Data Register (high-order)	TCDT	R/W		0 0 0 0 0 0 0 0$_B$
68$_H$	Timer Control Status Register	TCCS	R/W		0 0 0 0 0 0 0 0$_B$
69$_H$ to 6E$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F$_H$	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1$_B$
70$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
71$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
72$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
73$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
74$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
75$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
76$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
77$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
78$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
79$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
7A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
7B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
7C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
7D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
7E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
7F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
80$_H$ to 8F$_H$	CAN Controller. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (MB90F598/F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
B0H	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
B1H	Interrupt Control Register 01	ICR01	R/W		0 0 0 0 0 1 1 1B
B2H	Interrupt Control Register 02	ICR02	R/W		0 0 0 0 0 1 1 1B
B3H	Interrupt Control Register 03	ICR03	R/W		0 0 0 0 0 1 1 1B
B4H	Interrupt Control Register 04	ICR04	R/W	Interrupt controller	0 0 0 0 0 1 1 1B
B5H	Interrupt Control Register 05	ICR05	R/W		0 0 0 0 0 1 1 1B
B6H	Interrupt Control Register 06	ICR06	R/W		0 0 0 0 0 1 1 1B
B7H	Interrupt Control Register 07	ICR07	R/W		0 0 0 0 0 1 1 1B
B8H	Interrupt Control Register 08	ICR08	R/W		0 0 0 0 0 1 1 1B
B9H	Interrupt Control Register 09	ICR09	R/W		0 0 0 0 0 1 1 1B
BAH	Interrupt Control Register 10	ICR10	R/W		0 0 0 0 0 1 1 1B
BBH	Interrupt Control Register 11	ICR11	R/W		0 0 0 0 0 1 1 1B
BCH	Interrupt Control Register 12	ICR12	R/W		0 0 0 0 0 1 1 1B
BDH	Interrupt Control Register 13	ICR13	R/W		0 0 0 0 0 1 1 1B
BEH	Interrupt Control Register 14	ICR14	R/W		0 0 0 0 0 1 1 1B
BFH	Interrupt Control Register 15	ICR15	R/W		0 0 0 0 0 1 1 1B
C0H to FFH	Reserved				
1900H	Reload Register L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXXB
1901H	Reload Register H	PRLH0	R/W		XXXXXXXXB
1902H	Reload Register L	PRLL1	R/W		XXXXXXXXB
1903H	Reload Register H	PRLH1	R/W		XXXXXXXXB
1904H	Reload Register L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXXB
1905H	Reload Register H	PRLH2	R/W		XXXXXXXXB
1906H	Reload Register L	PRLL3	R/W		XXXXXXXXB
1907H	Reload Register H	PRLH3	R/W		XXXXXXXXB
1908H	Reload Register L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXXB
1909H	Reload Register H	PRLH4	R/W		XXXXXXXXB
190AH	Reload Register L	PRLL5	R/W		XXXXXXXXB
190BH	Reload Register H	PRLH5	R/W		XXXXXXXXB
190CH	Reload Register L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXXB
190DH	Reload Register H	PRLH6	R/W		XXXXXXXXB
190EH	Reload Register L	PRLL7	R/W		XXXXXXXXB
190FH	Reload Register H	PRLH7	R/W		XXXXXXXXB

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Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload Register L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload Register H	PRLH8	R/W		XXXXXXXXB
1912H	Reload Register L	PRLL9	R/W		XXXXXXXXB
1913H	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914H	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload Register H	PRLHA	R/W		XXXXXXXXB
1916H	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1917H	Reload Register H	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1929H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
192AH	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
192BH	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
192C$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
192D$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
192E$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
192F$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1930$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Controller. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Controller. Refer to section about CAN Controller				
1C00$_H$ to 1EFF$_H$	Reserved				
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX$_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX$_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX$_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX$_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX$_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

Note: Initial value of "_" represents unused bit; "X" represents unknown value.
Addresses in the rage 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading "X", and any write access should not be performed.

■ CAN CONTROLLER

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbit/s to 2 Mbit/s (when input clock is at 16 MHz)

List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000081H				
000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000083H				
000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000085H				
000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000087H				
000088H	Receive complete register	RCR	R/W	00000000 00000000B
000089H				
00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00008BH				
00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00008DH				
00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00008FH				
001B00H	Control status register	CSR	R/W, R	00---000 0----0-1B
001B01H				
001B02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
001B03H				
001B04H	Receive/transmit error counter	RTEC	R	00000000 00000000B
001B05H				
001B06H	Bit timing register	BTR	R/W	-1111111 11111111B
001B07H				

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Address	Register	Abbreviation	Access	Initial Value
001B08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
001B09H				
001B0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
001B0BH				
001B0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
001B0DH				
001B0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
001B0FH				
001B10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
001B11H				
001B12H				XXXXXXXX XXXXXXXXB
001B13H				
001B14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
001B15H				
001B16H				XXXXX--- XXXXXXXXB
001B17H				
001B18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
001B19H				
001B1AH				XXXXX--- XXXXXXXXB
001B1BH				

List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
001A00H to 001A1FH	General-purpose RAM	--	R/W	XXXXXXXXB to XXXXXXXXB
001A20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
001A21H				
001A22H				XXXXX--- XXXXXXXXB
001A23H				
001A24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
001A25H				
001A26H				XXXXX--- XXXXXXXXB
001A27H				
001A28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
001A29H				
001A2AH				XXXXX--- XXXXXXXXB
001A2BH				
001A2CH	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXXB
001A2DH				
001A2EH				XXXXX--- XXXXXXXXB
001A2FH				
001A30H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXXB
001A31H				
001A32H				XXXXX--- XXXXXXXXB
001A33H				
001A34H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXXB
001A35H				
001A36H				XXXXX--- XXXXXXXXB
001A37H				
001A38H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXXB
001A39H				
001A3AH				XXXXX--- XXXXXXXXB
001A3BH				
001A3CH	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXXB
001A3DH				
001A3EH				XXXXX--- XXXXXXXXB
001A3FH				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001A40H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXXB
001A41H				
001A42H				XXXXX--- XXXXXXXXB
001A43H				
001A44H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXXB
001A45H				
001A46H				XXXXX--- XXXXXXXXB
001A47H				
001A48H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXXB
001A49H				
001A4AH				XXXXX--- XXXXXXXXB
001A4BH				
001A4CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXXB
001A4DH				
001A4EH				XXXXX--- XXXXXXXXB
001A4FH				
001A50H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXXB
001A51H				
001A52H				XXXXX--- XXXXXXXXB
001A53H				
001A54H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXXB
001A55H				
001A56H				XXXXX--- XXXXXXXXB
001A57H				
001A58H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXXB
001A59H				
001A5AH				XXXXX--- XXXXXXXXB
001A5BH				
001A5CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXXB
001A5DH				
001A5EH				XXXXX--- XXXXXXXXB
001A5FH				

List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H				
001A62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H				
001A64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H				
001A66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H				
001A68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H				
001A6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH				
001A6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH				
001A6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH				
001A70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H				
001A72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H				
001A74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H				
001A76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H				
001A78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H				
001A7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH				
001A7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH				
001A7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH				
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

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Address	Register	Abbreviation	Access	Initial Value
001A88H to 001A8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
001A90H to 001A97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
001A98H to 001A9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
001AA0H to 001AA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
001AA8H to 001AAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
001AB0H to 001AB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
001AB8H to 001ABFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
001AC0H to 001AC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
001AC8H to 001ACFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
001AD0H to 001AD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
001AD8H to 001ADFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
001AE0H to 001AE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
001AE8H to 001AEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
001AF0H to 001AF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
001AF8H to 001AFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

■ INTERRUPT MAP

Interrupt source	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	——	——
INT9 instruction	N/A	# 09	FFFFD8$_H$	——	——
Exception	N/A	# 10	FFFFD4$_H$	——	——
CAN RX	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN TX/NS	N/A	# 12	FFFFCC$_H$		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
Time Base Timer	N/A	# 14	FFFFC4$_H$		
16-bit Reload Timer 0	*1	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/10-bit A/D Converter	*1	# 16	FFFFBC$_H$		
I/O Timer	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4$_H$		
Serial I/O	*1	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC$_H$		
Input Capture 0	*1	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	# 22	FFFFA4$_H$		
Output Compare 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
8/16-bit PPG 2/3	N/A	# 24	FFFF9C$_H$		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Input Capture 1	*1	# 26	FFFF94$_H$		
8/16-bit PPG 4/5	N/A	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 1	*1	# 28	FFFF8C$_H$		
8/16-bit PPG 6/7	N/A	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2	*1	# 30	FFFF84$_H$		
8/16-bit PPG 8/9	N/A	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 2	*1	# 32	FFFF7C$_H$		
Input Capture 3	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
8/16-bit PPG A/B	N/A	# 34	FFFF74$_H$		
Output Compare 3	*1	# 35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	# 36	FFFF6C$_H$		
UART 0 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	# 38	FFFF64$_H$		
UART 1 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Note:
- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.

- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} – 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Clamp Current	I_{CLAMP}	–2.0	2.0	mA	
“L” level max. output current	I_{OL1}	—	15	mA	Normal output *3
“L” level avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level max. output current	I_{OL2}	—	40	mA	High current output *3
“L” level avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level max. overall output current	$\sum I_{OL2}$		330	mA	Total high current output
“L” level avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level avg. overall output current	$\sum I_{OLAV2}$		250	mA	Total high current output, average value *5
“H” level max. output current	I_{OH1}	—	–15	mA	Normal output *3
“H” level avg. output current	I_{OHAV1}	—	–4	mA	Normal output, average value *4
“H” level max. output current	I_{OH2}	—	–40	mA	High current output *3
“H” level avg. output current	I_{OHAV2}	—	–30	mA	High current output, average value *4
“H” level max. overall output current	$\sum I_{OH1}$	—	–100	mA	Total normal output
“H” level max. overall output current	$\sum I_{OH2}$	—	–330	mA	Total high current output
“H” level avg. overall output current	$\sum I_{OHAV1}$	—	–50	mA	Total normal output, average value *5
“H” level avg. overall output current	$\sum I_{OHAV2}$	—	–250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598/F598G
			400	mW	MB90598
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1: AV_{CC}, AVRL and AVRL does not exceed V_{CC} and AVRL does not exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

Note: Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40	—	+85	°C	

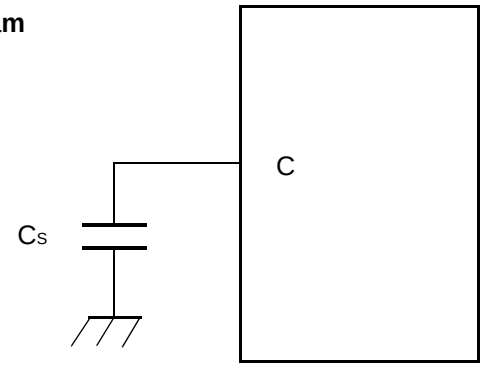
*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

- **C Pin Connection Diagram**



3. DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} +0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} +0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} +0.3	V	
Output H voltage	V_{OH1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output H voltage	V_{OH2}	P70 to P87	V_{CC} = 4.5 V, I_{OH2} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OL2}	P70 to P87	V_{CC} = 4.5 V, I_{OL2} = 30.0 mA	—	—	0.5	V	
Input leak current	I_{IL}		V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	5	µA	
Power supply current *	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At normal operating	—	35	60	mA	MB90598
				—	50	90	mA	MB90F598
				—	40	60	mA	MB90F598G
	I_{CCS}		V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	—	11	18	mA	
	I_{CTS}		V_{CC} = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	—	0.3	0.6	mA	
	I_{CCH}		V_{CC} = 5.0 V±10%, At stop, T_A = 25°C	—	—	20	µA	
	I_{CCH2}		V_{CC} = 5.0 V±10%, At Hardware stand-by mode, TA = 25°C	—	—	20	µA	MB90598 MB90F598
				—	50	100	µA	MB90F598G
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	

*: Current values are tentative and subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock.

4. AC Characteristics

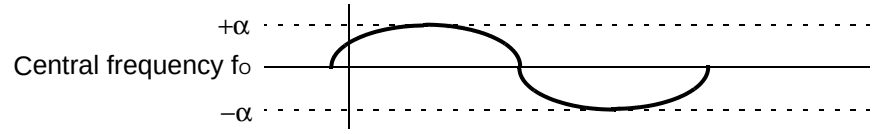
(1) Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

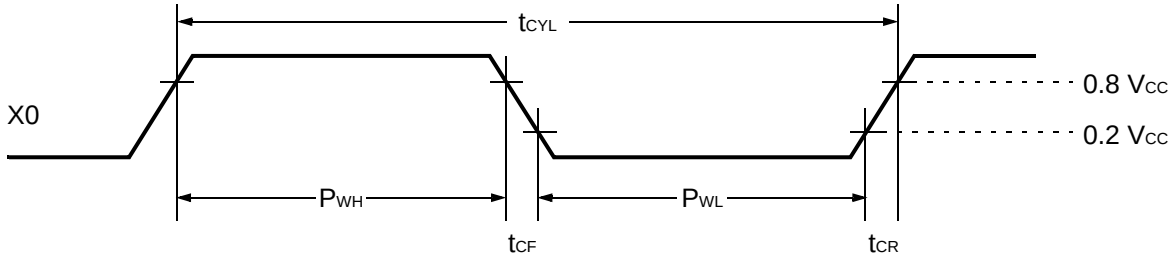
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using an oscillation circuit
			3		16	MHz	When using an external clock
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using an oscillation circuit
			62.5		333	ns	When using an external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

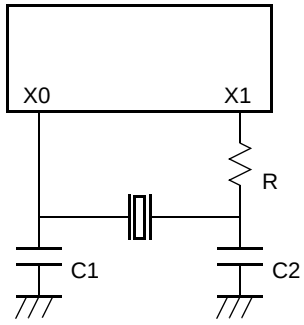
$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



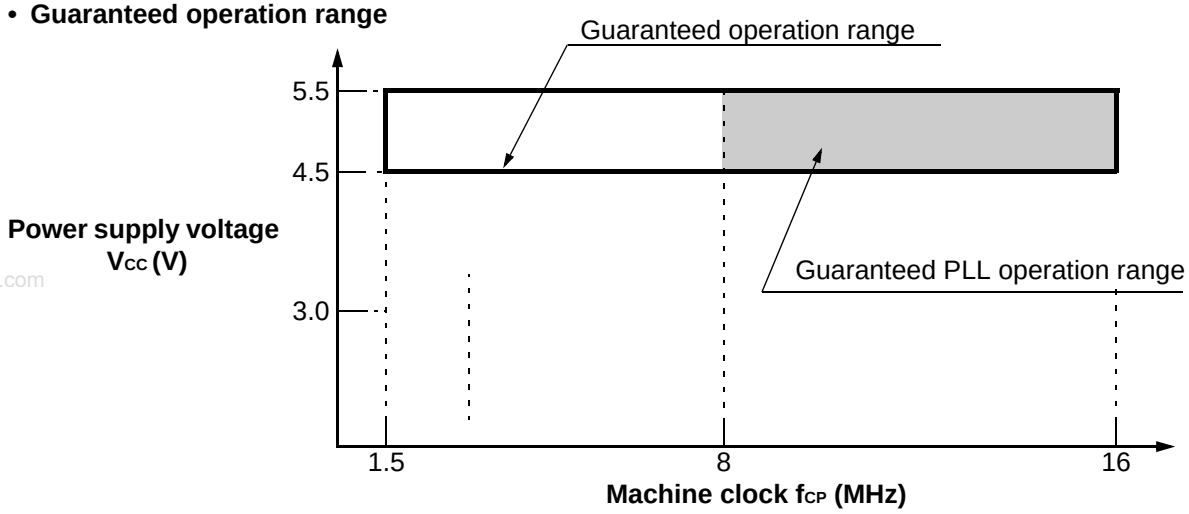
- **Clock Timing**



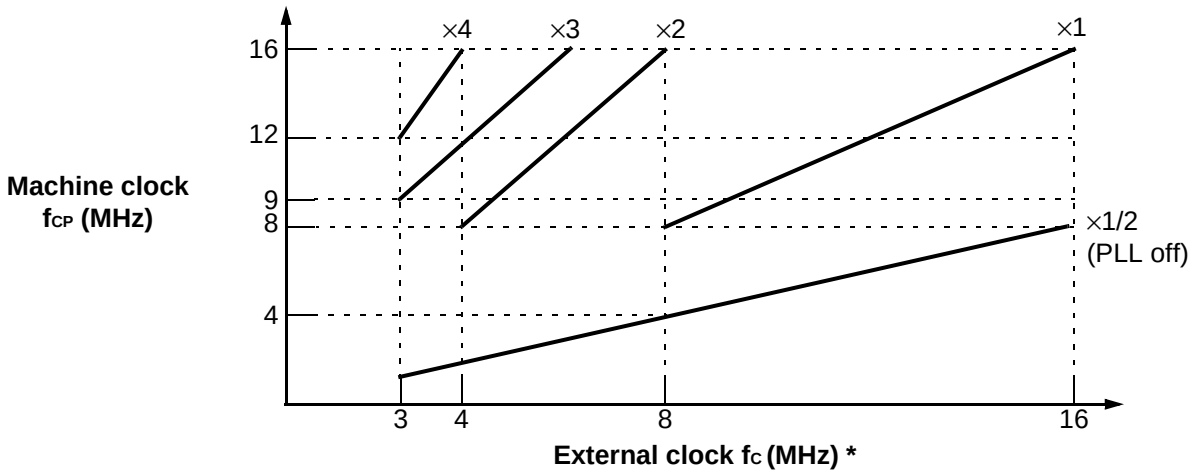
Example of Oscillation circuit



- **Guaranteed operation range**



- **External clock frequency and machine clock frequency**

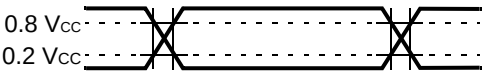


*: When using the oscillation circuit, the maximum oscillation clock frequency is 5 MHz.

AC characteristics are set to the measured reference voltage values below.

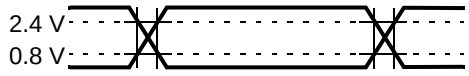
- **Input signal waveform**

Hysteresis Input Pin



- **Output signal waveform**

Output Pin



(2) Reset and Hardware Standby Input

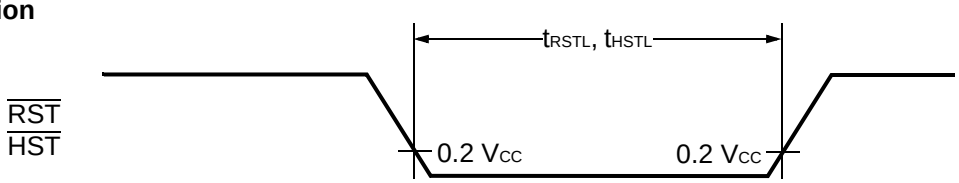
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode

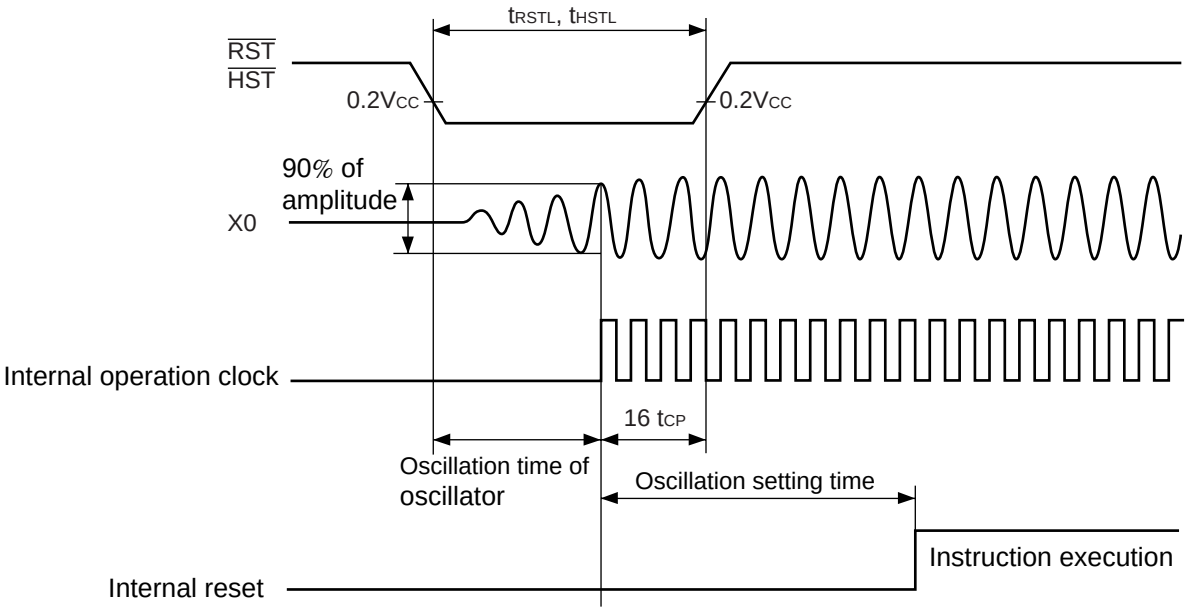
*1: "t_{cp}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

Under Normal Operation



In Stop Mode



(3)Power On Reset

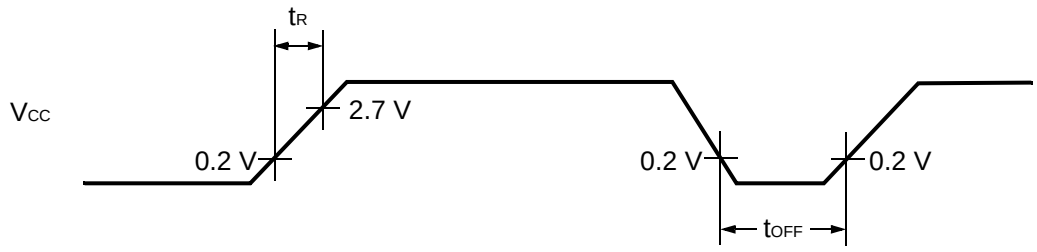
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

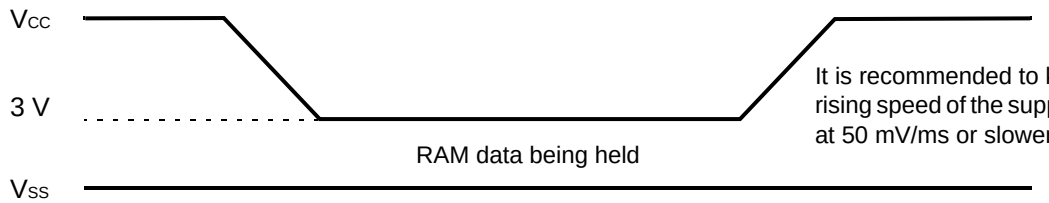
*: V_{CC} must be kept lower than 0.2 V before power-on.

Note: • The above values are used for creating a power-on reset.

• Some registers in the device are initialized only upon a power-on reset. To initialize these register, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

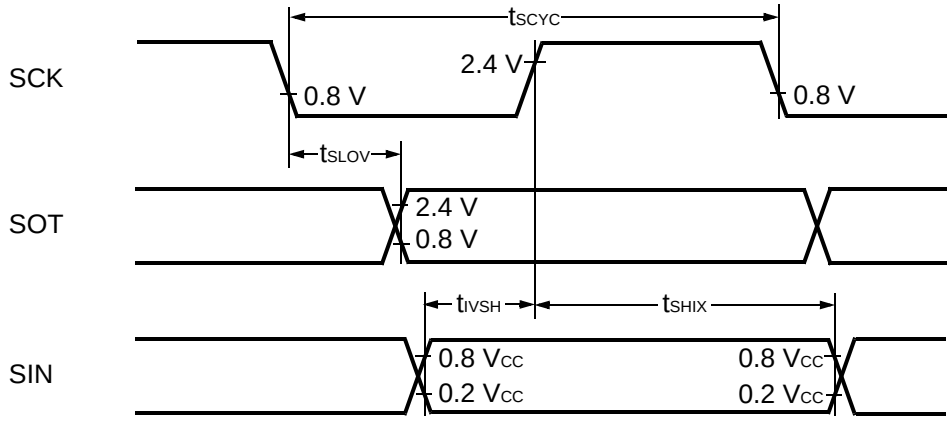
(4) UART0/1, Serial I/O Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

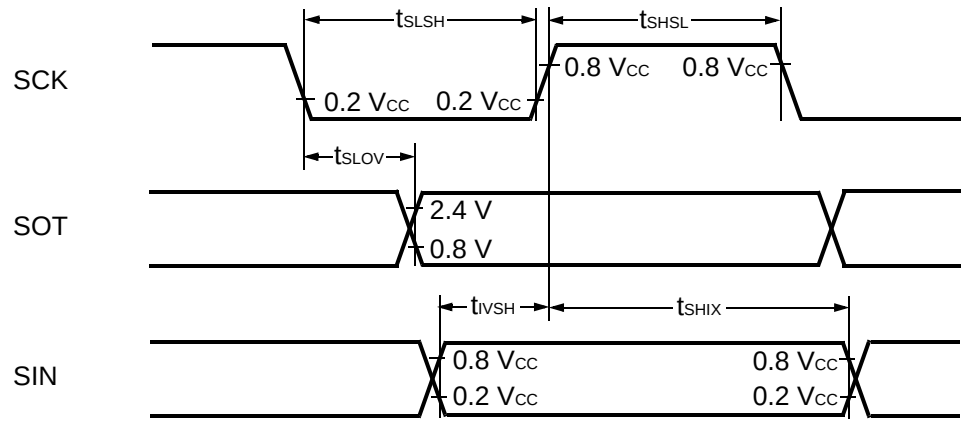
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Note: 1. AC characteristic in CLK synchronized mode.
2. C_L is load capacity value of pins when testing.
3. t_{CP} is the machine cycle (Unit: ns).

- **Internal Shift Clock Mode**



• **External Shift Clock Mode**

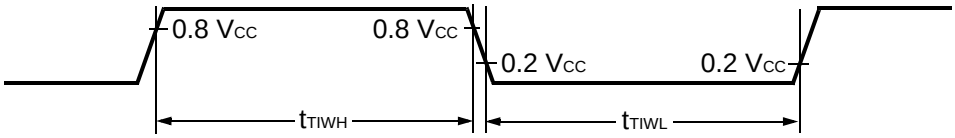


(5) Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN3					

• **Timer Input Timing**

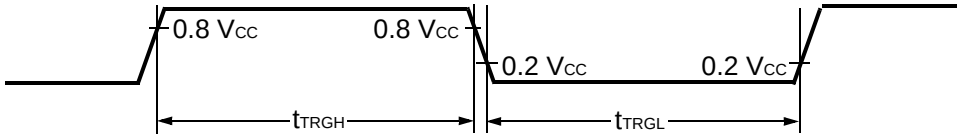


(6) Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under normal operation
				1	—	µs	In stop mode

- **Trigger Input Timing**



(7) Slew Rate High Current Outputs

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

- Slew Rate Output Timing

$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

5. A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0 V,3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5	AVRL +0.5	AVRL + 4.5	mV	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5	AVRH − 1.5	AVRH + 1.5	mV	
Conversion time	—	—	—	352t_{CP}	—	ns	
Sampling time	—	—	—	64t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	−10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V595 MB90V595G MB90F598 MB90F598G
			—	140	600	µA	MB90598
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

*: When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

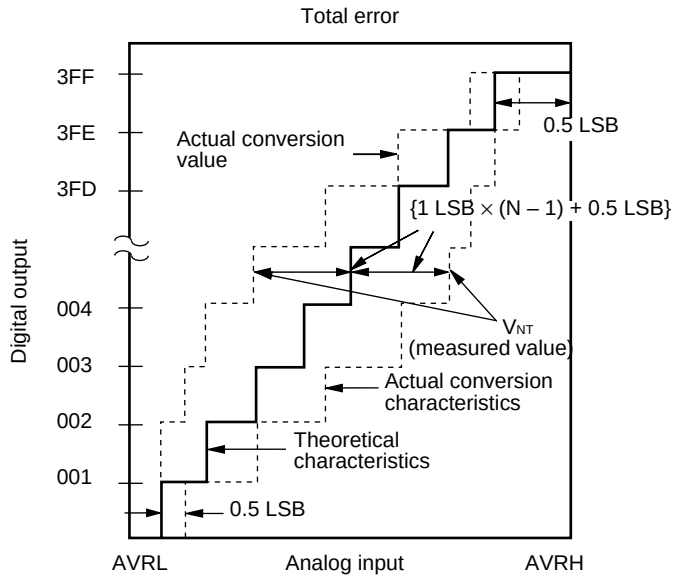
6. A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

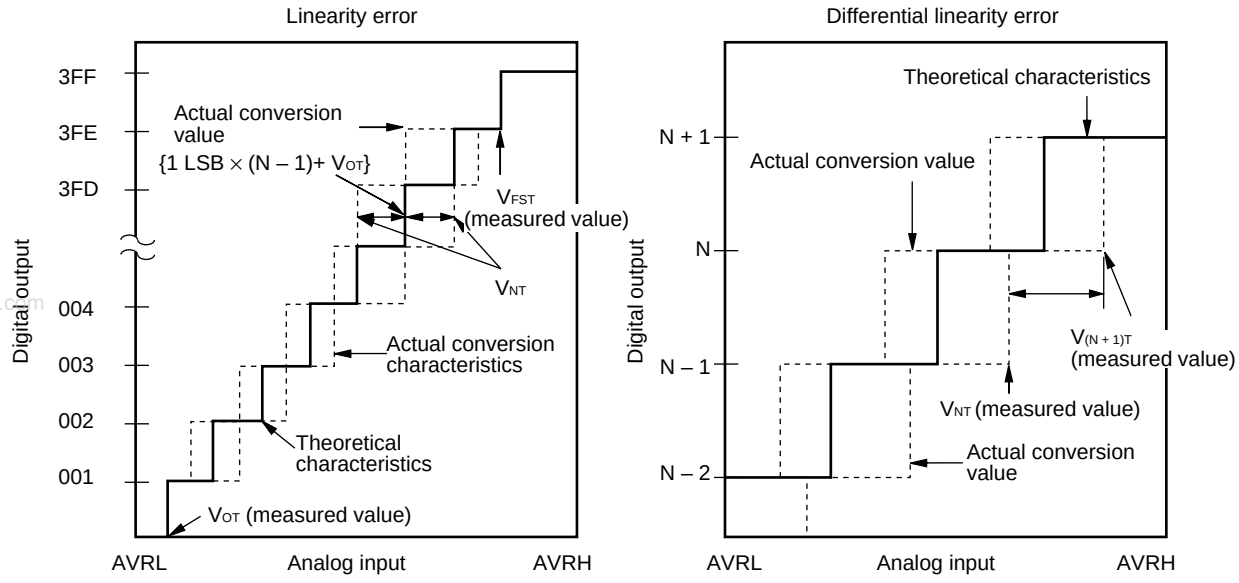
V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

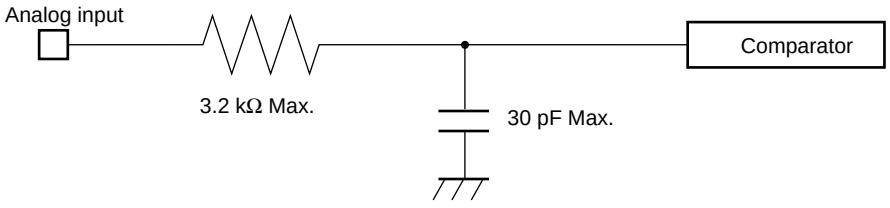
7. Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions, :

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 µs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**



- **Error**

The smaller the | AVRH – AVRL |, the greater the error would become relatively.

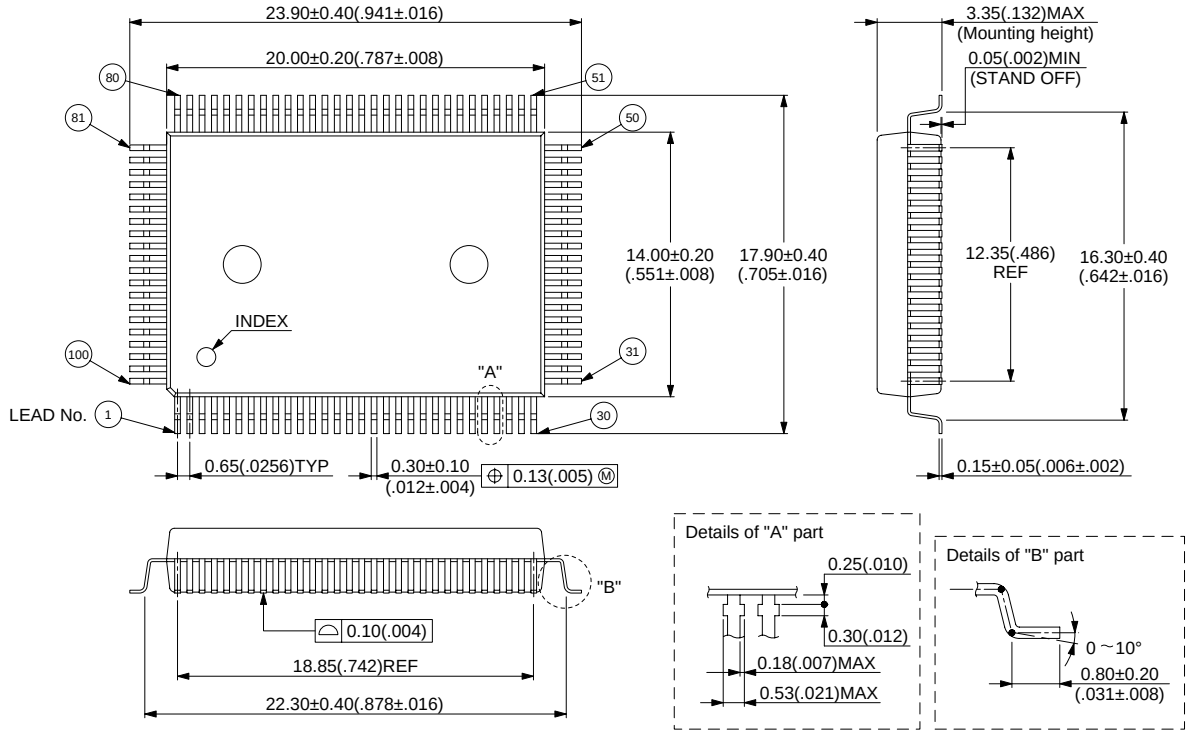
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90598PF MB90F598PF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595CR MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

■ PACKAGE DIMENSION

100-pin plastic QFP
(FPT-100P-M06)

Note: This package dimension is for the reference. Please consult separately about a formal version.



Dimensions in mm (inches)

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