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CCD Image Sensors

IL-C3/IL-C4 TURBOSENSOR™

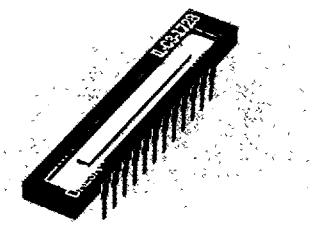
IL-C3/IL-C4 Linear Image Sensor Arrays

T-41-55

DALSA INC

FEATURES

- **60 MHz Effective Data Rate**
- **14μm (H) x 14μm (V) Pixel Size**
- **Photodiode Photoelements**
- **Electronic Shutter for Exposure Control**
- **128 to 2048 Elements**
- **Antiblooming**



DESCRIPTION

DALSA's IL-C3/C4 linear CCD image sensors use TURBOSENSOR™ technology to provide data rates of 30 MHz per output for an effective output rate of 60 MHz. The series is ideally suited for high speed, high performance applications, and employs buried channel CCD shift registers to maximize output speed and reduce noise. Dual outputs are used to maximize readout times. The dynamic range of the photoelements on the IL-C3 series exceeds 5,000:1 and provides output which is linear for all light levels. White reference signals can be generated on both outputs, providing a reference level or an end-of-frame function. Exposure control is incorporated to allow integration times shorter than the readout times if desired. All sensors in both series are functionally equivalent and pin-for-pin compatible. Support electronics designed for the IL-C4 series can also operate the C3 series sensors.

APPLICATIONS

The IL-C3/C4 series are ideally suited for applications requiring maximum speed and high resolution. The IL-C4-2048 provides over 400 points-per-inch resolution across five inches.

DALSA also offers the CL-Cx line scan cameras which utilize the IL-C3/C4 sensors for:

- **High Performance Document Scanning**
- **Inspection**
- **Bar Code Scanning**
- **Gauging and Measurement**

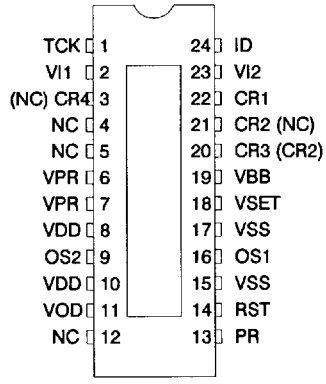
For mechanical information regarding package size and tolerance, refer to package #50-01-24005 in **Optical and Mechanical Considerations of Sensors** on pp. 101-104 of this databook.

IL-C4 SERIES PIN FUNCTIONAL DESCRIPTION

NOTE: Please consult factory for pinouts on all sensors that do not have a "B" suffix on the part number.

PIN	SYMBOL	NAME - IL-C4 Series
1	TCK	Transfer Clock
2	VI1	White Reference Input 1
3	CR4	Readout Clock, Phase 4
4,5,12	NC	No Connection
6,7	VPR	Pixel Reset Bias
8,10	VDD	Amplifier Supply Voltage
9	OS2	Output Signal 2, Even Pixels
11	VOD	Output Drain Bias Voltage
13	PR	Pixel Reset Clock
14	RST	Output Reset Clock
15,17	VSS	Ground Reference
16	OS1	Output Signal 1, Odd Pixels
18	VSET	Output Node Set Voltage
19	VBB	Substrate Bias Voltage
20	CR3	Readout Clock, Phase 3
21	CR2	Readout Clock, Phase 2
22	CR1	Readout Clock, Phase 1
23	VI2	White Reference Input 2
24	ID	Electrical Reference Diode Input

B Version



10-00048

IL-C3 PINOUT VARIATIONS

3, 21	NC	No connection
20	CR2	Readout Clock, Phase 2

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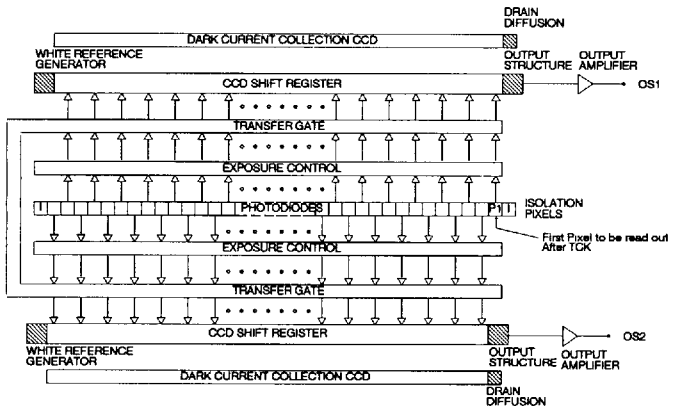
IL-C3/C4 IMAGE SENSOR BLOCK DIAGRAM



PACKAGE

PIN 1 Location

12-00045

2

FUNCTIONAL DESCRIPTION

PHOTOELEMENTS

The IL-C3 sensors consist of a line of 128, 256, 512 or 1728 pixels which are 14μm square for a photosensitive area of 196 square micrometers and 1:1 height to width aspect ratio. Two phase CCD shift registers are employed. The IL-C4 offer 1024 or 2048 photoelements with four phase CCD shift registers to improve Charge Transfer Efficiency (CTE) for the longer array lengths. The same photoelement is incorporated into both the IL-C3 and IL-C4 series.

The TURBOSENSOR™ photoelement offers ultra high speed operation and responds linearly with respect to input light intensity. An electronic shutter (PR, VPR) exists for exposure control and blooming suppression.

TRANSFER GATE

This gate controls the flow of light generated signal charge from the photoelements into the CCD shift registers. Electrons from the photoelement are transferred when a high potential (equal to the high clock voltage) is applied to the transfer gate. A single input to the device (TCK) controls the transfer gate for both the even and odd pixels.

CCD SHIFT REGISTERS

Two buried channel CCD signal transport shift registers, one on each side of the line of photoelements, are used to maximize speed, improve charge transfer efficiency and reduce noise. Alternate signal charge packets are transferred to the inner pair of transport CCD shift registers and serially shifted towards the output structure.

The use of bilinear CCD shift registers increases the effective data rate to 60 MHz by providing access to even and odd photoelements simultaneously. In addition to the signal transport CCDs, two outer CCD shift registers provide protection to the inner shift registers from peripherally generated electron noise thereby reducing noise.

WHITE REFERENCES

A white reference signal can be created in the last element of the CCD shift registers to be read out. Generation is controlled by the input signals VI1, VI2, and ID. Adjustment of the VI1 and VI2 voltages can provide approximately 0 - 150% of the maximum video output signal. Many applications disable this feature to provide a dark reference.

OUTPUT STRUCTURE

The signal charge packets from the transport shift registers are transferred serially from the CR1 phase, over the SET gate (VSET bias), to a floating sensing diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier structure, producing an output signal voltage (OS1 or OS2). The floating sensing diffusion is cleared of signal charge by the reset gate, driven by the reset clock (RST) in preparation for the subsequent signal charge packet.

RECOMMENDED DC OPERATION

SIGNAL NAMES

The signal names assigned to the package pins describe both the function of the pin as well as the sense of input signals. DC (unclocked) bias and supply voltages are designated with signal names beginning with "V". Clocked signals begin with any other letter and are representative of the function of the pin.

SUPPLY VOLTAGES

VDD provides operating current to the on chip output amplifier and hence should be well regulated. The substrate, or bulk bias voltage, VBB, is negative with respect to ground in some applications. This low current bias should be well regulated. Since protection diodes are provided between many clock lines and the substrate, no clocks can be permitted to go below VBB. A negative VBB can reduce charge injection.

OUTPUT BIAS

A high impedance DC gate bias, VSET, controls transfer of signal charge onto the output sensing diffusion. This voltage should be adjusted externally to optimize output structure operation. If VSET is not optimized, single bright pixels (or a white reference pixel) will appear to "bleed" into adjacent pixels and could be mistaken for very poor CTE or crosstalk.

The shift register output drain voltage, VOD, is a bias provided to the output structure to discharge signal electrons after sensing. This voltage can be fixed at VDD.

WHITE REFERENCE BIAS

The white reference generator uses two high impedance DC biases, VI1 and VI2, to produce a reference output pixel. Adjustment of the relative voltages of VI1 and VI2 via resistive dividers will allow the user to set the white reference output equal to the maximum output voltage.

The VI2 potential should be higher than the VI1 potential in order to create a white reference. To create a dark reference or to disable the white reference the VI2 potential should be lower than the VI1 potential.

PHOTOELEMENT BIAS

VPR is a high impedance DC bias that is used to reset the photoelements when exposure control is used. If VPR is too high a loss of low light level sensitivity will occur. If VPR is too low the photodetectors will appear to saturate even under dark conditions. VPR can be set by a resistive divider. When exposure control is disabled, VPR can be connected to VDD.

IL-C3/C4 DC OPERATING CONDITIONS

Recommended Operating Conditions at Tp = 25°C. (See notes)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Amplifier supply voltage	14.0	15.0	16.0	V
VBB	Substrate voltage	-3.0	-0.5	0.0	V
VOD	Shift register drain voltage	14.0	15.0	16.0	V
VI1	White Reference Input 1	0.0	3.0	12.0	V
V12	White Reference Input 2	0.0	6.0	12.0	V
VSET (IL-C3)	Set Voltage	2.0	5.5	12.0	V
VSET (IL-C4)	Set Voltage	2.0	3.0	12.0	V
VPR	Pixel Reset Bias	0.0	12.0	15.0	V

NOTES:

(1) Voltages with respect to ground (VSS).
(2) Tp is defined as the package temperature.

IL-C3/IL-C4 TURBOSENSOR™

RECOMMENDED CLOCK OPERATION

PHOTOELEMENTS

Signal charge electrons are photogenerated during the exposure period, which is set by the time between the high to low transition of the Pixel Reset Clock (PR) and the following high to low transition of the transfer pulse (TCK). Signal charge is integrating when PR and TCK are low. Exposure control is achieved by adjusting the time duration of the high level on PR. Antiblooming can be obtained by returning the PR clock to a positive potential for its low period. A reasonable of level of antiblooming occurs when the low potential of PR is approximately 4 volts. When TCK is pulsed high the pixel data is transferred into the first phase (CR1) of the CCD readout shift register. If exposure control is used, the rising edge of PR should follow the falling edge of TCK. If exposure control is not desired, PR should be connected to ground.

TRANSPORT CLOCKS

Four phase transport clocks (CR1-CR4) are required for the IL-C4 series. All transport clocks can be operated at 50% duty cycle continuously. CR1 and CR3 are complementary, non-overlapping as are CR2 and CR4. The IL-C3 series employs 2 phase transport clocks (CR1, CR2). These are complementary signals at 50% duty cycle. The clock high voltages can be set by the user for the specific application. In general, higher clock voltages will provide better CTE and higher operating speeds; however, power dissipation on the device will increase due to an increase in C dV/dt current to the clocks. Power dissipation must be considered for the larger arrays, especially the 2048 element device. It is recommended that the rising and falling edges of the transport clocks have rise/fall times of approximately 1/6 of the clock period.

TRANSFER CLOCK

The transfer clock (TCK) controls the transfer of signal from the pixels into the CCD shift register (CR1). The high voltage on this clock line should be equal to the high voltage on the transport clocks. The TCK low voltage can be brought as far negative as VBB.

WHITE REFERENCE

The one clock required for reference pulse generation is ID, and is active low. This pulse occurs at the same time as the TCK pulse. If electrical reference output is not required, ID should be maintained at a high DC voltage (VDD).

OUTPUT CONTROL CLOCKS

One output structure clock (RST) is required to clear the output node after sensing. This clock should go to a high voltage equal to the transport clock (CR) high voltages, and to a low of VSS. During RST high, the outputs (OS1 and OS2) will go to a reset level as shown in the clock diagrams.

OUTPUT SIGNALS

The output signals OS1 and OS2 provide video data for the odd and even pixels, respectively. The frequency of OS1 and OS2 is equal to the frequency of the RST clock. Current buffering of the output video signals is recommended. The AC signal rides on a DC offset. AC coupling is recommended to eliminate the DC offset.

IL-C3/C4 CLOCK CHARACTERISTICS

Recommended Operating Conditions at Tp = 25°C.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VH(CR)	Transport clock HIGH	8.0	12.0	15.0	V
VL(CR)	Transport clock LOW	0.0	0.0	0.5	V
VH(TCK)	Transfer clock HIGH	7.0	12.0	15.0	V
VL(TCK)	Transfer clock LOW	0.0	0.0	0.5	V
VH(ID)	Input Diode clock HIGH	8.0	12.0	15.0	V
VL(ID)	Input Diode clock LOW	0.0	0.0	0.5	V
VH(RST)	Reset clock HIGH	7.0	12.0	15.0	V
VL(RST)	Reset clock LOW	0.0	0.0	0.5	V
VH(PR)	Pixel reset clock HIGH	8.0	12.0	15.0	V
VL(PR)	Pixel reset clock LOW	VBB	0.0	12.0	V
f(RST)	Reset freq.(per output rate)		15	30	MHz
f (DATA)	Data freq. (effective data rate)		30	60	MHz

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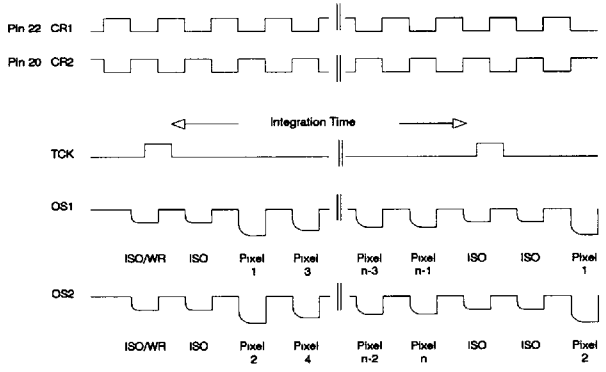
IL-C3 OVERALL CLOCKING

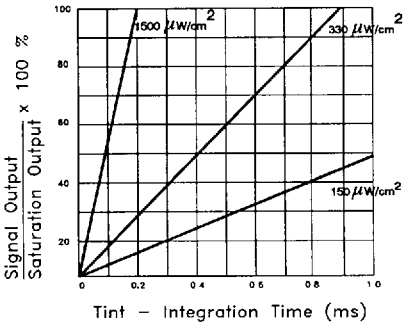


NOTES
1) n = number of photoelements in the array
2) Clocking is shown for (n/2 + 2) CR1 pulses between TCK pulses
3) Simplified clocking is shown for RST = CR1, with White Reference and Pixel Reset disabled.

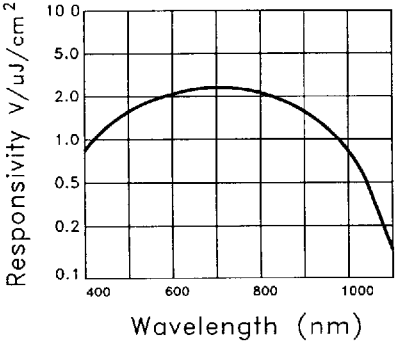
Please contact DALSA for further options on clock timing.

11-00074

IL-C3/C4 PERFORMANCE MEASUREMENTS



Output vs. Integration Time



Spectral Response

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IL-C4 PERFORMANCE CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C. (See notes).				
Dynamic range[1]		10,000:1		
Noise Equivalent Exposure (NEE)		60		pJ/cm²
Saturation Equivalent Exposure (SEE)[2]		600		nJ/cm²
Responsivity[2]		2.5		V/μJ/cm²
Saturation Output Amplitude (V_{SAT})[3]		1500		mV
V_{NOISE}[4]				
Peak-Peak		0.8		mV
RMS		0.16		mV
FPN (exposure control disabled)		5.0		mV
FPN (exposure control enabled)		10.0		mV
PRNU (exposure control disabled)[5]		5		% V_{SAT}
PRNU (exposure control enabled)[5]		15		% V_{SAT}
CTE[6]	0.99990	0.99999	0.999999	
White Reference Amplitude[3]		250		mV
DC Output Offset	7	9	12	V
DC Balance		100		mV
Output Gain Mismatch		10		% V_{SAT}
Storage Temperature (T_P)[7]	−70		+125	°C
Operating Temperature (T_P)[7]	−60		+90	°C

Notes:

1 Ratio of V_{SAT} to RMS Noise with reset noise eliminated through correlated double sampling (CDS).
2 Responsivity at peak Quantum Efficiency (near 700 nm)
3 Output amplitude with respect to dark reference level
4 Amplifier noise measured with reset noise eliminated through correlated double sampling (CDS).
5 PRNU is measured at approximately 50% V_{SAT} and is the difference between the active pixels with the lowest and highest outputs, expressed as a percentage of V_{SAT}.
6 CTE is the measurement for a one stage transfer, measured at f_{RST} = 3.75 MHz
7 Tp is package temperature.
8. Specifications are slightly different for IL-C3 sensor series

Test Conditions:

1. All tests are done at f_{RST} = 3.75 MHz, or f_{DATA} = 7.5 MHz.
2. Light Source QTH lamp with WBHM, unless otherwise noted
3. VDD, VOD = 15 V, VBB = 0 V; Clock high voltage 12 V, low voltage 0 V, (includes CRx, TCK, RST as applicable); VSET as required for maximum V_{SAT} and CTE
4. All measurements exclude first and last pixel of each output

IL-C3 ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Recommended Operating Conditions at Tp = 25°C.				
Output impedance		200		Ω
Amplifier supply current		20		mA
DC Bias Currents (VOD, VSET, VBB, VPR)			1	mA
Amplifier power dissipation	225	300	550	mW
Resistance to VBB				
Transport clock (CR1, CR2)		5		MΩ
Transfer clock		5		MΩ
Pixel Reset, Set gate		5		MΩ
Capacitance to VBB				
Transport clock (CR1, CR2)[1]		150		pF
Transfer clock (TCK)[1]		15		
Pixel Reset (PR)[1]		15		pF
Reset (RST), Set (VSET) gate		8		pF

Notes:

1 Capacitance given for 512 element array For other lengths apply the following factors 128 (0.3), 256 (0.6), 1024 (1.8), 1728 (3.0); 2048 (3.6).

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Optical and Mechanical Considerations of Sensors

Optical and Mechanical Considerations of DALSA CCD Image Sensors

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This applications note provides packaging information for the sensors listed in this databook. Please refer to the tables on the following pages for the critical dimensions of each image sensor series. For more information on a particular image sensor, please refer to the specific datasheet.

FIGURE 1. DIMENSIONS OF PACKAGE # 50-01-24005

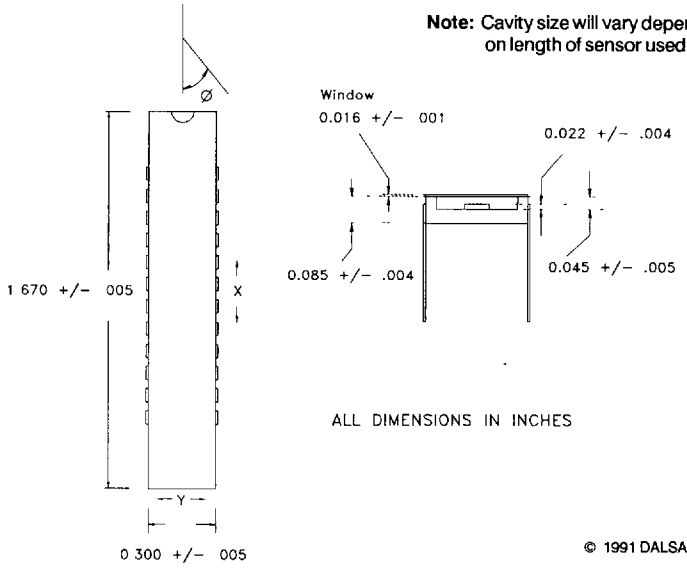

TABLE 1. PACKAGE # 50-01-24005 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-24005	IL-C3-0128	0.55 ± .09	0.15 ± .02	$0^{o} \pm 3.0^{o}$
50-01-24005	IL-C3-0256	0.55 ± .08	0.15 ± .02	$0^{o} \pm 2.5^{o}$
50-01-24005	IL-C3-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C9-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-C4-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C4-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C5-2048	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-C5-4096	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-C6-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-E1-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-E1-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-E1-2048	0.55 ± .04	0.15 ± .02	$0^{o} \pm 1.0^{o}$
50-01-24005	IL-F2-0512	0.55 ± .07	0.15 ± .02	$0^{o} \pm 2.0^{o}$
50-01-24005	IL-F2-1024	0.55 ± .05	0.15 ± .02	$0^{o} \pm 1.5^{o}$
50-01-24005	IL-F2-2048	0.55 ± .04	0 15 ± .02	$0^{o} \pm 1.0^{o}$

Note: X = center imaging area to center pin 1 along package Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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Optical and Mechanical Considerations of Sensors

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FIGURE 2. DIMENSIONS OF PACKAGE # 50-01-40003

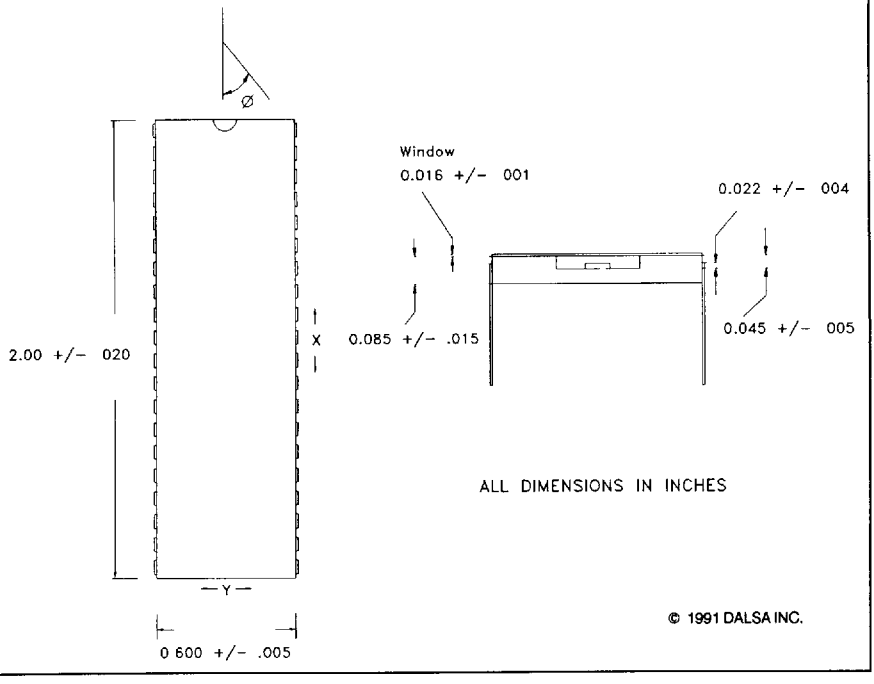

TABLE 2. PACKAGE # 50-01-40003 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40003	IT-C5-2048	0.95 ± 0.1	0.3 ± 0.05	$0^{\circ} \pm 2.5^{\circ}$
50-01-40003	IT-C5-4096	0.95 ± 0.08	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-E1-1536	0.95 ± 0.08	0.3 ± 0 05	$0^{\circ} \pm 2.0^{\circ}$
50-01-40003	IT-E1-2048	0.95 ± 0.06	0.3 ± 0.05	$0^{\circ} \pm 1.5^{\circ}$
50-01-40003	IT-F2-2048	0.95 ± 0.06	0.3 ± 0.03	$0^{\circ} \pm 1.5^{\circ}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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FIGURE 3. DIMENSIONS OF PACKAGE # 50-01-24002

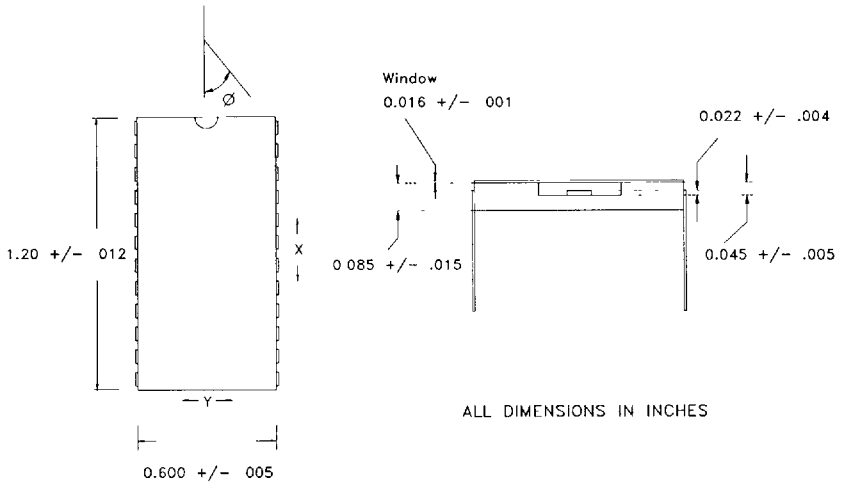

TABLE 3. PACKAGE # 50-01-40002 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-40002	IA-D1-0032	0.56 ± 0.12	0.3 ± 0.05	$0^{o} \pm 5.0^{o}$
50-01-40002	IA-D1-0064	0.57 ± 0.09	0.3 ± 0.04	$0^{o} \pm 4.0^{o}$
50-01-40002	IA-D1-0128	0.59 ± 0.12	0.3 ± 0.03	$0^{o} \pm 2.5^{o}$
50-01-40002	IA-D1-0256	0.71 ± 0.10	0.3 ± 0.03	$0^{o} \pm 1.5^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation

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FIGURE 4. DIMENSIONS OF PACKAGE # 50-01-28004

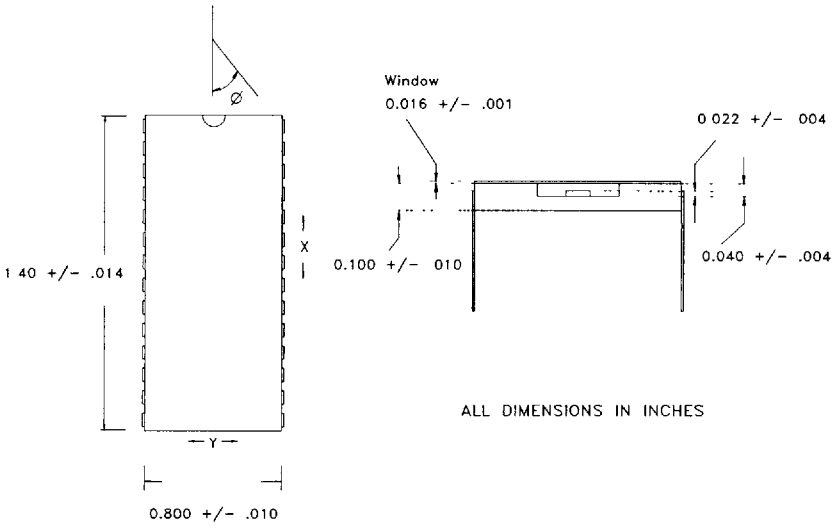

TABLE 4. PACKAGE # 50-01-28004 TYPICAL DIMENSIONS

Package #	Part	X	Y	Ø
50-01-28004	IA-D2-0512	0.65 ± 0.08	0.4 ± 0.04	$0^{o} \pm 3.0^{o}$

Note: X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation