

DATA SHEET

CBT6800

10-bit bus switch with precharged outputs
for live insertion

Product data
Supersedes data of 1999 Oct 28

2003 Sep 12

10-bit bus switch with precharged outputs for live insertion

CBT6800

FEATURES

- 5 Ω switch connection between two ports
- TTL compatible input and output levels
- Outputs are precharged by bias voltage to minimize signal distortion during live insertion
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBT6800 provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows bi-directional connections to be made while adding near-zero propagation delay. The device also precharges the B port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise.

The CBT6800 is organized as one 10-bit switch with a single enable (ON) input. When ON is low, the switch is on and port A is connected to port B. When ON is high, the switch between port A and port B is open and the B port is precharged to BIASV through the equivalent of a 10 kΩ resistor.

The CBT6800 is characterized for operation from -40 to 85 °C.

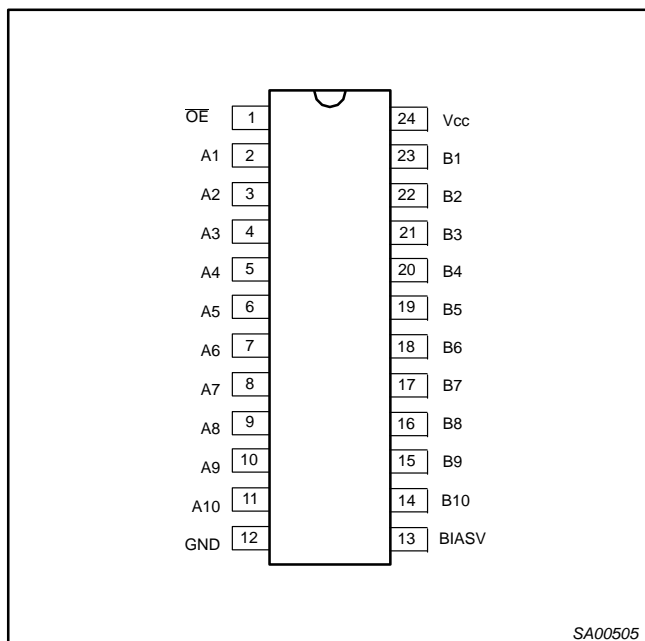
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25\text{ °C}; GND = 0\text{ V}$ | TYPICAL | UNIT |
|------------------------|---|--|---------|------|
| t_{PLH} t_{PHL} | Propagation delay An to Bn or Bn to An | $C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$ | 250 | ps |
| C_{IN} | Input capacitance - control pin | $V_I = 0\text{ V or } V_{CC}$ | 3.5 | pF |
| C_{OUT} | Output capacitance - I/O pins | Outputs disabled; $V_O = 0\text{ V or } V_{CC}$ | 8.2 | pF |
| I_{CCZ} | Total supply current | Outputs disabled; $V_{CC} = 5.5\text{ V}$ | 1 | μA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | DWG NUMBER |
|----------------------|-------------------|------------|------------|
| 24-Pin Plastic TSSOP | -40 to +85 °C | CBT6800PW | SOT355-1 |

PIN CONFIGURATION



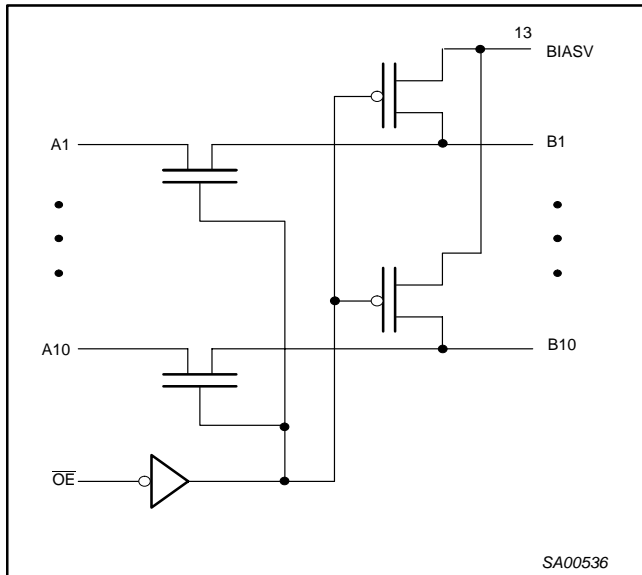
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|-----------------|--------------------------------------|
| 1 | OE | Output enable |
| 13 | BIASV | Precharge bias voltage input |
| 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | A1-A10 | A-port I/O pins |
| 23, 22, 21, 20, 19, 18, 17, 16, 15, 14 | B1-B10 | B-port I/O pins - with active pullup |
| 12 | GND | Ground (V) |
| 24 | V _{CC} | Positive supply voltage |

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LOGIC SYMBOL



FUNCTION TABLE

| \overline{OE} | B1 - B10 | FUNCTION |
|-----------------|----------|-----------|
| L | A1 - A10 | Connect |
| H | BIASV | Precharge |

H = HIGH voltage level
 L = LOW voltage level
 Z = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-----------|-------------------------------|------------|--------------|------|
| V_{CC} | DC supply voltage | | -0.5 to +7.0 | V |
| I_{IK} | DC input diode current | | -50 | mA |
| V_I | DC input voltage ³ | | -1.2 to +7.0 | V |
| I_{SW} | DC clamp diode current | $V_O < 0$ | -50 | mA |
| T_{stg} | Storage temperature range | | -65 to 150 | °C |
| BiasV | DC voltage range | | -0.5 to 6.0 | V |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|-----------|--------------------------------------|--------|----------|------|
| | | Min | Max | |
| V_{CC} | DC supply voltage | 4.5 | 5.5 | V |
| BIASV | DC supply voltage | 1.3 | V_{CC} | V |
| V_{IH} | HIGH-level input voltage | 2.0 | — | V |
| V_{IL} | LOW-level Input voltage | — | 0.8 | V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | °C |

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|-----------------|---|--|---|------------------|---------|---------------|
| | | | $T_{amb} = -40 \text{ to } +85 \text{ } ^\circ\text{C}$ | | | |
| | | | Min | Typ ¹ | Max | |
| V_{IK} | Input clamp voltage | $V_{CC} = 4.5 \text{ V}; I_I = -18 \text{ mA}$ | — | — | -1.2 | V |
| I_I | Input leakage current - \overline{OE} | $V_{CC} = 5.5 \text{ V}; V_I = \text{GND or } 5.5 \text{ V}$ | — | — | ± 5 | μA |
| I_O | Output bias current | $V_{CC} = 4.5 \text{ V}; \text{BiasV} = 2.4 \text{ V}; V_O = 0$ | 0.25 | — | — | mA |
| I_{CC} | Quiescent supply current | $V_{CC} = 5.5 \text{ V}; I_O = 0, V_I = V_{CC} \text{ or } \text{GND}$ | — | — | 50 | μA |
| ΔI_{CC} | Control pins ² | $V_{CC} = 5.5 \text{ V}$, one input at 3.4 V, other inputs at V_{CC} or GND | — | — | 2.5 | mA |
| C_I | Control pins | $V_I = 3 \text{ V or } 0$ | — | 3.5 | — | pF |
| $C_{O(OFF)}$ | Off-state capacitance - I/O pins | $V_O = 3 \text{ V or } 0$; switch off | — | 8.2 | — | pF |
| r_{on}^3 | On-resistance | $V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 64 \text{ mA}$ | — | 5 | 7 | Ω |
| | | $V_{CC} = 4.5 \text{ V}; V_I = 0 \text{ V}; I_I = 30 \text{ mA}$ | — | 5 | 7 | |
| | | $V_{CC} = 4.5 \text{ V}; V_I = 2.4 \text{ V}; I_I = 15 \text{ mA}$ | — | 10 | 15 | |
| VP | Pass gate voltage | $V_{IN} = V_{CC} = 5.0 \text{ V}, I_{OUT} = -100 \mu\text{A}$ | 3.4 | 3.6 | 3.9 | V |

NOTES:

1. All typical values are at $V_{CC} = 5 \text{ V}, T_{amb} = 25 \text{ } ^\circ\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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AC CHARACTERISTICS

GND = 0 V; $C_L = 50 \text{ pF}$; $t_r = t_f \leq 2.5 \text{ ns}$

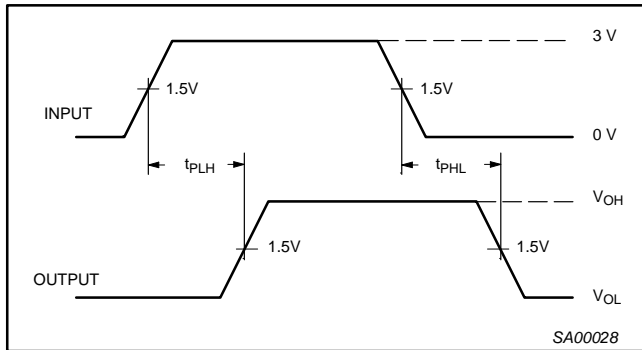
| SYMBOL | PARAMETER | FROM (INPUT) | TO (OUTPUT) | LIMITS | | UNIT |
|------------------------|--------------------------------|------------------------|-------------|---|------------|------|
| | | | | $V_{CC} = +5.0 \text{ V} \pm 0.5 \text{ V}$ | | |
| | | | | Min | Max | |
| t_{pd} | Propagation delay ¹ | A or B | B or A | — | .25 | ns |
| t_{pZH} T_{PZL} | BIASV = GND BIASV = 3 V | $\overline{\text{ON}}$ | A or B | 2.4 3.0 | 7.7 8.3 | ns |
| t_{pHZ} T_{PLZ} | BIASV = GND BIASV = 3 V | $\overline{\text{ON}}$ | A or B | 1.0 3.1 | 5.3 7.8 | ns |

NOTE:

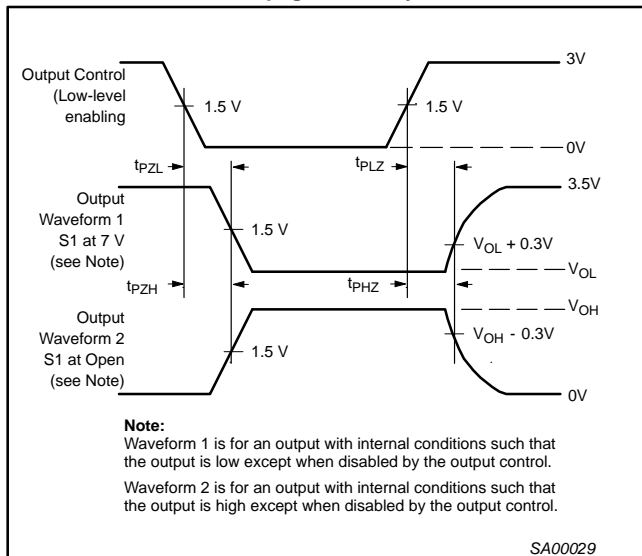
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

$V_M = 1.5 \text{ V}$, $V_{IN} = \text{GND to } 3.0 \text{ V}$

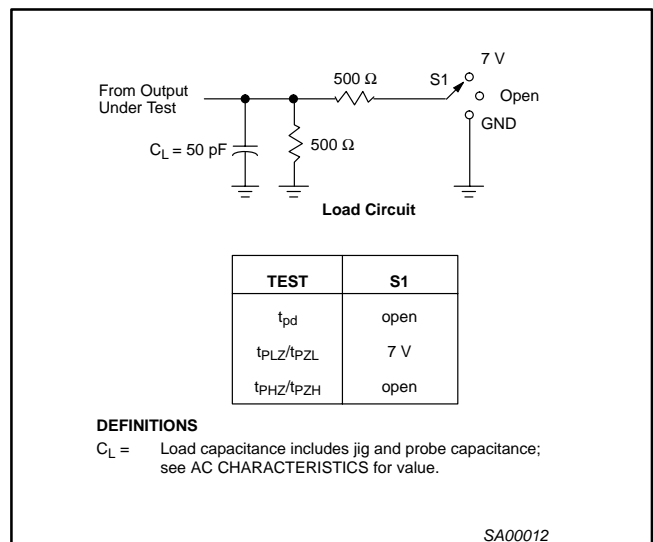


Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



NOTES:

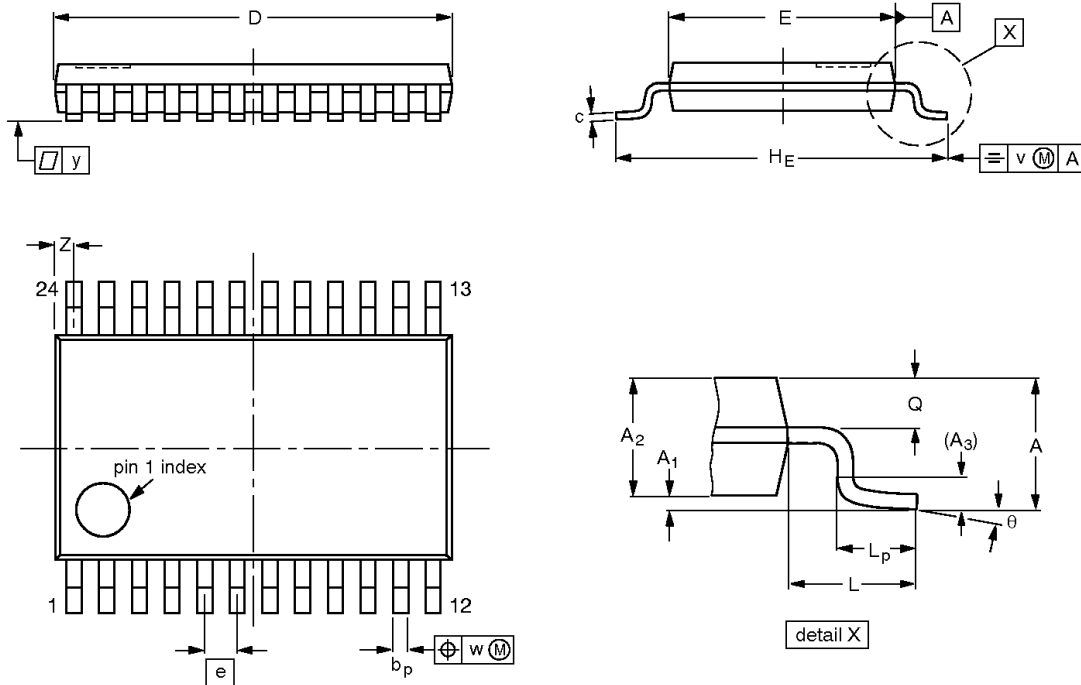
1. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
2. The outputs are measured one at a time with one transition per measurement.

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 7.9 7.7 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.5 0.2 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT355-1 | | MO-153 | | | | 99-12-27 03-02-19 |

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CBT6800**REVISION HISTORY**

| Rev | Date | Description |
|------------|-------------|--|
| _2 | 20030912 | Product data (9397 750 12059); ECN 853-2182 30126 dated 18 July 2003. Supersedes data of 28 October 1999 (9397 750 06552). Modifications: <ul style="list-style-type: none">• Corrections to block diagram drawing |
| _1 | 19991028 | Product data (9397 750 06552); ECN: 853-2182 22598 of 28 October 1999 |

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Data sheet status

| Level | Data sheet status ^[1] | Product status ^[2] [3] | Definitions |
|-------|----------------------------------|-----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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