



Multiformat 216 MHz Video Encoder with Six NSV™ 14-Bit DACs

ADV7314

FEATURES

High Definition Input Formats

8-/10-/16-/20-, 24-/30-Bit (4:2:2, 4:4:4) Parallel YCrCb

Compliant with:

- SMPTE 293M (525p)
- BTA T-1004 EDTV2 525p
- ITU-R BT.1358 (625p/525p)
- ITU-R BT.1362 (625p/525p)
- SMPTE 274M (1080i) at 30 Hz and 25 Hz
- SMPTE 296M (720p)
- RGB in 3 × 10-Bit 4:4:4 Input Format

HDTV RGB Supported:

- RGB and RGBHV
- Other High Definition Formats Using Async Timing Mode

High Definition Output Formats

- YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
- YPrPb HDTV (EIA 770.3)

RGB, RGBHV

- CGMS-A (720p/1080i)
- Macrovision Rev 1.1 (525p/625p)
- CGMS-A (525p)

Standard Definition Input Formats

CCIR-656 4:2:2 8-/10-/16-/20-Bit Parallel Input

Standard Definition Output Formats

- Composite NTSC M/N
- Composite PAL M/N/B/D/G/H/I, PAL-60
- SMPTE 170M NTSC Compatible Composite Video
- ITU-R BT.470 PAL Compatible Composite Video
- S-Video (Y/C)
- EuroScart RGB
- Component YPrPb (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1.L1
- CGMS/WSS
- Closed Captioning

GENERAL FEATURES

- Simultaneous SD and HD Inputs and Outputs
- Oversampling up to 216 MHz
- Programmable DAC Gain Control
- Sync Outputs in All Modes

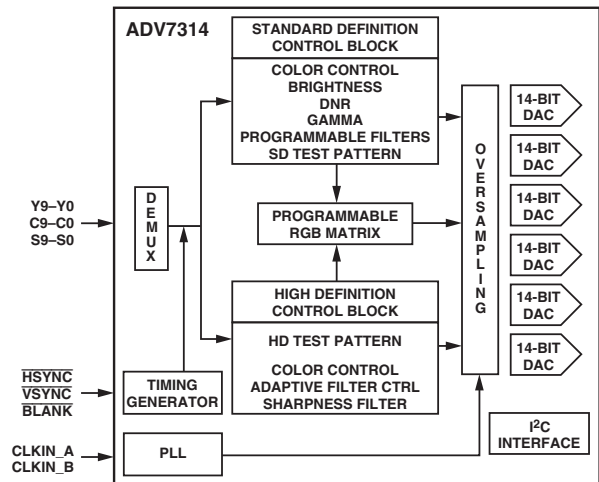
On-Board Voltage Reference

- Six 14-Bit NSV Precision Video DACs
- 2-Wire Serial I²C® Interface
- Dual Input/Output Supply 2.5 V/3.3 V Operation
- Analog and Digital Supply 2.5 V
- On-Board PLL
- 64-Lead LQFP Package
- Lead (Pb) Free Product

APPLICATIONS

- High End DVD
- High End PS DVD Recorders/Players
- SD/Prog Scan/HDTV Display Devices
- SD/HDTV Set Top Boxes
- Professional Video Systems

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV[®]7314 is a high speed, digital-to-analog encoder on a single monolithic chip. It includes six high speed NSV video D/A converters with TTL compatible inputs.

The ADV7314 has separate 8-/10-/16-/20-bit input ports that accept data in high definition and/or standard definition video format. For all standards, external horizontal, vertical and blanking signals, or EAV/SAV timing codes control the insertion of appropriate synchronization signals into the digital data stream and therefore the output signal.

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ADV7314

DETAILED FEATURES

High Definition Programmable Features (720p/1080i)

- 2× Oversampling (148.5 MHz)
- Internal Test Pattern Generator
(Color Hatch, Black Bar, Flat Field/Frame)
- Fully Programmable YCrCb to RGB Matrix
- Gamma Correction
- Programmable Adaptive Filter Control
- Programmable Sharpness Filter Control
- CGMS-A (720p/1080i)

Programmable Features (525p/625p)

- 8× Oversampling (216 MHz Output)
- Internal Test Pattern Generator
(Color Hatch, Black Bar, Flat Frame)
- Individual Y and PrPb Output Delay
- Gamma Correction
- Programmable Adaptive Filter Control
- Fully Programmable YCrCb to RGB Matrix
- Undershoot Limiter
- Macrovision Rev 1.1 (525p/625p)
- CGMS-A (525p)

Standard Definition Programmable Features

- 16× Oversampling (216 MHz)
- Internal Test Pattern Generator (Color Bars, Black Bar)
- Controlled Edge Rates for Sync, Active Video
- Individual Y and PrPb Output Delay
- Gamma Correction

Digital Noise Reduction (DNR)

Multiple Chroma and Luma Filters

Luma-SSAF™ Filter with Programmable Gain/Attenuation

PrPb SSAF

Separate Pedestal Control on Component and Composite/S-Video Outputs

VCR FF/RW Sync Mode

Macrovision Rev 7.1.L1

CGMS/WSS

Closed Captioning

Standards Directly Supported

| Resolution | Frame Rate (Hz) | Clk Input (MHz) | Standard |
|------------|-----------------|-----------------|---------------|
| 720×480 | 29.97 | 27 | ITU-R BT.656 |
| 720×576 | 25 | 27 | ITU-R BT.656 |
| 720×483 | 59.94 | 27 | SMPTE 293M |
| 720×480 | 59.94 | 27 | BTA T-1004 |
| 720×576 | 50 | 27 | ITU-R BT.1362 |
| 1280×720 | 60 | 74.25 | SMPTE 296M |
| 1920×1080 | 30 | 74.25 | SMPTE 274M |
| 1920×1080 | 25 | 74.25 | SMPTE 274M* |

Other standards are supported in Async Timing mode.

*SMPTE 274M-1998: System no.6

DETAILED FUNCTIONAL BLOCK DIAGRAM

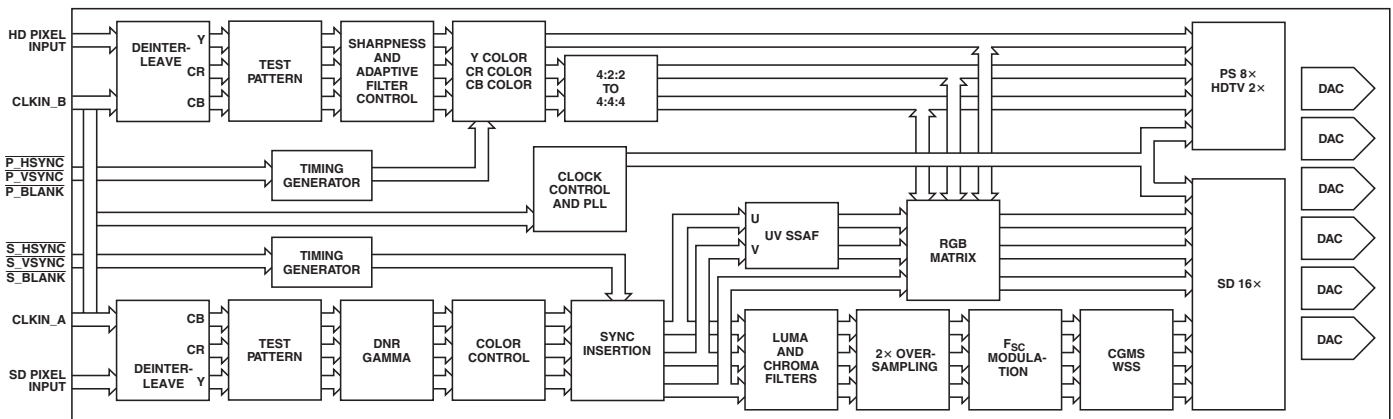


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ADV7314—SPECIFICATIONS

($V_{AA} = 2.375\text{ V} - 2.625\text{ V}$, $V_{DD} = 2.375\text{ V} - 2.625\text{ V}$; $V_{DD_IO} = 2.375\text{ V} - 3.6\text{ V}$,
 $V_{REF} = 1.235\text{ V}$, $R_{SET} = 3040\ \Omega$, $R_{LOAD} = 150\ \Omega$. All specifications T_{MIN} to T_{MAX}
(0°C to 70°C), unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions |
|--|------------------------|-----------|------------------------|---------------|--|
| STATIC PERFORMANCE¹ | | | | | |
| Resolution | | 14 | | Bits | |
| Integral Nonlinearity | | 2.0 | | LSB | |
| Differential Nonlinearity ² , +ve | | 1.0 | | LSB | |
| Differential Nonlinearity ² , -ve | | 3.0 | | LSB | |
| DIGITAL OUTPUTS | | | | | |
| Output Low Voltage, V_{OL} | | | 0.4 [0.4] ³ | V | $I_{SINK} = 3.2\text{ mA}$ $I_{SOURCE} = 400\ \mu\text{A}$ $V_{IN} = 0.4\text{ V}, 2.4\text{ V}$ |
| Output High Voltage, V_{OH} | 2.4 [2.0] ³ | | | V | |
| Three-State Leakage Current | | ± 1.0 | | μA | |
| Three-State Output Capacitance | | 2 | | pF | |
| DIGITAL AND CONTROL INPUTS | | | | | |
| Input High Voltage, V_{IH} | 2 | | | V | $V_{IN} = 2.4\text{ V}$ |
| Input Low Voltage, V_{IL} | | | 0.8 | V | |
| Input Leakage Current | | 3 | | μA | |
| Input Capacitance, C_{IN} | | 2 | | pF | |
| ANALOG OUTPUTS | | | | | |
| Full-Scale Output Current | 4.1 | 4.33 | 4.6 | mA | |
| Output Current Range | 4.1 | 4.33 | 4.6 | mA | |
| DAC-to-DAC Matching | | 1.0 | | % | |
| Output Compliance Range, V_{OC} | 0 | 1.0 | 1.4 | V | |
| Output Capacitance, C_{OUT} | | 7 | | pF | |
| VOLTAGE REFERENCE | | | | | |
| Internal Reference Range, V_{REF} | 1.15 | 1.235 | 1.3 | V | |
| External Reference Range, V_{REF} | 1.15 | 1.235 | 1.3 | V | |
| V_{REF} Current ⁴ | | ± 10 | | μA | |
| POWER REQUIREMENTS | | | | | |
| Normal Power Mode | | | | | |
| I_{DD} ⁵ | | 170 | | mA | SD Only [16×] PS Only [8×] HDTV Only [2×] SD [16×, 10 Bit] + PS [8×, 20 Bit] |
| | | 110 | | mA | |
| | | 95 | | mA | |
| | | 172 | 190 ⁶ | mA | |
| I_{DD_IO} | | 1.0 | | mA | |
| I_{AA} ^{7,8} | | 39 | 45 | mA | |
| Sleep Mode | | | | | |
| I_{DD} | | 200 | | μA | |
| I_{AA} | | 10 | | μA | |
| I_{DD_IO} | | 250 | | μA | |
| Power Supply Rejection Ratio | | 0.01 | | %/% | |

NOTES

¹Oversampling disabled. Static DAC performance will be improved with increased oversampling ratios.

²DNL measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for -ve DNL, the actual step value lies below the ideal step value.

³Value in brackets for $V_{DD_IO} = 2.375\text{ V} - 2.75\text{ V}$.

⁴External current required to overdrive internal V_{REF} .

⁵ I_{DD} , the circuit current, is the continuous current required to drive the digital core.

⁶Guaranteed maximum by characterization.

⁷ I_{AA} is the total current required to supply all DACs including the V_{REF} circuitry and the PLL circuitry.

⁸All DACs on.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS ($V_{AA} = 2.375\text{ V} - 2.625\text{ V}$, $V_{DD} = 2.375\text{ V} - 2.625\text{ V}$; $V_{DD_IO} = 2.375\text{ V} - 3.6\text{ V}$, $V_{REF} = 1.235\text{ V}$, $R_{SET} = 3040\ \Omega$, $R_{LOAD} = 150\ \Omega$. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions | |
|------------------------------|-----|-------|-----|---------------|---|---------------------------|
| PROGRESSIVE SCAN MODE | | | | | | |
| Luma Bandwidth | | 12.5 | | MHz | Luma Ramp Unweighted Flat Field Full Bandwidth | |
| Chroma Bandwidth | | 5.8 | | MHz | | |
| SNR | | 65.6 | | dB | | |
| SNR | | 72 | | dB | | |
| HDTV MODE | | | | | | |
| Luma Bandwidth | | 30 | | MHz | | |
| Chroma Bandwidth | | 13.75 | | MHz | | |
| STANDARD DEFINITION MODE | | | | | | |
| Hue Accuracy | | 0.44 | | $^{\circ}$ | Referenced to 40 IRE | |
| Color Saturation Accuracy | | 0.20 | | % | | |
| Chroma Nonlinear Gain | | 0.84 | | $\pm\%$ | | |
| Chroma Nonlinear Phase | | -0.2 | | \pm° | | |
| Chroma/Luma Intermodulation | | 0 | | $\pm\%$ | | |
| Chroma/Luma Gain Inequality | | 97.5 | | $\pm\%$ | | |
| Chroma/Luma Delay Inequality | | 0 | | ns | | |
| Luminance Nonlinearity | | 0.1 | | $\pm\%$ | | |
| Chroma AM Noise | | 84 | | dB | | |
| Chroma PM Noise | | 75.3 | | dB | | |
| Differential Gain | | 0.09 | | % | | NTSC |
| Differential Phase | | 0.12 | | $^{\circ}$ | | NTSC |
| SNR | | 63.5 | | dB | | Luma Ramp |
| SNR | | 77.7 | | dB | | Flat Field Full Bandwidth |

Specifications subject to change without notice.

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TIMING SPECIFICATIONS ($V_{AA} = 2.375\text{ V} - 2.625\text{ V}$, $V_{DD} = 2.375\text{ V} - 2.625\text{ V}$; $V_{DD,IO} = 2.375\text{ V} - 3.6\text{ V}$, $V_{REF} = 1.235\text{ V}$, $R_{SET} = 3040\ \Omega$, $R_{LOAD} = 150\ \Omega$. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|-----|-----|-----|--------------------|---|
| MPU PORT¹ | | | | | |
| SCLOCK Frequency | 0 | | 400 | kHz | The first clock is generated after this period Relevant for repeated start condition |
| SCLOCK High Pulsewidth, t_1 | 0.6 | | | μs | |
| SCLOCK Low Pulsewidth, t_2 | 1.3 | | | μs | |
| Hold Time (Start Condition), t_3 | 0.6 | | | μs | |
| Setup Time (Start Condition), t_4 | 0.6 | | | μs | |
| Data Setup Time, t_5 | 100 | | | ns | |
| SDATA, SCLOCK Rise Time, t_6 | | | 300 | ns | |
| SDATA, SCLOCK Fall Time, t_7 | | | 300 | ns | |
| Setup Time (Stop Condition), t_8 | 0.6 | | | μs | |
| RESET Low Time | 100 | | | ns | |
| ANALOG OUTPUTS | | | | | |
| Analog Output Delay ² | | 7 | | ns | |
| Output Skew | | 1 | | ns | |
| CLOCK CONTROL AND PIXEL PORT³ | | | | | |
| f_{CLK} | | | 27 | MHz | Progressive Scan Mode HDTV Mode/ASYNC Mode |
| f_{CLK} | | 81 | | MHz | |
| Clock High Time t_9 | 40 | | | % of one clk cycle | |
| Clock Low Time t_{10} | 40 | | | % of one clk cycle | |
| Data Setup Time t_{11}^1 | 2.0 | | | ns | |
| Data Hold Time t_{12}^1 | 2.0 | | | ns | |
| SD Output Access Time t_{13} | | | 15 | ns | |
| SD Output Hold Time t_{14} | 5.0 | | | ns | |
| HD Output Access Time t_{13} | | | 14 | ns | |
| HD Output Hold Time t_{14} | 5.0 | | | ns | |
| PIPELINE DELAY⁴ | | | | | |
| | | 63 | | clk cycles | SD [2×, 16×] |
| | | 76 | | clk cycles | SD Component Mode [16×] |
| | | 35 | | clk cycles | PS [1×] |
| | | 41 | | clk cycles | PS [8×] |
| | | 36 | | clk cycles | HD [2×, 1×] |

NOTES

¹Guaranteed by characterization.

²Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.

³Data: C [9:0]; Y [9:0], S[9:0]

Control: $\overline{P_HSYNC}$, $\overline{P_VSYNC}$, $\overline{P_BLANK}$, $\overline{S_HSYNC}$, $\overline{S_VSYNC}$, $\overline{S_BLANK}$.

⁴SD, PS = 27 MHz, HD = 74.25 MHz.

Specifications subject to change without notice.

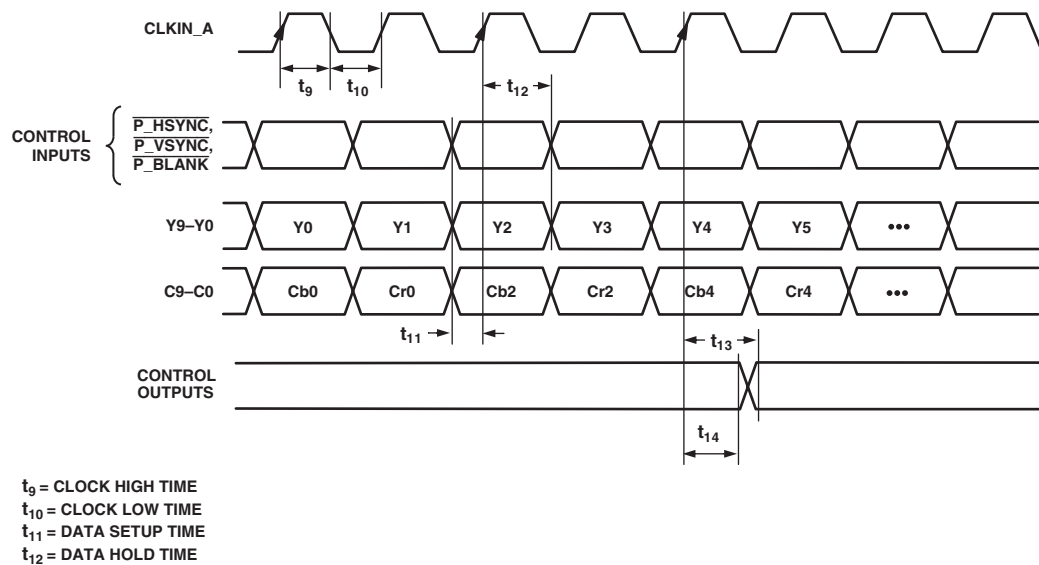


Figure 1. HD Only 4:2:2 Input Mode [Input Mode 010]; PS Only 4:2:2 Input Mode [Input Mode 001]

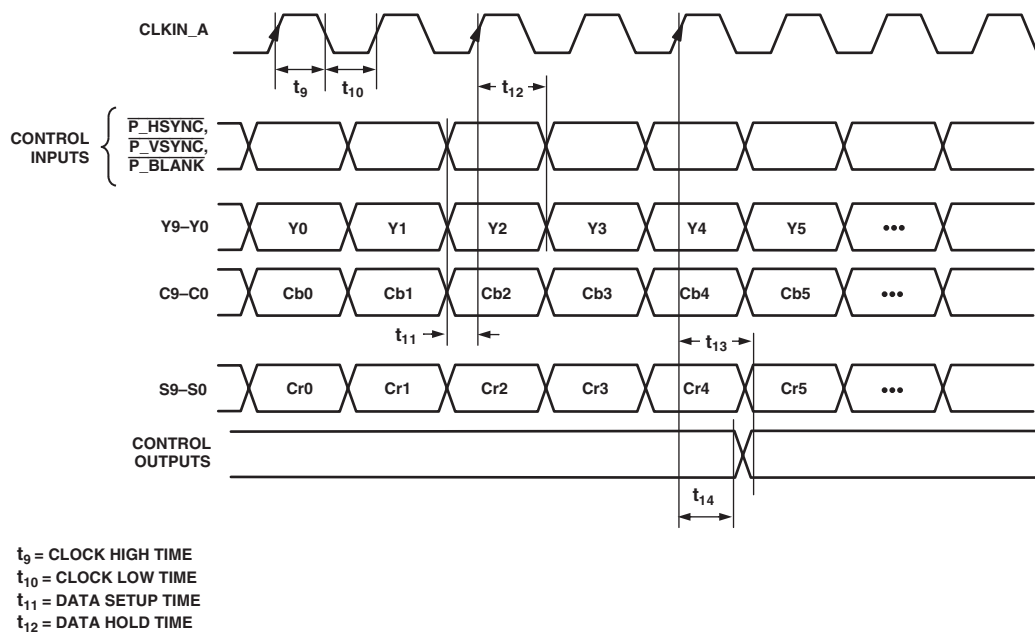


Figure 2. HD Only 4:4:4 Input Mode [Input Mode 010]; PS Only 4:4:4 Input Mode [Input Mode 001]

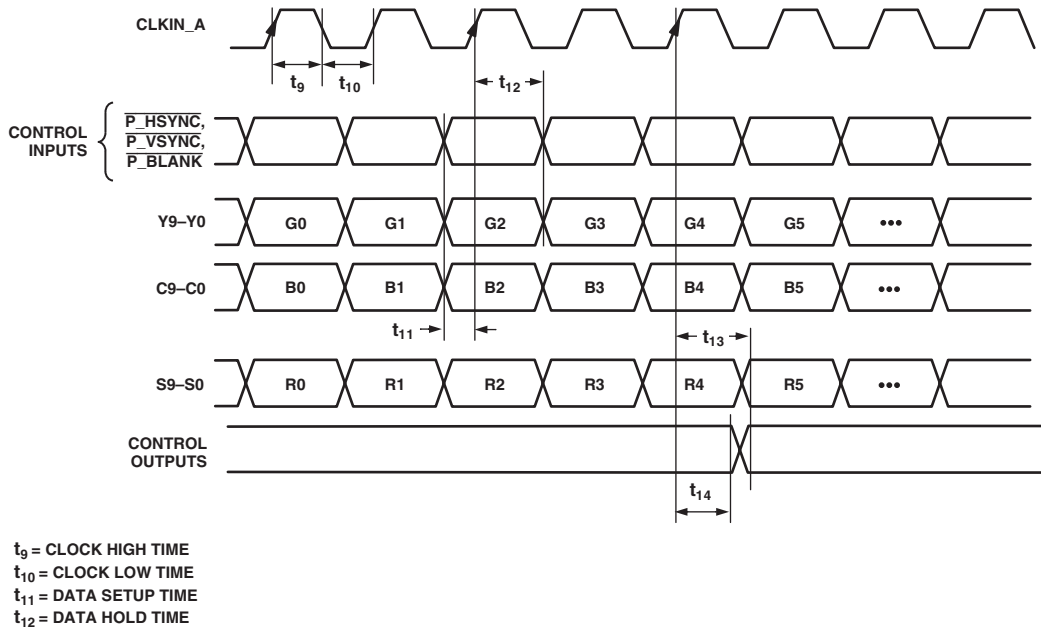


Figure 3. HD RGB 4:4:4 Input Mode [Input Mode 010]

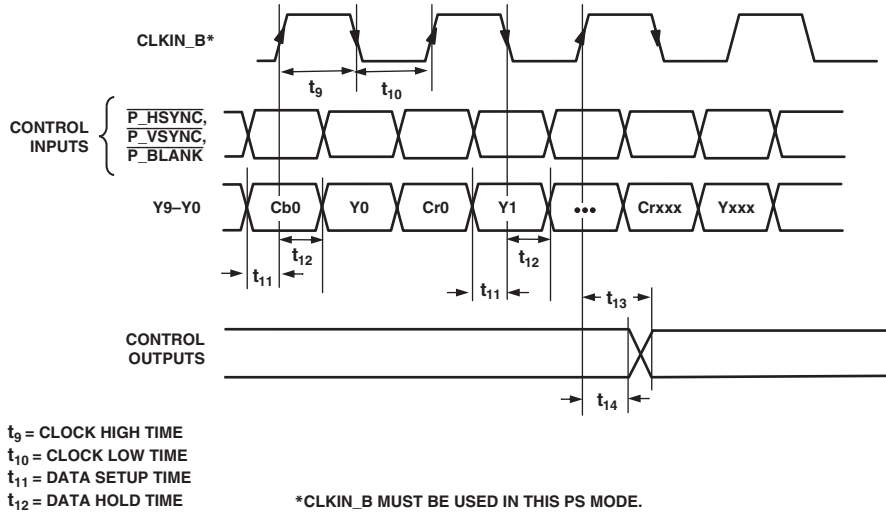
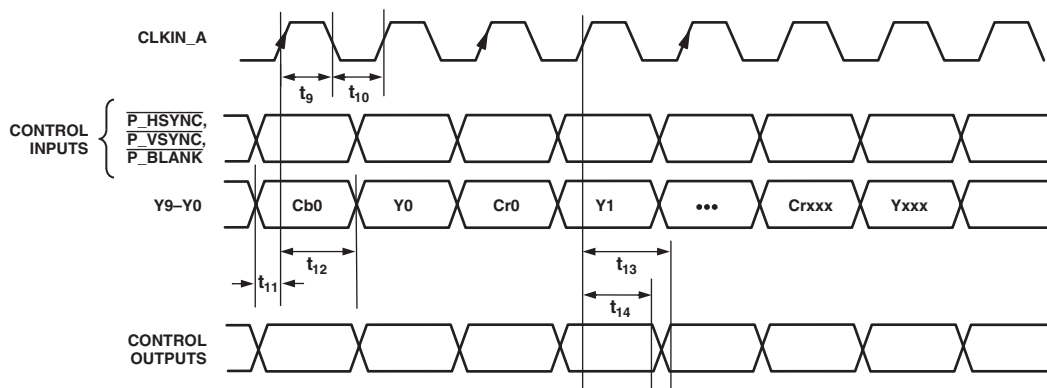
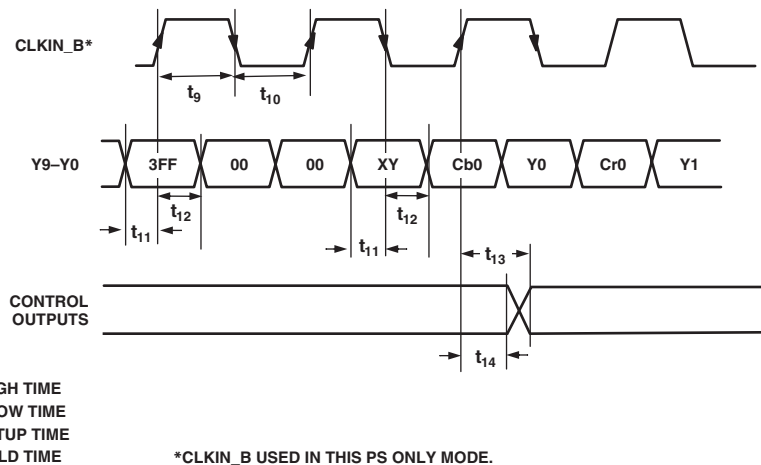


Figure 4. PS 4:2:2 1x10-Bit Interleaved at 27 MHz HSYNC/VSYNC Input Mode [Input Mode 100]



t_9 = CLOCK HIGH TIME
 t_{10} = CLOCK LOW TIME
 t_{11} = DATA SETUP TIME
 t_{12} = DATA HOLD TIME

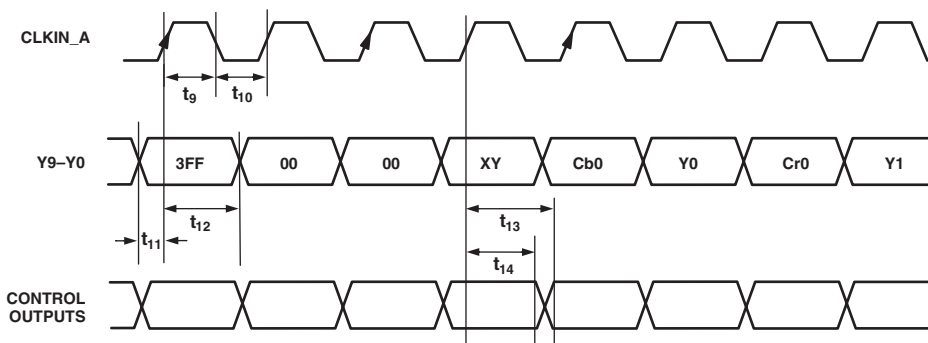
Figure 5. PS 4:2:2 1x10-Bit Interleaved at 54 MHz $\overline{\text{HSYNC}}/\overline{\text{VSYNC}}$ Input Mode [Input Mode 111]



t_9 = CLOCK HIGH TIME
 t_{10} = CLOCK LOW TIME
 t_{11} = DATA SETUP TIME
 t_{12} = DATA HOLD TIME

*CLKIN_B USED IN THIS PS ONLY MODE.

Figure 6. PS Only 4:2:2 1x10-Bit Interleaved at 27 MHz EAV/SAV Input Mode [Input Mode 100]



t_9 = CLOCK HIGH TIME
 t_{10} = CLOCK LOW TIME
 t_{11} = DATA SETUP TIME
 t_{12} = DATA HOLD TIME

NOTE: Y0, Cb0 SEQUENCE AS PER SUBADDRESS 0x01 BIT 1

Figure 7. PS Only 4:2:2 1x10-Bit Interleaved at 54 MHz EAV/SAV Input Mode [Input Mode 111]

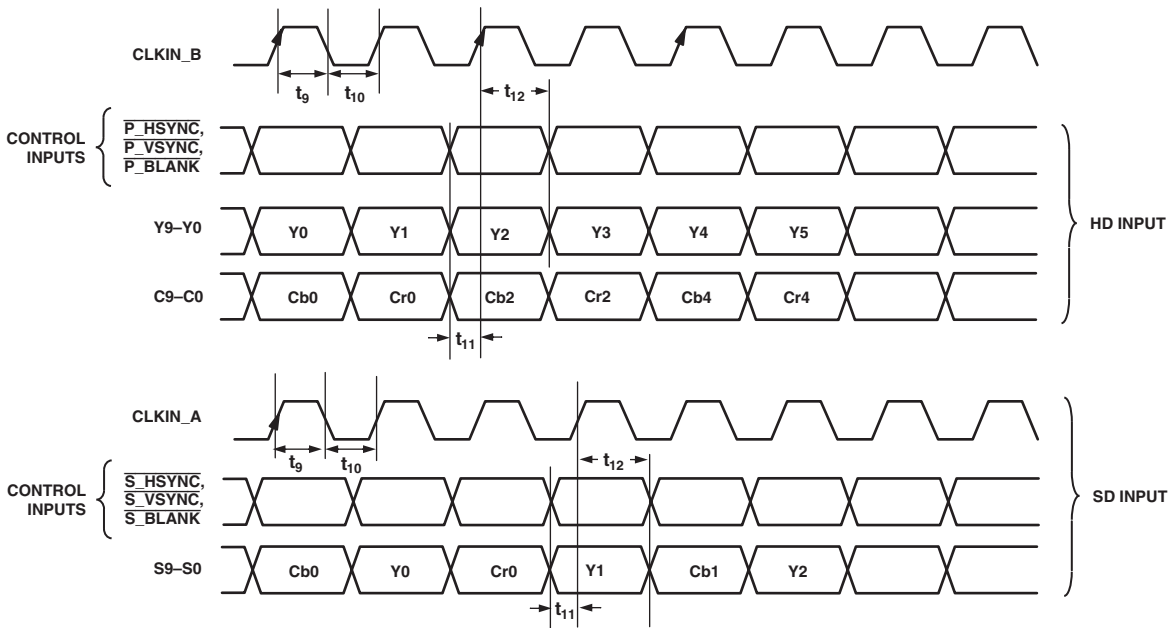


Figure 8. HD 4:2:2 and SD (10-Bit) Simultaneous Input Mode [Input Mode 101]; SD Oversampled [Input Mode 110] HD Oversampled

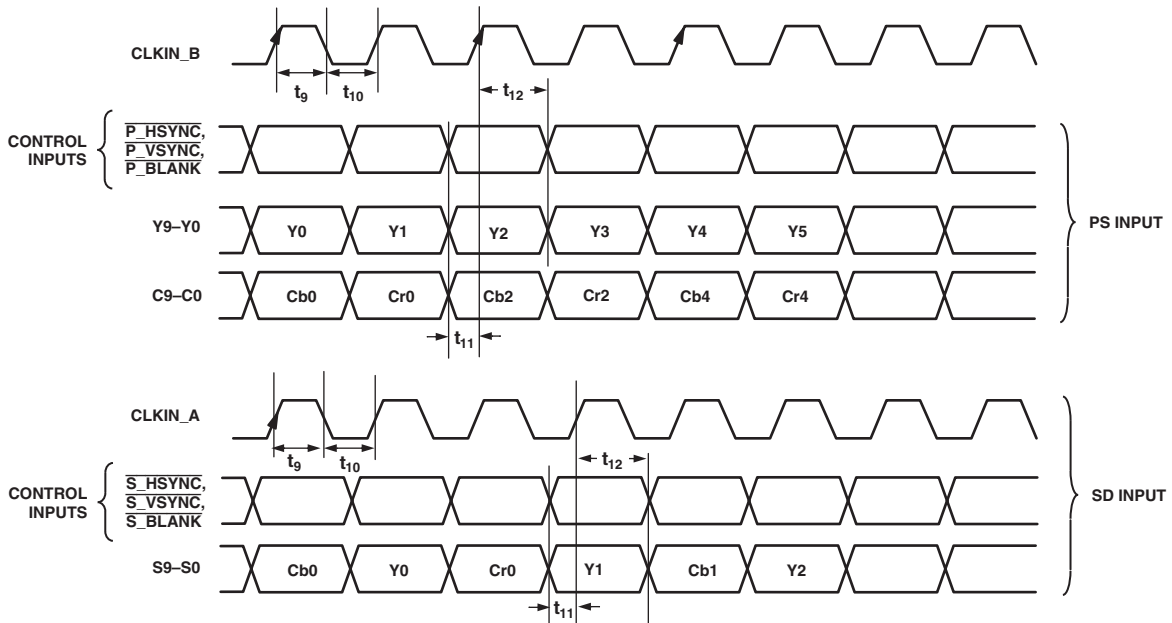


Figure 9. PS (4:2:2) and SD (10-Bit) Simultaneous Input Mode [Input Mode 011]

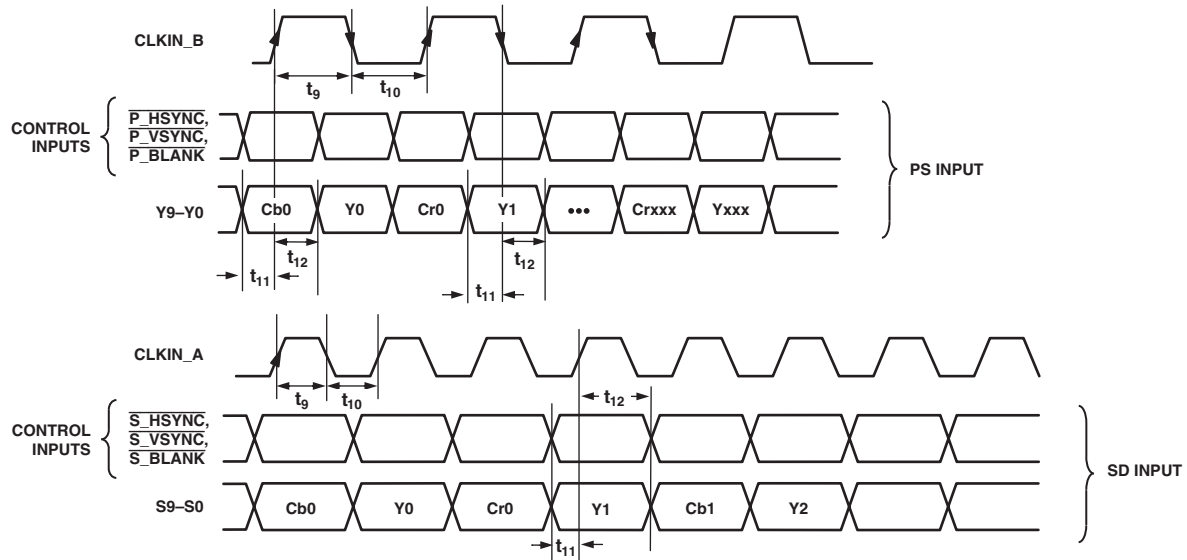
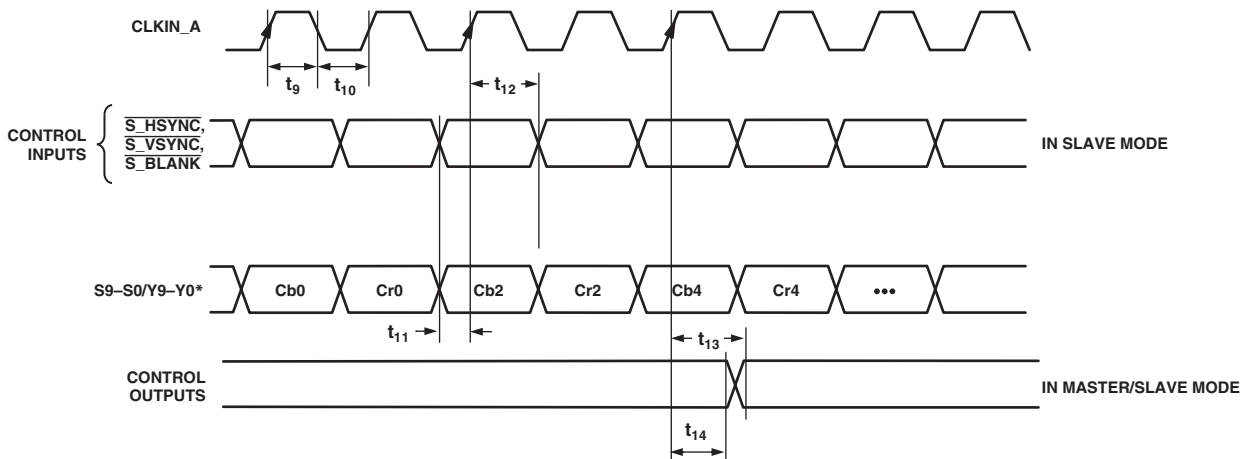


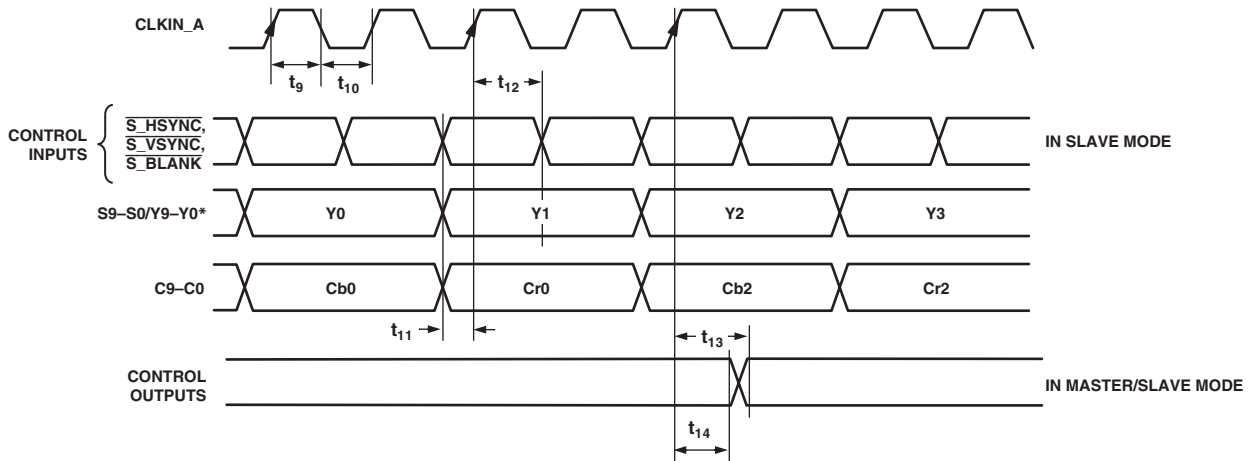
Figure 10. PS (10-Bit) and SD (10-Bit) Simultaneous Input Mode [Input Mode 100]



*SELECTED BY ADDRESS 0x01 BIT 7

Figure 11. 10-/8-Bit SD Only Pixel Input Mode [Input Mode 000]

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*SELECTED BY ADDRESS 0x01 BIT 7

Figure 12. 20-/16-Bit SD Only Pixel Input Mode [Input Mode 000]

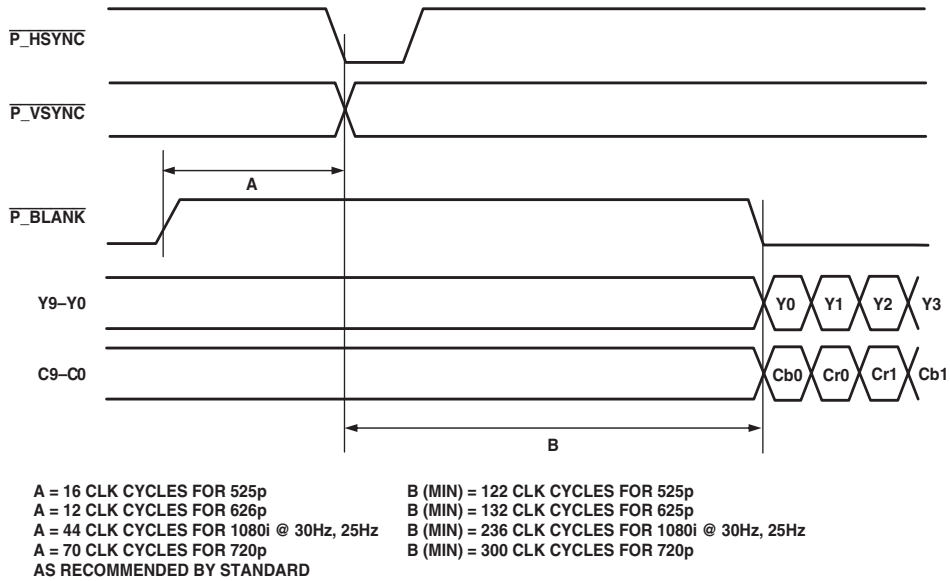
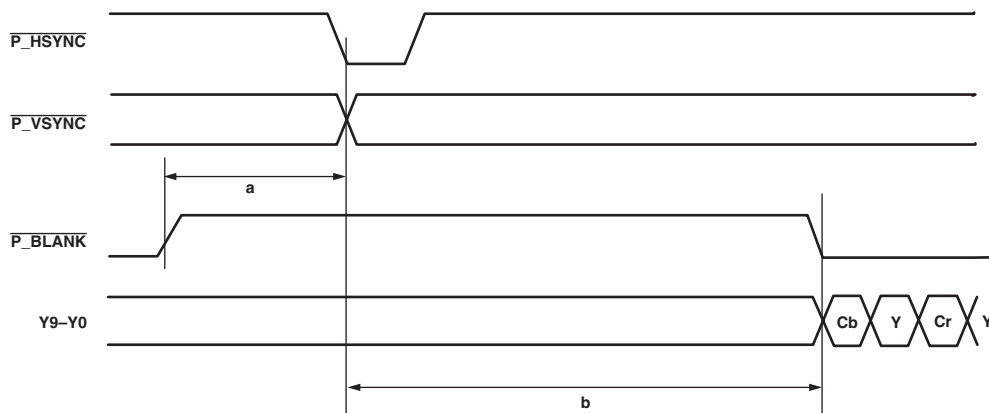
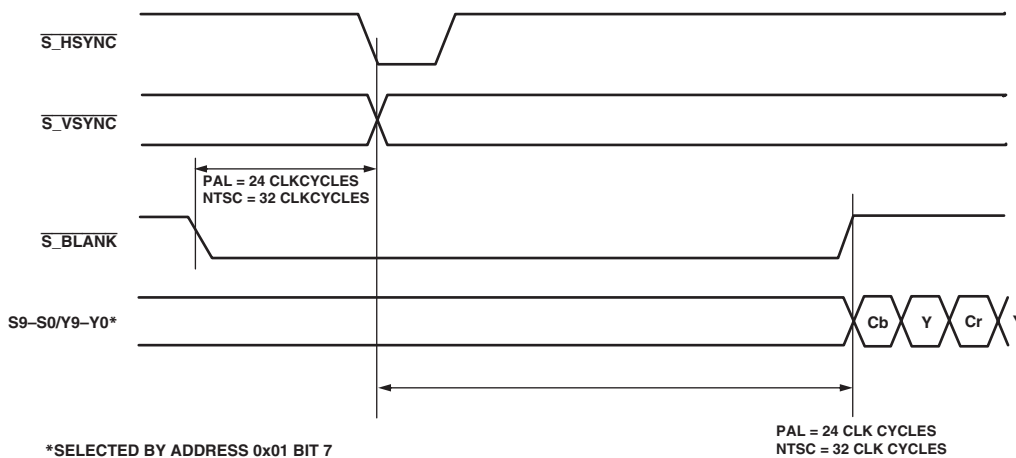


Figure 13. HD 4:2:2 Input Timing Diagram



a = 32 CLK CYCLES FOR 525p
 a = 24 CLK CYCLES FOR 625p
 AS RECOMMENDED BY STANDARD
 b(MIN) = 244 CLK CYCLES FOR 525p
 b(MIN) = 264 CLK CYCLES FOR 625p

Figure 14. PS 4:2:2 1x10-Bit Interleaved Input Timing Diagram



*SELECTED BY ADDRESS 0x01 BIT 7

PAL = 24 CLK CYCLES
 NTSC = 32 CLK CYCLES

Figure 15. SD Timing Input for Timing Mode 1

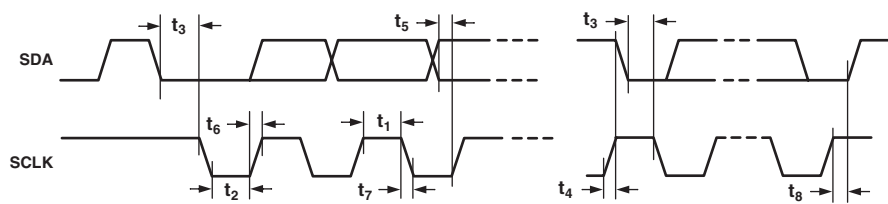


Figure 16. MPU Port Timing Diagram

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ABSOLUTE MAXIMUM RATINGS*

| | |
|---|--|
| V _{AA} to AGND | +3.0 V to -0.3 V |
| V _{DD} to GND | +3.0 V to -0.3 V |
| V _{DD_IO} to IO_GND | -0.3 V to V _{DD_IO} to +0.3 V |
| Ambient Operating Temperature (T _A) | 0°C to 70°C |
| Storage Temperature (T _S) | -65°C to +150°C |
| Infrared Reflow Soldering (20 secs) | 260°C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

$$\theta_{JC} = 11^{\circ}\text{C/W}$$

$$\theta_{JA} = 47^{\circ}\text{C/W}$$

The ADV7314 is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and is able to withstand surface-mount soldering at up to 255°C [$\pm 5^{\circ}\text{C}$]. In addition, it is backward compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ORDERING GUIDE*

| Model | Package Description | Package Option |
|------------|------------------------------|----------------|
| ADV7314KST | Plastic Quad Flatpack (LQFP) | ST-64 |

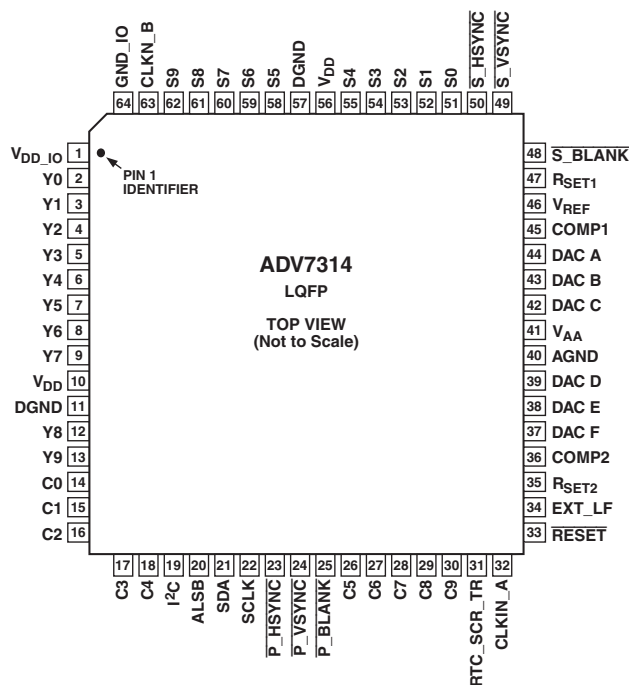
*Analog output short circuit to any power supply or common can be of an indefinite duration.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7314 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

| Pin No. | Mnemonic | Input/Output | Function |
|---------|--------------|--------------|--|
| 11, 57 | DGND | G | Digital Ground. |
| 40 | AGND | G | Analog Ground. |
| 32 | CLKIN_A | I | Pixel Clock Input for HD (74.25 MHz Only, PS Only (27 MHz), SD Only (27 MHz). |
| 63 | CLKIN_B | I | Pixel Clock Input. Requires a 27 MHz reference clock for Progressive Scan mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes. |
| 36, 45 | COMP2, COMP1 | O | Compensation Pin for DACs. Connect 0.1 μ F capacitor from COMP pin to V _{AA} . |
| 44 | DAC A | O | CVBS/Green/Y/Y Analog Output. |
| 43 | DAC B | O | Chroma/Blue/U/Pb Analog Output. |
| 42 | DAC C | O | Luma/Red/V/Pr Analog Output. |
| 39 | DAC D | O | In SD Only Mode: CVBS/Green/Y Analog Output. In HD Only mode and simultaneous HD/SD mode: Y/Green [HD] Analog Output. |
| 38 | DAC E | O | In SD Only Mode: Luma/Blue/U Analog Output. In HD Only mode and simultaneous HD/SD mode: Pr/Red Analog Output. |
| 37 | DAC F | O | In SD Only Mode: Chroma/Red/V Analog Output. In HD Only mode and simultaneous HD/SD mode: Pb/Blue [HD] Analog Output. |
| 23 | P_HSYNC | I | Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD. |
| 24 | P_VSYNC | I | Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD. |
| 25 | P_BLANK | I | Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD. |
| 48 | S_BLANK | I/O | Video Blanking Control Signal for SD only. |

ADV7314

| Pin No. | Mnemonic | Input/Output | Function |
|--------------|---------------------------------------|--------------|--|
| 50 | $\overline{S_HSYNC}$ | I/O | Video Horizontal Sync Control Signal for SD Only. |
| 49 | $\overline{S_VSYNC}$ | I/O | Video Vertical Sync Control Signal for SD Only. |
| 2–9, 12–13 | Y9–Y0 | I | SD or Progressive Scan/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0. For 8-bit data input, LSB is set up on Y2. |
| 14–18, 26–30 | C9–C0 | I | Progressive Scan/HDTV Input Port. In 4:4:4 Input mode, this port is used for the Cb[Blue/U] data. The LSB is set up on Pin C0. For 8-bit data input, LSB is set up on C2. |
| 51–55, 58–62 | S9–S0 | I | SD or Progressive Scan/HDTV Input Port for Cr [Red/V] Data in 4:4:4 Input Mode. LSB is set up on Pin S0. For 8-bit data input, LSB is set up on S2. |
| 33 | \overline{RESET} | I | This input resets the on-chip timing generator and sets the ADV7314 into default register setting. \overline{RESET} is an active low signal. |
| 35, 47 | R _{SET2} , R _{SET1} | I | A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs. |
| 22 | SCLK | I | I ² C Port Serial Interface Clock Input. |
| 21 | SDA | I/O | I ² C Port Serial Data Input/Output. |
| 20 | ALSB | I | TTL Address Input. This signal sets up the LSB of the I ² C address. When this pin is tied low, the I ² C filter is activated, reducing noise on the I ² C interface. |
| 1 | V _{DD_IO} | P | Power Supply for Digital Inputs and Outputs. |
| 10, 56 | V _{DD} | P | Digital Power Supply. |
| 41 | V _{AA} | P | Analog Power Supply. |
| 46 | V _{REF} | I/O | Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V). |
| 34 | EXT_LF | I | External Loop Filter for the Internal PLL. |
| 31 | RTC_SCR_TR | I | Multifunctional Input. Real-time control (RTC) input, timing reset input, subcarrier reset input. |
| 19 | I ² C | I | This input pin must be tied high (V _{DD_IO}) for the ADV7314 to interface over the I ² C port. |
| 64 | GND_IO | | Digital Input/Output Ground. |

TERMINOLOGY

| | |
|-------|---|
| SD | Standard definition video, conforming to ITU-R BT.601/656. |
| HD | High definition video, such as progressive scan or HDTV. |
| PS | Progressive scan video, conforming to SMPTE 293M, ITU-R BT.1358, BTA T-1004 EDTV2, BTA 1362 |
| HDTV | High definition television video, conforming to SMPTE 274M or SMPTE 296M. |
| YCrCb | SD, HD, or PS component digital video. |
| YPrPb | HD, SD, or PS component analog video. |

MPU PORT DESCRIPTION

The ADV7314 supports a 2-wire serial (I²C compatible) micro-processor bus driving multiple peripherals. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7314 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 17. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7314 to Logic 0 or Logic 1. When ALSB is set to 1, there is greater input bandwidth on the I²C lines, which allows high speed data transfers on this bus. When ALSB is set to 0, there is reduced input bandwidth on the I²C lines, which means that pulses of less than 50 ns will not pass into the I²C internal controller. This mode is recommended for noisy systems.

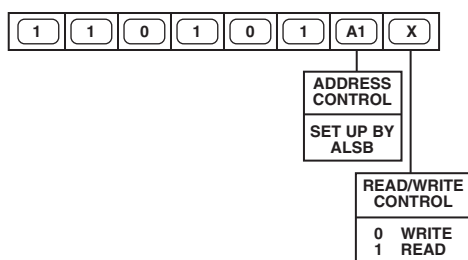


Figure 17. ADV7314 Slave Address = D4h

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at

this point and maintain an idle condition. The idle condition is when the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/W bit determines the direction of the data.

A Logic 0 on the LSB of the first byte means that the master will write information to the peripheral. A Logic 1 on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7314 acts as a standard slave device on the bus. The data on the SDA pin is eight bits wide, supporting the 7-bit addresses plus the R/W bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility, which allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without having to update all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCL high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7314 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode the user exceeds the highest subaddress, the following action will be taken:

1. In read mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is when the SDA line is not pulled low on the ninth pulse.
2. In write mode, the data for the invalid byte will not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7314, and the part will return to the idle condition.

ADV7314

Before writing to the subcarrier frequency registers, the ADV7314 must have been reset at least once since power-up.

The four subcarrier frequency registers must be updated starting with subcarrier frequency register 0 through subcarrier frequency register 3. The subcarrier frequency will not update until the last subcarrier frequency register byte has been received by the ADV7314.

Figure 18 illustrates an example of the data transfer for a write sequence and the start and stop conditions.

Figure 19 shows bus write and read sequences.

REGISTER ACCESS

The MPU can write to or read from all of the registers of the ADV7314 except the subaddress registers, which are write-only registers. The subaddress register determines which register the

next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is then performed from/to the target address, which increments to the next address until a stop command on the bus is performed.

Register Programming

The following section describes the functionality of each register. All registers can be read from as well as written to unless otherwise stated.

Subaddress Register (SR7-SR0)

The communications register is an 8-bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place.

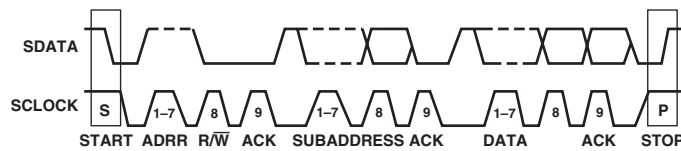


Figure 18. Bus Data Transfer

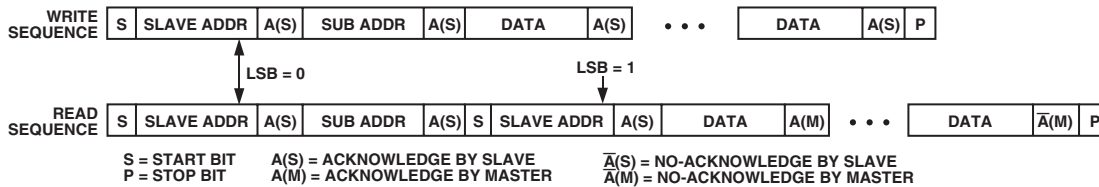


Figure 19. Write and Read Sequence

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Register Reset Value (Shaded) | | |
|----------------------|----------------------|---|-------|-------|-------|-------|-------|-------|-------|---------------------|----------------------|---|---|--|
| 00h | Power Mode Register | Sleep Mode. With this control enabled, the current consumption is reduced to μ A level. All DACs and the internal PLL ckt are disabled. I ² C registers can be read from and written to in sleep mode. | | | | | | | | 0 | Sleep Mode off | FCh | | |
| | | | | | | | | | | 1 | Sleep Mode on | | | |
| | | PLL and Oversampling Control. This control allows the internal PLL ckt to be powered down and the oversampling to be switched off. | | | | | | | | 0 | | PLL on | | |
| | | | | | | | | | | 1 | | PLL off | | |
| | | DAC F. Power on/off. | | | | | | | | 0 | | DAC F off | | |
| | | | | | | | | | | 1 | | DAC F on | | |
| | | DAC E. Power on/off. | | | | | | | | 0 | | DAC E off | | |
| | | | | | | | | | | 1 | | DAC E on | | |
| | | DAC D. Power on/off. | | | | | | | | 0 | | DAC D off | | |
| | | | | | | | | | | 1 | | DAC D on | | |
| | | DAC C. Power on/off. | | | | 0 | | | | | | DAC C off | | |
| | | | | | | 1 | | | | | | DAC C on | | |
| | | DAC B. Power on/off. | | | 0 | | | | | | | DAC B off | | |
| | | | | | 1 | | | | | | | DAC B on | | |
| DAC A. Power on/off. | | 0 | | | | | | | | DAC A off | | | | |
| | | 1 | | | | | | | | DAC A on | | | | |
| 01h | Mode Select Register | BTA T-1004 or 1362 Compatibility | | | | | | | | 0 | Disabled | Only for PS dual edge clk mode | | |
| | | | | | | | | | | 1 | Enabled | | | |
| | | Clock Edge | | | | | | | | 0 | | Cb clocked on rising edge | Only for PS interleaved input at 27 MHz | |
| | | | | | | | | | | 1 | | Y clocked on rising edge | | |
| | | Reserved | | | | | | | 0 | | | 38h | | |
| | | Clock Align | | | | | | | | 0 | | | | |
| | | | | | | | | | | 1 | | Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns. | Only if two input clocks are used | |
| | | Input Mode | | 0 | 0 | 0 | | | | | | | SD input only | |
| | | | | 0 | 0 | 1 | | | | | | | PS input only | |
| | | | | 0 | 1 | 0 | | | | | | | HDTV input only | |
| | | | | 0 | 1 | 1 | | | | | | | SD and PS [20-bit] | |
| | | | | 1 | 0 | 0 | | | | | | | SD and PS [10-bit] | |
| | | | | 1 | 0 | 1 | | | | | | | SD and HDTV [SD oversampled] | |
| | | | | 1 | 1 | 0 | | | | | | | SD and HDTV [HDTV oversampled] | |
| | 1 | 1 | 1 | | | | | | | PS only [at 54 MHz] | | | | |
| Y/S Bus Swap | 0 | | | | | | | | | | 10-bit data on S Bus | SD Only. 10-Bit/20-Bit Input mode | | |
| | 1 | | | | | | | | | | 10-bit data on Y Bus | | | |

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| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | | |
|---------|-------------------------------------|-------------------------------------|-------------------------------------|-------|-------|-------|-------|-------|-------|---------------|---|-------------|---------------------------------|-------|
| 02h | Mode Register 0 | Reserved | | | | | | | 0 | 0 | Zero must be written to these bits | 20h | | |
| | | Test Pattern Black Bar | | | | | | 0 | | | | Disabled | 11h, Bit 2 must be enabled also | |
| | | | | | | | | 1 | | | | Enabled | | |
| | | RGB Matrix | | | | | 0 | | | | | | Disable Programmable RGB Matrix | |
| | | | | | | | 1 | | | | | | Enable Programmable RGB Matrix | |
| | | Sync on RGB ¹ | | | | | 0 | | | | | | No Sync | |
| | | | | | | | 1 | | | | | | Sync on all RGB outputs | |
| | | RGB/YUV Output | | | | 0 | | | | | | | RGB component outputs | |
| | | | | 1 | | | | | | | YUV component outputs | | | |
| SD Sync | | | 0 | | | | | | | | No Sync output | | | |
| | | | 1 | | | | | | | | Output SD syncs on S_HSYNC output, S_VSYNC output, S_BLANK output | | | |
| HD Sync | | 0 | | | | | | | | | No Sync output | | | |
| | | 1 | | | | | | | | | Output HD syncs on P_HSYNC output, P_VSYNC output, P_BLANK output | | | |
| 03h | RGB Matrix 0 | | | | | | | | x | x | LSB for GY | 03h | | |
| 04h | RGB Matrix 1 | | | | | | x | x | | | LSB for RV | F0h | | |
| | | | | | | | | | | | LSB for BU | | | |
| | | | | x | x | | | | | | | | LSB for GV | |
| | | x | x | | | | | | | | | | LSB for GU | |
| 05h | RGB Matrix 2 | x | x | x | x | x | x | x | x | x | Bit 9–2 for GY | 4Eh | | |
| 06h | RGB Matrix 3 | x | x | x | x | x | x | x | x | x | Bit 9–2 for GU | 0Eh | | |
| 07h | RGB Matrix 4 | x | x | x | x | x | x | x | x | x | Bit 9–2 for GV | 24h | | |
| 08h | RGB Matrix 5 | x | x | x | x | x | x | x | x | x | Bit 9–2 for BU | 92h | | |
| 09h | RGB Matrix 6 | x | x | x | x | x | x | x | x | x | Bit 9–2 for RV | 7Ch | | |
| 0Ah | DAC A,B,C Output Level ² | Positive Gain to DAC Output Voltage | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0% | 00h | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +0.018% | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.036% | | |
| | | | | | | | | | | | | ... | | |
| | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +7.382% | | |
| | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +7.5% | | |
| | | | Negative Gain to DAC Output Voltage | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | -7.5% |
| | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | -7.382% | | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -7.364% | | |
| | | | | | | | | | | | | ... | | |
| 0Bh | DAC D,E,F Output Level | Positive Gain to DAC Output Voltage | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0% | 00h | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | +0.018% | | |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.036% | | |
| | | | | | | | | | | | | ... | | |
| | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | +7.382% | | |
| | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +7.5% | | |
| | | | Negative Gain to DAC Output Voltage | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | -7.5% |
| | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | -7.382% | | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -7.364% | | |
| | | | | | | | | | | | | ... | | |
| 0Ch | | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Note 3 | 00h | | | |
| 0Dh | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Note 3 | 00h | | | |
| 0Eh | Reserved | | | | | | | | | | 00h | | | |
| 0Fh | Reserved | | | | | | | | | | 00h | | | |

¹For more detail, refer to Appendix 7.

²For more detail on the programmable output levels, refer to the Programmable DAC Gain Control section.

³Must be written to after power-up/reset.

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Values | | |
|------------------------------|--------------------|-----------------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------------------|--------------|------------------------------------|-------------------|
| 10h | HD Mode Register 1 | HD Output Standard | | | | | | | 0 | 0 | EIA770.2 output | 00h | | |
| | | | | | | | | | | 0 | 1 | | EIA770.1 output | |
| | | | | | | | | | | 1 | 0 | | Output levels for full input range | |
| | | | | | | | | | | 1 | 1 | | Reserved | |
| | | HD Input Control Signals | | | | | | 0 | 0 | | | | HSYNC, VSYNC, BLANK | |
| | | | | | | | | 0 | 1 | | | | EAV/SAV codes | |
| | | | | | | | | 1 | 0 | | | | Async timing mode | |
| | | | | | | | | 1 | 1 | | | | Reserved | |
| | | HD 625p | | | | 0 | | | | | | | 525p | |
| | | | | | | | 1 | | | | | | 625p | |
| | | HD 720p | | | 0 | | | | | | | | 1080i | |
| | | | | | | 1 | | | | | | | 720p | |
| | | HD BLANK Polarity | | 0 | | | | | | | | | | BLANK active high |
| | | | | 1 | | | | | | | | | | BLANK active low |
| HD Macrovision for 525p/625p | 0 | | | | | | | | | | Macrovision off | | | |
| | 1 | | | | | | | | | | Macrovision on | | | |
| 11h | HD Mode Register 2 | HD Pixel Data Valid | | | | | | | 0 | | Pixel data valid off | 00h | | |
| | | | | | | | | | | 1 | | | Pixel data valid on | |
| | | | | | | | | | | 0 | | | Reserved | |
| | | HD Test Pattern Enable | | | | | | 0 | | | | | HD test pattern off | |
| | | | | | | | | | 1 | | | | HD test pattern on | |
| | | HD Test Pattern Hatch/Field | | | | | 0 | | | | | | Hatch | |
| | | | | | | | 1 | | | | | | Field/Frame | |
| | | HD VBI Open | | | | 0 | | | | | | | Disabled | |
| | | | | | | 1 | | | | | | | Enabled | |
| | | HD Undershoot Limiter | | 0 | 0 | | | | | | | | | Disabled |
| | | | | 0 | 1 | | | | | | | | | -11 IRE |
| | | | | 1 | 0 | | | | | | | | | -6 IRE |
| | | | | 1 | 1 | | | | | | | | | -1.5 IRE |
| | | HD Sharpness Filter | 0 | | | | | | | | | | | Disabled |
| 1 | | | | | | | | | | | Enabled | | | |

ADV7314

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | | |
|--|--------------------|--|-------|-------|-------|-------|-------|-------|-------|-------|--|-------------------------------|-----------------------------------|-------------|
| 12h | HD Mode Register 3 | HD Y Delay with Respect to Falling Edge of HSYNC | | | | | | 0 | 0 | 0 | 0 clk cycle | 00h | | |
| | | | | | | | | 0 | 0 | 1 | 1 clk cycle | | | |
| | | | | | | | | | 0 | 1 | 0 | | 2 clk cycle | |
| | | | | | | | | | 0 | 1 | 1 | | 3 clk cycle | |
| | | | | | | | | | 1 | 0 | 0 | | 4 clk cycle | |
| | | HD with Respect to Falling Edge of HSYNC | | | | 0 | 0 | 0 | | | | | 0 clk cycle | |
| | | | | | | 0 | 0 | 1 | | | | | 1 clk cycle | |
| | | | | | | 0 | 1 | 0 | | | | | 2 clk cycle | |
| | | | | | | 0 | 1 | 1 | | | | | 3 clk cycle | |
| | | | | | | 1 | 0 | 0 | | | | | 4 clk cycle | |
| | | HD CGMS | | | 0 | | | | | | | | Disabled | |
| | | | | | 1 | | | | | | | | Enabled | |
| HD CGMS CRC | | | 0 | | | | | | | | Disabled | | | |
| | | | 1 | | | | | | | | Enabled | | | |
| 13h | HD Mode Register 4 | HD Cr/Cb Sequence | | | | | | | | 0 | Cb after falling edge of HSYNC | 4Ch | | |
| | | | | | | | | | | 1 | Cr after falling edge of HSYNC | | | |
| | | Reserved | | | | | | | | 0 | | 0 must be written to this bit | | |
| | | HD Input Format | | | | | | | 0 | | | 8-bit input | | |
| | | | | | | | | | 1 | | | 10-bit input | | |
| | | Sinc Filter on DAC D, E, F | | | | | | 0 | | | | | Disabled | |
| | | | | | | | | 1 | | | | | Enabled | |
| | | Reserved | | | | | 0 | | | | | | 0 must be written to this bit | |
| | | | | | | | 1 | | | | | | Enabled | |
| | | HD Chroma SSAF | | | | 0 | | | | | | | Disabled | |
| | | | | | | 1 | | | | | | | Enabled | |
| | | HD Chroma Input | | | 0 | | | | | | | | 4:4:4 | |
| | | | 1 | | | | | | | | 4:2:2 | | | |
| HD Double Buffering | | | 0 | | | | | | | | Disabled | | | |
| | | | 1 | | | | | | | | Enabled | | | |
| 14h | HD Mode Register 5 | HD Timing Reset | | | | | | | | x | A low-high-low transition resets the internal HD timing counters | 00h | | |
| | | | | | | | | 0 | 0 | | | | 30 Hz/2200 total samples/line | |
| | | 1080i Frame Rate | | | | | | 0 | 1 | | | | 25 Hz/2640 total samples/line | |
| | | Reserved | | | 0 | 0 | 0 | | | | | | 0 should be written to these bits | |
| | | HD VSYNC/Field Input | | | 0 | | | | | | | | | Field Input |
| | | | | | 1 | | | | | | | | | VSYNC Input |
| Lines/Frame ¹ | | | 0 | | | | | | | | Update Field/line counter | | | |
| | | | 1 | | | | | | | | Field/line counter free running | | | |
| 15h | HD Mode Register 6 | Reserved | | | | | | | | 0 | 0 must be written to this bit | 00h | | |
| | | HD RGB Input | | | | | | | | 0 | | | Disabled | |
| | | | | | | | | | | | 1 | | Enabled | |
| | | HD Sync on PrPb | | | | | | | 0 | | | | Disabled | |
| | | | | | | | | | 1 | | | | Enabled | |
| | | HD Color DAC Swap | | | | | | 0 | | | | | DAC E = Pb; DAC F = Pr | |
| | | | | | | | | 1 | | | | | DAC E = Pr; DAC F = Pb | |
| | | HD Gamma Curve A/B | | | | | 0 | | | | | | Gamma Curve A | |
| | | | | | | | 1 | | | | | | Gamma Curve B | |
| | | HD Gamma Curve Enable | | | | 0 | | | | | | | Disabled | |
| | | | | | | 1 | | | | | | | Enabled | |
| | | HD Adaptive Filter Mode ² | | | 0 | | | | | | | | Mode A | |
| | | | 1 | | | | | | | | Mode B | | | |
| HD Adaptive Filter Enable ² | | | 0 | | | | | | | | Disabled | | | |
| | | | 1 | | | | | | | | Enabled | | | |

NOTES

¹When set to 0, the line and field counters automatically wrap around at the end of the field/frame of the standard selected. When set to 1, the field/line counters are free running and wrap around when external sync signals indicate so.

²Adaptive Filter mode is not available in PS only @ 54 MHz input mode.

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | |
|------------------|--------------------------|----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------------|------------------|-------------|-------------|
| 16h | HD Y Level ¹ | | x | x | x | x | x | x | x | x | Y color value | A0h | |
| 17h | HD Cr Level ¹ | | x | x | x | x | x | x | x | x | Cr color value | 80h | |
| 18h | HD Cb Level ¹ | | x | x | x | x | x | x | x | x | Cb color value | 80h | |
| 19h | | Reserved | | | | | | | | | | 00h | |
| 1Ah | | Reserved | | | | | | | | | | 00h | |
| 1Bh | | Reserved | | | | | | | | | | 00h | |
| 1Ch | | Reserved | | | | | | | | | | 00h | |
| 1Dh | | Reserved | | | | | | | | | | 00h | |
| 1Eh | | Reserved | | | | | | | | | | 00h | |
| 1Fh | | Reserved | | | | | | | | | | 00h | |
| 15h | HD Mode Register 6 | HD Gamma Curve Enable | | | 0 | | | | | | | Disabled | |
| | | | | 1 | | | | | | | | Enabled | |
| | | HD Adaptive Filter Mode | | 0 | | | | | | | | | Mode A |
| | | | | 1 | | | | | | | | | Mode B |
| | | HD Adaptive Filter Enable | 0 | | | | | | | | | Disabled | |
| | | | 1 | | | | | | | | | | Enabled |
| 20h | HD Sharpness Filter Gain | HD Sharpness Filter Gain Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 00h | |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | | |
| | | | | | | | .. | .. | .. | .. | | | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = -8 | | |
| | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | 1 | 1 | 1 | 1 | Gain A = -1 | | | |
| | | HD Sharpness Filter Gain Value B | 0 | 0 | 0 | 0 | | | | | | | Gain B = 0 |
| | | | 0 | 0 | 0 | 1 | | | | | | | Gain B = +1 |
| | | | .. | .. | .. | .. | | | | | | | |
| 0 | 1 | | 1 | 1 | | | | | | Gain B = +7 | | | |
| 1 | 0 | | 0 | 0 | | | | | | Gain B = -8 | | | |
| | .. | .. | .. | .. | | | | | | | | | |
| | 1 | 1 | 1 | 1 | | | | | | Gain B = -1 | | | |
| 21h ² | HD CGMS | HD CGMS Data Bits | 0 | 0 | 0 | 0 | C19 | C18 | C17 | C16 | CGMS 19-16 | 00h | |
| 22h | HD CGMS | HD CGMS Data Bits | C15 | C14 | C13 | C12 | C11 | C10 | C9 | C8 | CGMS 15-8 | 00h | |
| 23h | HD CGMS | HD CGMS Data Bits | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | CGMS 7-0 | 00h | |
| 24h | HD Gamma A ¹ | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A0 | 00h | |
| 25h | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A1 | 00h | |
| 26h | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A2 | 00h | |
| 27h | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A3 | 00h | |
| 28h | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A4 | 00h | |
| 29h | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A5 | 00h | |
| 2Ah | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A6 | 00h | |
| 2Bh | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A7 | 00h | |
| 2Ch | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A8 | 00h | |
| 2Dh | HD Gamma A | HD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A9 | 00h | |
| 2Eh | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B0 | 00h | |
| 2Fh | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B1 | 00h | |
| 30h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B2 | 00h | |
| 31h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B3 | 00h | |
| 32h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B4 | 00h | |
| 33h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B5 | 00h | |
| 34h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B6 | 00h | |
| 35h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B7 | 00h | |
| 36h | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B8 | 00h | |
| 37h ² | HD Gamma B | HD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B9 | 00h | |

NOTES

¹Used for internal test pattern only.

²Programmable gamma correction is not available in PS only mode @ 54 MHz operation.

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| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Value | | |
|---------|--------------------------------|--------------------------------------|-------|-----------------------------------|-------|-------|-------|-------|-------|-------|------------------|-------|-------------|--|
| 38h | HD Adaptive Filter Gain 1 | HD Adaptive Filter Gain 1 Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 00h | | |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | | | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = -8 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = -1 | | | |
| | | | | HD Adaptive Filter Gain 1 Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | | | 1 | 0 | 0 | 0 | | | | | Gain B = -8 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 1 | 1 | 1 | 1 | | | | | Gain B = -1 | |
| 39h | HD Adaptive Filter Gain 2 | HD Adaptive Filter Gain 2 Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 00h | | |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | | | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = -8 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = -1 | | | |
| | | | | HD Adaptive Filter Gain 2 Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | | | 1 | 0 | 0 | 0 | | | | | Gain B = -8 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 1 | 1 | 1 | 1 | | | | | Gain B = -1 | |
| 3Ah | HD Adaptive Filter Gain 3 | HD Adaptive Filter Gain 3 Value A | | | | | 0 | 0 | 0 | 0 | Gain A = 0 | 00h | | |
| | | | | | | | 0 | 0 | 0 | 1 | Gain A = +1 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 0 | 1 | 1 | 1 | Gain A = +7 | | | |
| | | | | | | | 1 | 0 | 0 | 0 | Gain A = -8 | | | |
| | | | | | | | .. | .. | .. | .. | | | | |
| | | | | | | | 1 | 1 | 1 | 1 | Gain A = -1 | | | |
| | | | | HD Adaptive Filter Gain 3 Value B | 0 | 0 | 0 | 0 | | | | | Gain B = 0 | |
| | | | | | 0 | 0 | 0 | 1 | | | | | Gain B = +1 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 0 | 1 | 1 | 1 | | | | | Gain B = +7 | |
| | | | | | 1 | 0 | 0 | 0 | | | | | Gain B = -8 | |
| | | | | | .. | .. | .. | .. | | | | | | |
| | | | | | 1 | 1 | 1 | 1 | | | | | Gain B = -1 | |
| 3Bh | HD Adaptive Filter Threshold A | HD Adaptive Filter Threshold A Value | x | x | x | x | x | x | x | x | Threshold A | 00h | | |
| | | | | | | | | | | | | | | |
| 3Ch | HD Adaptive Filter Threshold B | HD Adaptive Filter Threshold B Value | x | x | x | x | x | x | x | x | Threshold B | 00h | | |
| | | | | | | | | | | | | | | |
| 3Dh | HD Adaptive Filter Threshold C | HD Adaptive Filter Threshold C Value | x | x | x | x | x | x | x | x | Threshold C | 00h | | |
| | | | | | | | | | | | | | | |

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | | |
|------------------------------|--------------------|--------------------------|-------|-------|-------|-------|-------|-------|-------|----------|---------------------------------------|----------------|------------------------------------|--|
| 3Eh | | Reserved | | | | | | | | | | 00h | | |
| 3Fh | | Reserved | | | | | | | | | | 00h | | |
| 40h | SD Mode Register 0 | SD Standard | | | | | | | 0 | 0 | NTSC | 00h | | |
| | | | | | | | | | 0 | 1 | PAL B, D, G, H, I | | | |
| | | | | | | | | | | 1 | 0 | | PAL M | |
| | | | | | | | | | | 1 | 1 | | PAL N | |
| | | SD Luma Filter | | | | | 0 | 0 | 0 | | | | LPF NTSC | |
| | | | | | | | 0 | 0 | 1 | | | | LPF PAL | |
| | | | | | | | 0 | 1 | 0 | | | | Notch NTSC | |
| | | | | | | | 0 | 1 | 1 | | | | Notch PAL | |
| | | | | | | | 1 | 0 | 0 | | | | SSAF Luma | |
| | | | | | | | 1 | 0 | 1 | | | | Luma CIF | |
| | | | | | | | 1 | 1 | 0 | | | | Luma QCIF | |
| | | | | | | | 1 | 1 | 1 | | | | Reserved | |
| | | SD Chroma Filter | 0 | 0 | 0 | | | | | | | | 1.3 MHz | |
| | | | 0 | 0 | 1 | | | | | | | | 0.65 MHz | |
| | | | 0 | 1 | 0 | | | | | | | | 1.0 MHz | |
| | | | 0 | 1 | 1 | | | | | | | | 2.0 MHz | |
| | | | 1 | 0 | 0 | | | | | | | | Reserved | |
| | | | 1 | 0 | 1 | | | | | | | | Chroma CIF | |
| | | | 1 | 1 | 0 | | | | | | | | Chroma QCIF | |
| | | 1 | 1 | 1 | | | | | | | | | 3.0 MHz | |
| 41h | | Reserved | | | | | | | | | | 00h | | |
| 42h | SD Mode Register 1 | SD UV SSAF | | | | | | | 0 | | Disabled | 08h | | |
| | | | | | | | | | 1 | | Enabled | | | |
| | | SD DAC Output 1 | | | | | | | 0 | | Refer to Output Configuration section | | | |
| | | | | | | | | | 1 | | Refer to Output Configuration section | | | |
| | | SD DAC Output 2 | | | | | | 0 | | | Refer to Output Configuration section | | | |
| | | | | | | | | 1 | | | Refer to Output Configuration section | | | |
| | | SD Pedestal | | | | | 0 | | | | Disabled | | | |
| | | | | | | | 1 | | | | Enabled | | | |
| | | SD Square Pixel | | | | 0 | | | | | | | Disabled | |
| | | | | | | 1 | | | | | | | Enabled | |
| SD VCR FF/RW Sync | | | 0 | | | | | | | Disabled | | | | |
| | | | 1 | | | | | | | Enabled | | | | |
| SD Pixel Data Valid | | 0 | | | | | | | | Disabled | | | | |
| | | 1 | | | | | | | | Enabled | | | | |
| SD SAV/EAV Step Edge Control | 0 | | | | | | | | | Disabled | | | | |
| | 1 | | | | | | | | | Enabled | | | | |
| 43h | SD Mode Register 2 | SD Pedestal YPrPb Output | | | | | | | 0 | | No pedestal on YUV | 00h | | |
| | | | | | | | | | 1 | | 7.5 IRE pedestal on YUV | | | |
| | | SD Output Levels Y | | | | | | | | 0 | | Y = 700/300 mV | | |
| | | | | | | | | | | 1 | | Y = 714/286 mV | | |
| | | SD Output Levels PrPb | | | | | 0 | 0 | | | | | 700 mV p-p[PAL]; 1000 mV p-p[NTSC] | |
| | | | | | | | 0 | 1 | | | | | 700 mV p-p | |
| | | | | | | | 1 | 0 | | | | | 1000 mV p-p | |
| | | | | | | | 1 | 1 | | | | | 648 mV p-p | |
| | | SD VBI Open | | | | 0 | | | | | | Disabled | | |
| | | | | | | 1 | | | | | | Enabled | | |
| | | SD CC Field Control | 0 | 0 | | | | | | | | | CC disabled | |
| | | | 0 | 1 | | | | | | | | | CC on odd field only | |
| | | | 1 | 0 | | | | | | | | | CC on even field only | |
| 1 | 1 | | | | | | | | | | CC on both fields | | | |
| | Reserved | 0 | | | | | | | | | Reserved | | | |

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| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | | |
|----------------|------------------|------------------------|-------|-------|-------|-------|-------|-------|----------------------|------------------------------|---|----------------------|---------|----------|
| 44h | SD Mode Register | SD VSYNC-3H | | | | | | | | 0 | Disabled | 00h | | |
| | | | | | | | | | | 1 | VSYNC = 2.5 lines [PAL] VSYNC = 3 lines [NTSC] | | | |
| | | SD RTC/TR/SCR* | | | | | | | | 0 | 0 | Genlock disabled | | |
| | | | | | | | | | | 0 | 1 | Subcarrier reset | | |
| | | | | | | | | | | 1 | 0 | Timing reset | | |
| | | | | | | | | | | 1 | 1 | RTC enabled | | |
| | | SD Active Video Length | | | | | | 0 | | | | 720 pixels | | |
| | | | | | | | | 1 | | | | 710 [NTSC]/702 [PAL] | | |
| | | SD Chroma | | | | | 0 | | | | | Chroma enabled | | |
| | | | | | | | 1 | | | | | Chroma disabled | | |
| | | SD Burst | | | | 0 | | | | | | Enabled | | |
| | | | | | | 1 | | | | | | Disabled | | |
| SD Color Bars | | | 0 | | | | | | | Disabled | | | | |
| | | | 1 | | | | | | | Enabled | | | | |
| SD DAC Swap | | 0 | | | | | | | | DAC B = Luma, DAC C = Chroma | | | | |
| | | 1 | | | | | | | | DAC B = Chroma, DAC C = Luma | | | | |
| 45h | Reserved | | | | | | | | | | 00h | | | |
| 46h | Reserved | | | | | | | | | | 00h | | | |
| 47h | SD Mode Register | SD PrPb Scale | | | | | | | | 0 | Disabled | 00h | | |
| | | | | | | | | | | 1 | Enabled | | | |
| | | SD Y Scale | | | | | | | | 0 | 0 | Disabled | | |
| | | | | | | | | | | 1 | 1 | Enabled | | |
| | | SD Hue Adjust | | | | | | | 0 | | | Disabled | | |
| | | | | | | | | | 1 | | | Enabled | | |
| | | SD Brightness | | | | | | 0 | | | | Disabled | | |
| | | | | | | | | 1 | | | | Enabled | | |
| | | SD Luma SSAF Gain | | | | | 0 | | | | | Disabled | | |
| | | | | | 1 | | | | | Enabled | | | | |
| Reserved | | | | 0 | | | | | | 0 must be written to | | | | |
| Reserved | | | 0 | | | | | | | 0 must be written to | | | | |
| Reserved | | 0 | | | | | | | | 0 must be written to | | | | |
| 48h | SD Mode Register | Reserved | | | | | | | | | | 00h | | |
| | | Reserved | | | | | | | | 0 | 0 must be written to | | | |
| | | SD Double Buffering | | | | | | | | 0 | | Disabled | | |
| | | | | | | | | | | 1 | | Enabled | | |
| | | SD Input Format | | | | | 0 | 0 | | | | 8-bit input | | |
| | | | | | | | 0 | 1 | | | | 16-bit input | | |
| | | | | | | | 1 | 0 | | | | 10-bit input | | |
| | | | | | | | 1 | 1 | | | | 20-bit input | | |
| | | SD Digital Noise | | | | 0 | | | | | | Disabled | | |
| | | | | | | 1 | | | | | | Enabled | | |
| | | SD Gamma Control | | | 0 | | | | | | | Disabled | | |
| | | | 1 | | | | | | | Enabled | | | | |
| SD Gamma Curve | | 0 | | | | | | | | Gamma Curve A | | | | |
| | | 1 | | | | | | | | Gamma Curve B | | | | |
| 49h | SD Mode Register | SD Undershoot Limiter | | | | | | | 0 | 0 | Disabled | 00h | | |
| | | | | | | | | | | 0 | 1 | | -11 IRE | |
| | | | | | | | | | | | 1 | | 0 | -6 IRE |
| | | | | | | | | | | | 1 | | 1 | -1.5 IRE |
| | | Reserved | | | | | | | 0 | | 0 must be written to | | | |
| | | SD Black Burst Output | | | | | | 0 | | | | Disabled | | |
| | | | | | | | | 1 | | | | Enabled | | |
| | | SD Chroma Delay | | | | 0 | 0 | | | | | Disabled | | |
| | | | | | | 0 | 1 | | | | | 4 clk cycles | | |
| | | | | | | 1 | 0 | | | | | 8 clk cycles | | |
| | | | | | | 1 | 1 | | | | | Reserved | | |
| Reserved | | | 0 | | | | | | 0 must be written to | | | | | |
| Reserved | | 0 | | | | | | | 0 must be written to | | | | | |

*See Figure 31, RTC Timing and Connections.

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | |
|--------------------|-------------------------------|---|-------|-------|-------|-------|-------|-------|-------|--|--|-------------|---------------------|
| 4Ah | SD Timing Register 0 | SD Slave/Master Mode | | | | | | | 0 | 0 | Slave mode | 08h | |
| | | | | | | | | | | 1 | 1 | | Master mode |
| | | SD Timing Mode | | | | | | | 0 | 0 | | | Mode 0 |
| | | | | | | | | | 0 | 1 | | | Mode 1 |
| | | | | | | | | | 1 | 0 | | | Mode 2 |
| | | | | | | | | | 1 | 1 | | | Mode 3 |
| | | SD BLANK Input | | | | | | 0 | | | | | Enabled |
| | | | | | | | | 1 | | | | | Disabled |
| | | SD Luma Delay | | | 0 | 0 | | | | | | | No delay |
| | | | | | 0 | 1 | | | | | | | 2 clk cycles |
| | | | | | 1 | 0 | | | | | | | 4 clk cycles |
| | | | | | 1 | 1 | | | | | | | 6 clk cycles |
| SD Min. Luma Value | | 0 | | | | | | | | -40 IRE | | | |
| | | 1 | | | | | | | | -7.5 IRE | | | |
| SD Timing Reset | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A low-high-low transition will reset the internal SD timing counters | | | |
| 4Bh | SD Timing Register 1 | SD HSYNC Width | | | | | | | 0 | 0 | Ta = 1 clk cycle | 00h | |
| | | | | | | | | | | 0 | 1 | | Ta = 4 clk cycles |
| | | | | | | | | | | 1 | 0 | | Ta = 16 clk cycles |
| | | | | | | | | | | 1 | 1 | | Ta = 128 clk cycles |
| | | SD HSYNC to VSYNC delay | | | | | 0 | 0 | | | | | Tb = 0 clk cycle |
| | | | | | | | 0 | 1 | | | | | Tb = 4 clk cycles |
| | | | | | | | 1 | 0 | | | | | Tb = 8 clk cycles |
| | | | | | | | 1 | 1 | | | | | Tb = 18 clk cycles |
| | | SD HSYNC to VSYNC Rising Edge Delay [Mode 1 only] VSYNC Width [Mode 2 only] | | x | 0 | | | | | | | | Tc = Tb |
| | | | | x | 1 | | | | | | | | Tc = Tb + 32 μs |
| | | | | 0 | 0 | | | | | | | | 1 clk cycle |
| | | | | 0 | 1 | | | | | | | | 4 clk cycles |
| | | | 1 | 0 | | | | | | | 16 clk cycles | | |
| | | | 1 | 1 | | | | | | | 128 clk cycles | | |
| | | HSYNC to Pixel Data Adjust | 0 | 0 | | | | | | | | | 0 clk cycles |
| | | | 0 | 1 | | | | | | | | | 1 clk cycle |
| | | | 1 | 0 | | | | | | | | | 2 clk cycles |
| | | | 1 | 1 | | | | | | | | | 3 clk cycles |
| 4Ch | SD F _{SC} Register 0 | | x | x | x | x | x | x | x | x | Subcarrier Frequency Bit 7-0 | 16h | |
| 4Dh | SD F _{SC} Register 1 | | x | x | x | x | x | x | x | x | Subcarrier Frequency Bit 15-8 | 7Ch | |
| 4Eh | SD F _{SC} Register 2 | | x | x | x | x | x | x | x | x | Subcarrier Frequency Bit 23-16 | F0h | |
| 4Fh | SD F _{SC} Register 3 | | x | x | x | x | x | x | x | x | Subcarrier Frequency Bit 31-24 | 21h | |
| 50h | SD F _{SC} Phase | | x | x | x | x | x | x | x | x | Subcarrier Phase Bit 9-2 | 00h | |
| 51h | SD Closed Captioning | Extended Data on Even Fields | x | x | x | x | x | x | x | x | Extended Data Bit 7-0 | 00h | |
| 52h | SD Closed Captioning | Extended Data on Even Fields | x | x | x | x | x | x | x | x | Extended Data Bit 15-8 | 00h | |
| 53h | SD Closed Captioning | Data on Odd Fields | x | x | x | x | x | x | x | x | Data Bit 7-0 | 00h | |
| 54h | SD Closed Captioning | Data on Odd Fields | x | x | x | x | x | x | x | x | Data Bit 15-8 | 00h | |
| 55h | SD Pedestal Register 0 | Pedestal on Odd Fields | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | Setting any of these bits to 1 will disable pedestal on the line number indicated by the bit settings. | 00h | |
| 56h | SD Pedestal Register 1 | Pedestal on Odd Fields | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | | 00h | |
| 57h | SD Pedestal Register 2 | Pedestal on Even Fields | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 00h | |
| 58h | SD Pedestal Register 3 | Pedestal on Even Fields | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | | 00h | |



Figure 20. Timing Register 1 in PAL Mode

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| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | |
|---------|-------------------|----------------------------------|-------------|-------|-------|-------|-------|--------------|--------------|------------|---|--|----------|
| 59h | SD CGMS/WSS 0 | SD CGMS Data | | | | | 19 | 18 | 17 | 16 | CGMS Data Bits C19-C16 | 00h | |
| | | SD CGMS CRC | | | | 0 | | | | | Disabled | | |
| | | | | | | 1 | | | | | Enabled | | |
| | | SD CGMS on Odd | | | 0 | | | | | | Disabled | | |
| | | | | | 1 | | | | | | Enabled | | |
| | SD CGMS on Even | | 0 | | | | | | | Disabled | | | |
| | | | 1 | | | | | | | Enabled | | | |
| | SD WSS | | 0 | | | | | | | Disabled | | | |
| | | | 1 | | | | | | | Enabled | | | |
| 5Ah | SD CGMS/WSS 1 | SD CGMS/WSS Data | | | 13 | 12 | 11 | 10 | 9 | 8 | CGMS Data Bits C13-C8 or WSS Data Bits C13-C8 | 00h | |
| | | | | 15 | 14 | | | | | | | CGMS Data Bits C15-C14 | 00h |
| 5Bh | SD CGMS/WSS 2 | SD CGMS/WSS Data | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | CGMS/WSS Data Bits C7-C0 | 00h | |
| 5Ch | SD LSB Register | SD LSB for Y Scale | | | | | | | x | x | SD Y Scale Bit 1-0 | | |
| | | SD LSB for U Scale | | | | | x | x | | | SD U Scale Bit 1-0 | | |
| | | SD LSB for V Scale | | | x | x | | | | | SD V Scale Bit 1-0 | | |
| | | SD LSB for F _{SC} Phase | x | x | | | | | | | Subcarrier Phase Bits 1-0 | | |
| 5Dh | SD Y Scale | SD Y Scale Value | x | x | x | x | x | x | x | x | SD Y Scale Bit 7-2 | 00h | |
| 5Eh | SD V Scale | SD V Scale Value | x | x | x | x | x | x | x | x | SD V Scale Bit 7-2 | 00h | |
| 5Fh | SD U Scale | SD U Scale Value | x | x | x | x | x | x | x | x | SD U Scale Bit 7-2 | 00h | |
| 60h | SD Hue Register | SD Hue Adjust Value | x | x | x | x | x | x | x | x | SD Hue Adjust Bit 7-0 | 00h | |
| 61h | SD Brightness/WSS | SD Brightness Value | | x | x | x | x | x | x | x | SD Brightness Bit 6-0 | 00h | |
| | | SD Blank WSS Data | 0 | | | | | | | | | Disabled | Line 23 |
| | | | 1 | | | | | | | | Enabled | | |
| 62h | SD Luma SSAF | SD Luma SSAF Gain/Attenuation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -4 dB | 00h |
| | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 dB | |
| | | | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | +4 dB | |
| 63h | SD DNR 0 | Coring Gain Border | | | | | 0 | 0 | 0 | 0 | No gain | 00h | |
| | | | | | | | 0 | 0 | 0 | 1 | +1/16 [-1/8] | | |
| | | | | | | | 0 | 0 | 1 | 0 | +2/16 [-2/8] | | |
| | | | | | | | 0 | 0 | 1 | 1 | +3/16 [-3/8] | | |
| | | | | | | | 0 | 1 | 0 | 0 | +4/16 [-4/8] | | |
| | | | | | | | 0 | 1 | 0 | 1 | +5/16 [-5/8] | | |
| | | | | | | | 0 | 1 | 1 | 0 | +6/16 [-6/8] | | |
| | | | | | | | 0 | 1 | 1 | 1 | +7/16 [-7/8] | | |
| | | | | | | 1 | 0 | 0 | 0 | +8/16 [-1] | | | |
| | | Coring Gain Data | 0 | 0 | 0 | 0 | | | | | No gain | In DNR Mode the values in brackets apply | |
| | | | 0 | 0 | 0 | 1 | | | | | +1/16 [-1/8] | | |
| | | | 0 | 0 | 1 | 0 | | | | | +2/16 [-2/8] | | |
| | | | 0 | 0 | 1 | 1 | | | | | +3/16 [-3/8] | | |
| | | | 0 | 1 | 0 | 0 | | | | | +4/16 [-4/8] | | |
| 0 | 1 | | 0 | 1 | | | | | +5/16 [-5/8] | | | | |
| 0 | 1 | 1 | 0 | | | | | +6/16 [-6/8] | | | | | |
| 0 | 1 | 1 | 1 | | | | | +7/16 [-7/8] | | | | | |
| 1 | 0 | 0 | 0 | | | | | +8/16 [-1] | | | | | |
| 64h | SD DNR 1 | DNR Threshold | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | |
| | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| | | | | | ... | ... | ... | ... | ... | ... | ... | | |
| | | | | | 1 | 1 | 1 | 1 | 1 | 0 | 62 | | |
| | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 63 | | |
| | | | Border Area | 0 | | | | | | | | | 2 pixels |
| | | | | 1 | | | | | | | | | 4 pixels |
| | | 0 | | | | | | | | | 8 pixels | | |
| | | Block Size Control | 1 | | | | | | | | 16 pixels | | |

| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value | |
|---------|----------------------|------------------------------|-------|-------|-------|-------|-------|-------|-------|-----------------|--|-------------|--------------------|
| 65h | SD DNR 2 | DNR Input Select | | | | | | 0 | 0 | 1 | Filter A | 00h | |
| | | | | | | | | 0 | 1 | 0 | Filter B | | |
| | | | | | | | | 0 | 1 | 1 | Filter C | | |
| | | | | | | | | 1 | 0 | 0 | Filter D | | |
| | | DNR Mode | | | | 0 | | | | | | | DNR mode |
| | | | | | | 1 | | | | | | | DNR Sharpness mode |
| | | DNR Block Offset | 0 | 0 | 0 | 0 | | | | | | | 0 pixel offset |
| | | | 0 | 0 | 0 | 1 | | | | | | | 1 pixel offset |
| ... | ... | | ... | ... | | | | | | ... | | | |
| 1 | 1 | | 1 | 0 | | | | | | 14 pixel offset | | | |
| | | | 1 | 1 | 1 | 1 | | | | 15 pixel offset | | | |
| 66h | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A0 | 00h | |
| 67h | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A1 | 00h | |
| 68h | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A2 | 00h | |
| 69h | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A3 | 00h | |
| 6Ah | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A4 | 00h | |
| 6Bh | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A5 | 00h | |
| 6Ch | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A6 | 00h | |
| 6Dh | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A7 | 00h | |
| 6Eh | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A8 | 00h | |
| 6Fh | SD Gamma A | SD Gamma Curve A Data Points | x | x | x | x | x | x | x | x | A9 | 00h | |
| 70h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B0 | 00h | |
| 71h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B1 | 00h | |
| 72h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B2 | 00h | |
| 73h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B3 | 00h | |
| 74h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B4 | 00h | |
| 75h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B5 | 00h | |
| 76h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B6 | 00h | |
| 77h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B7 | 00h | |
| 78h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B8 | 00h | |
| 79h | SD Gamma B | SD Gamma Curve B Data Points | x | x | x | x | x | x | x | x | B9 | 00h | |
| 7Ah | SD Brightness Detect | SD Brightness Value | x | x | x | x | x | x | x | x | Read only | | |
| 7Bh | Field Count Register | Field Count | | | | | | x | x | x | Read only | | |
| | | Reserved | | | | | 0 | | | | 0 must be written to this | | |
| | | Reserved | | | | 0 | | | | | 0 must be written to this | | |
| | | Reserved | | | 0 | | | | | | 0 must be written to this | | |
| | | Revision Code | x | x | | | | | | | | Read Only | |
| 7Ch | 10-Bit Input | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Must write this for 10 bit Data Input (SD, PS, HD) | 00h | |

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| SR7-SR0 | Register | Bit Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register Setting | Reset Value |
|---------|-------------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------------------|-------------|
| 7Dh | Reserved | | | | | | | | | | | |
| 7Eh | Reserved | | | | | | | | | | | |
| 7Fh | Reserved | | | | | | | | | | | |
| 80h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 81h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 82h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 83h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 84h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 85h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 86h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 87h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 88h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 89h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Ah | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Bh | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Ch | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Dh | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Eh | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 8Fh | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 90h | Macrovision | MV Control Bits | x | x | x | x | x | x | x | x | | 00h |
| 91h | Macrovision | MV Control Bit | | | | | | | | x | | 00h |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 must be written to bits | |

INPUT CONFIGURATION

When 10-bit input data is applied, the following bits must be set to 1:

Address 0x7C, Bit 1 (Global 10-Bit Enable)

Address 0x13, Bit 2 (HD 10-Bit Enable)

Address 0x48, Bit 4 (SD 10-Bit Enable)

Note that the ADV7314 defaults to simultaneous standard definition and progressive scan on power-up. Address[01h]: Input Mode = 011.

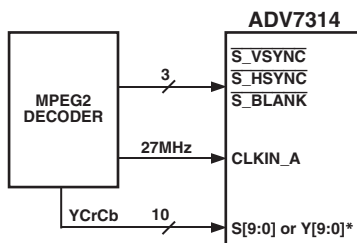
Standard Definition Only

Address [01h] Input Mode = 000

The 8-bit/10-bit multiplexed input data is input on Pins S9–S0 (or Y9–Y0, depending on Register Address 0x01, Bit7), with S0 being the LSB in 10-bit input mode. Input standards supported are ITU-R BT.601/656.

In 16-bit input mode, the Y pixel data is input on Pins S9–S2, and CrCb data is input on Pins C9–C2. The 27 MHz clock input must be input on the CLKIN_A pin.

Input sync signals are optional and are input on the $\overline{S_VSYNC}$, $\overline{S_HSYNC}$, and $\overline{S_BLANK}$ pins.



*Selected by Address 0x01 Bit 7

Figure 21 . SD Only Input Mode

Progressive Scan Only or HDTV Only

Address [01h] Input Mode 001 or 010, Respectively

YCrCb Progressive Scan, HDTV, or any other HD YCrCb data can be input in 4:2:2 or 4:4:4. In 4:2:2 input mode, the Y data is input on Pins Y9–Y0 and the CrCb data on Pins C9–C0. In 4:4:4 input mode, Y data is input on Pins Y9–Y0, Cb data on Pins C9–C0, and Cr data on Pins S9–S0.

If the YCrCb data does not conform to SMPTE 293M (525p), ITU-R BT.1358M (625p), SMPTE 274M (1080i), SMPTE 296M (720p), or BTA T-1004/1362, the async timing mode must be used.

RGB data can be input in 4:4:4 format in PS Input mode only or in HDTV Input mode only when HD RGB input is enabled. G data is input on Pins Y9–Y0, R data on S9–S0, and B data on C9–C0.

The clock signal must be input on the CLKIN_A pin.

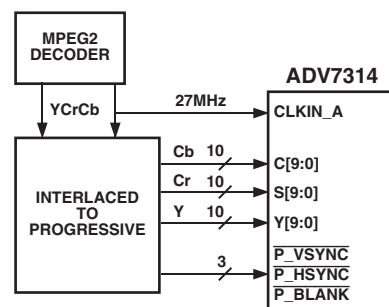


Figure 22. Progressive Scan Input Mode

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Simultaneous Standard Definition and Progressive Scan or HDTV

Address [01h]: Input Mode 011 (SD 40-Bit, PS 20-Bit) or 101 (SH and HD, SD Oversampled), 110 (SD and HD, HD Oversampled)

YCrCb PS, HDTV, or any other HD data must be input in 4:2:2 format. In 4:2:2 input mode, the HD Y data is input on Pins Y9–Y0 and the HD CrCb data on C9–C0.

If PS 4:2:2 data is interleaved onto a single 10-bit bus, Y9–Y0 are used for the input port. The input data is to be input at 27 MHz with the data clocked on the rising and falling edge of the input clock. The input mode register at Address 01h is set accordingly.

If the YCrCb data does not conform to SMPTE 293M (525p), ITU-R BT.1358M (625p), SMPTE 274M (1080i), SMPTE 296M (720p), or BTA T-1004, the Async Timing mode must be used.

The 8-bit or 10-bit standard definition data must be compliant to ITU-R BT.601/656 in 4:2:2 format.

Standard definition data is input on Pins S9–S0, with S0 being the LSB. Using 8-bit input format, the data is input on Pins S9–S2.

The clock input for SD must be input on CLKIN_A, and the clock input for HD must be input on CLKIN_B.

Synchronization signals are optional. SD syncs are input on pins $\overline{S_VSYNC}$, $\overline{S_HSYNC}$, and $\overline{S_BLANK}$.

HD syncs are input on Pins $\overline{P_VSYNC}$, $\overline{P_HSYNC}$, $\overline{P_BLANK}$.

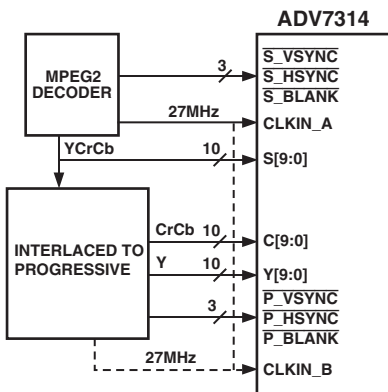


Figure 23. Simultaneous PS and SD Input

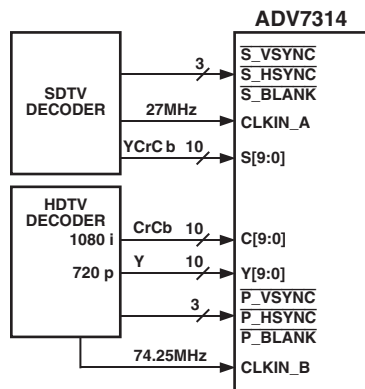


Figure 24. Simultaneous HD and SD Input

If in simultaneous SD/HD input mode, the two clock phases differ by less than 9.25 ns or more than 27.75 ns, the CLOCK

ALIGN bit [Address 01h, Bit 3] must be set accordingly. If the application uses the same clock source for both SD and PS, the CLOCK ALIGN bit must be set since the phase difference between both inputs is less than 9.25 ns.

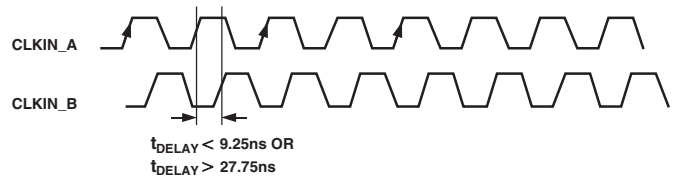


Figure 25. Clock Phase with Two Input Clocks

Progressive Scan at 27 MHz (Dual Edge) or 54 MHz Address [01h]: Input Mode 100 OR 111, Respectively

YCrCb progressive scan data can be input at 27 MHz or 54 MHz. The input data is interleaved onto a single 8-/10-bit bus and is input on Pins Y9–Y0. When a 27 MHz clock is supplied, the data is clocked in on the rising and falling edge of the input clock and CLOCK EDGE [Address 01h, Bit 1] must be set accordingly.

The following figures show the possible conditions. (a) Cb data on the rising edge and (b) Y data on the rising edge.

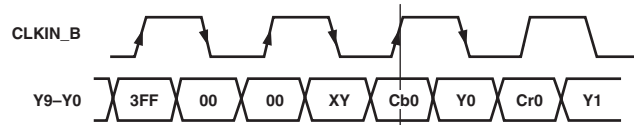


Figure 26a. Clock Edge Address 01h, Bit 1 Should Be Set to 0

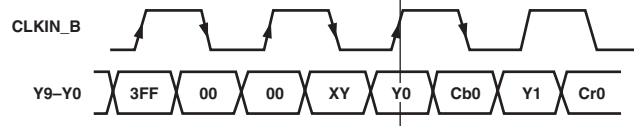


Figure 26b. Clock Edge Address 01h, Bit 1 Should Be Set to 1

With a 54 MHz clock, the data is latched on the every rising edge.

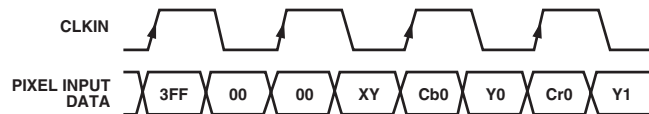


Figure 26c. Input Sequence in PS Bit Interleaved Mode, EAV/SAV Followed by Cb0 Data

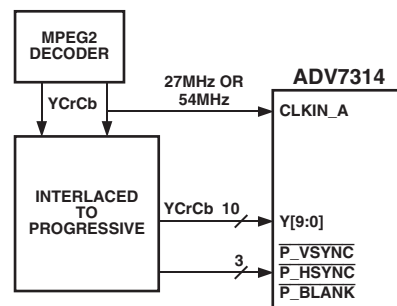


Figure 27. 1x 10-Bit PS at 27 MHz or 54 MHz

Table I provides an overview of all possible input configurations.

Table I. Input Configurations

| Input Format | Total Bits | | Input Video | Input Pins | Subaddress | Register Setting |
|-----------------------------|-------------------|-------|------------------|------------------|------------|-------------------|
| ITU-R BT.656 | 8 | 4:2:2 | YCrCb | S9-S2 [MSB = S9] | 01h 48h | 00h 00h |
| | 10 | 4:2:2 | YCrCb | S9-S0 [MSB = S9] | 01h 48h | 00h 10h |
| | 16 | 4:2:2 | Y | S9-S2 [MSB = S9] | 01h | 00h |
| | | | CrCb | Y9-Y2 [MSB = Y9] | 48h | 08h |
| | 20 | 4:2:2 | Y | S9-S0 [MSB = S9] | 01h | 00h |
| | | | CrCb | Y9-Y0 [MSB = Y9] | 48h | 18h |
| 8 | 4:2:2 | YCrCb | Y9-Y2 [MSB = Y9] | 01h 48h | 80h 00h | |
| 10 | 4:2:2 | YCrCb | Y9-Y0 [MSB = Y9] | 01h 48h | 80h 10h | |
| PS Only | 8 [27 MHz clock] | 4:2:2 | YCrCb | Y9-Y2 [MSB = Y9] | 01h 13h | 10h 40h |
| | 10 [27 MHz clock] | 4:2:2 | YCrCb | Y9-Y0 [MSB = Y9] | 01h 13h | 10h 44h |
| | 8 [54 MHz clock] | 4:2:2 | YCrCb | Y9-Y2 [MSB = Y9] | 01h 13h | 70h 40h |
| | 10 [54 MHz clock] | 4:2:2 | YCrCb | Y9-Y0 [MSB = Y9] | 70h 13h | 10h 44h |
| | | | Y | Y9-Y2 [MSB = Y9] | 01h | 10h |
| | 16 | 4:2:2 | CrCb | C9-C2 [MSB = C9] | 13h | 40h |
| | | | Y | Y9-Y0 [MSB = Y9] | 01h | 10h |
| | 20 | 4:2:2 | CrCb | C9-C0 [MSB = C9] | 13h | 44h |
| | | | Y | Y9-Y2 [MSB = Y9] | 01h | 10h |
| | 24 | 4:4:4 | Cr | S9-S2 [MSB = S9] | 13h | 00h |
| Y | | | Y9-Y0 [MSB = Y9] | 01h | 10h | |
| CrCb | | | C9-C2 [MSB = C9] | 13h | 00h | |
| 30 | 4:4:4 | Y | Y9-Y0 [MSB = Y9] | 01h | 10h | |
| | | CrCb | C9-C0 [MSB = C9] | 13h | 04h | |
| | | Cr | S9-S0 [MSB = S9] | 13h | 04h | |
| HDTV Only | 16 | 4:2:2 | Y | Y9-Y2 [MSB = Y9] | 01h | 20h |
| | | | CrCb | C9-Y2 [MSB = C9] | 13h | 40h |
| | 20 | 4:2:2 | Y | Y9-Y0 [MSB = Y9] | 01h | 20h |
| | | | CrCb | C9-C0 [MSB = C9] | 13h | 44h |
| | 24 | 4:4:4 | Y | Y9-Y2 [MSB = Y9] | 01h | 20h |
| | | | CrCb | C9-Y2 [MSB = C9] | 13h | 00h |
| | | | Cr | S9-S2 [MSB = S9] | 13h | 00h |
| | 30 | 4:4:4 | Y | Y9-Y0 [MSB = Y9] | 01h | 20h |
| | | | CrCb | C9-C0 [MSB = C9] | 13h | 04h |
| | | | Cr | S9-S0 [MSB = S9] | 13h | 04h |
| HD RGB | 24 | 4:4:4 | G | Y9-Y2 [MSB = Y9] | 01h | 10h or 20h |
| | | | B | C9-C2 [MSB = C9] | 13h | 00h |
| | | | R | S9-S2 [MSB = S9] | 15h | 02h |
| | 30 | 4:4:4 | G | Y9-Y0 [MSB = Y9] | 01h | 10h or 20h |
| | | | B | C9-C0 [MSB = C9] | 13h | 04h |
| | | | R | S9-S0 [MSB = S9] | 15h | 02h |
| ITU-R BT.656 and PS | 8 | 4:2:2 | YCrCb | S9-S2 [MSB = S9] | 01h | 40h |
| | 8 | 4:2:2 | YCrCb | Y9-Y2 [MSB = Y9] | 13h 48h | 40h 00h |
| ITU-R BT.656 and PS | 10 | 4:2:2 | YCrCb | S9-S0 [MSB = S9] | 01h | 40h |
| | 10 | 4:2:2 | YCrCb | Y9-Y0 [MSB = Y9] | 13h 48h | 44h 10h |
| ITU-R BT.656 and PS or HDTV | 8 | 4:2:2 | YCrCb | S9-S2 [MSB = S9] | 01h | 30h or 50h or 60h |
| | 16 | 4:2:2 | Y | Y9-Y2 [MSB = Y9] | 13h | 60h |
| | | | CrCb | C9-C2 [MSB = C9] | 48h | 00h |
| ITU-R BT.656 and PS or HDTV | 10 | 4:2:2 | YCrCb | S9-S0 [MSB = S9] | 01h | 30h or 50h or 60h |
| | 20 | 4:2:2 | Y | Y9-Y0 [MSB = Y9] | 13h 48h | 60h 10h |

ADV7314

OUTPUT CONFIGURATION

These tables show which output signals are assigned to the DACs when the control bits are set accordingly.

Table II. Output Configuration in SD Only Mode

| RGB/YUV Output 02h, Bit 5 | SD DAC Output 1 42h, Bit 2 | SD DAC Output 2 42h, Bit 1 | DAC A | DAC B | DAC C | DAC D | DAC E | DAC F |
|---------------------------|----------------------------|----------------------------|-------|-------|--------|-------|-------|--------|
| 0 | 0 | 0 | CVBS | Luma | Chroma | G | B | R |
| 0 | 0 | 1 | G | B | R | CVBS | Luma | Chroma |
| 0 | 1 | 0 | G | Luma | Chroma | CVBS | B | R |
| 0 | 1 | 1 | CVBS | B | R | G | Luma | Chroma |
| 1 | 0 | 0 | CVBS | Luma | Chroma | Y | U | V |
| 1 | 0 | 1 | Y | U | V | CVBS | Luma | Chroma |
| 1 | 1 | 0 | Y | Luma | Chroma | CVBS | U | V |
| 1 | 1 | 1 | CVBS | U | V | Y | Luma | Chroma |

| Luma/Chroma Swap 44h, Bit 7 | |
|-----------------------------|--|
| 0 | Table as above |
| 1 | Table above with all Luma/Chroma instances swapped |

Table III. Output Configuration in HD/PS Only Mode

| HD Input Format | HD RGB Input 15h, Bit 1 | RGB/YPrPb Output 02h, Bit 5 | HD Color Swap 15h, Bit 3 | DAC A | DAC B | DAC C | DAC D | DAC E | DAC F |
|-----------------|-------------------------|-----------------------------|--------------------------|-------|-------|-------|-------|-------|-------|
| YCrCb 4:2:2 | 0 | 0 | 0 | N/A | N/A | N/A | G | B | R |
| YCrCb 4:2:2 | 0 | 0 | 1 | N/A | N/A | N/A | G | R | B |
| YCrCb 4:2:2 | 0 | 1 | 0 | N/A | N/A | N/A | Y | Pb | Pr |
| YCrCb 4:2:2 | 0 | 1 | 1 | N/A | N/A | N/A | Y | Pr | Pb |
| YCrCb 4:4:4 | 0 | 0 | 0 | N/A | N/A | N/A | G | B | R |
| YCrCb 4:4:4 | 0 | 0 | 1 | N/A | N/A | N/A | G | R | B |
| YCrCb 4:4:4 | 0 | 1 | 0 | N/A | N/A | N/A | Y | Pb | Pr |
| YCrCb 4:4:4 | 0 | 1 | 1 | N/A | N/A | N/A | Y | Pr | Pb |
| RGB 4:4:4 | 1 | 0 | 0 | N/A | N/A | N/A | G | B | R |
| RGB 4:4:4 | 1 | 0 | 1 | N/A | N/A | N/A | G | R | B |
| RGB 4:4:4 | 1 | 1 | 0 | N/A | N/A | N/A | G | B | R |
| RGB 4:4:4 | 1 | 1 | 1 | N/A | N/A | N/A | G | R | B |

Table IV. Output Configuration in Simultaneous SD and HD/PS Mode

| Input Formats | RGB/YPrPb Output 02h, Bit 5 | HD Color Swap 15h, Bit 3 | DAC A | DAC B | DAC C | DAC D | DAC E | DAC F |
|------------------------------------|-----------------------------|--------------------------|-------|-------|--------|-------|-------|-------|
| ITU-R BT.656 and HD YCrCb in 4:2:2 | 0 | 0 | CVBS | Luma | Chroma | G | B | R |
| ITU-R BT.656 and HD YCrCb in 4:2:2 | 0 | 1 | CVBS | Luma | Chroma | G | R | B |
| ITU-R BT.656 and HD YCrCb in 4:2:2 | 1 | 0 | CVBS | Luma | Chroma | Y | Pb | Pr |
| ITU-R BT.656 and HD YCrCb in 4:2:2 | 1 | 1 | CVBS | Luma | Chroma | Y | Pr | Pb |

TIMING MODES

HD Async Timing Mode

[Subaddress 10h, Bit 3,2]

For any input data that does not conform to the standards selectable in input mode, Subaddress 01h, asynchronous timing mode can be used to interface to the ADV7314. Timing control signals for $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ have to be programmed by the user. Macrovision and programmable

oversampling rates are not available in async timing mode. When using async mode, the PLL must be turned off [Subaddress 00h, Bit 1 = 1].

Figures 28a and 28b show an example of how to program the ADV7314 to accept a different high definition standard other than SMPTE 293M, SMPTE 274M, SMPTE 296M, or ITU-R BT.1358. The truth table in Table V must be followed when programming the control signals in async timing mode.

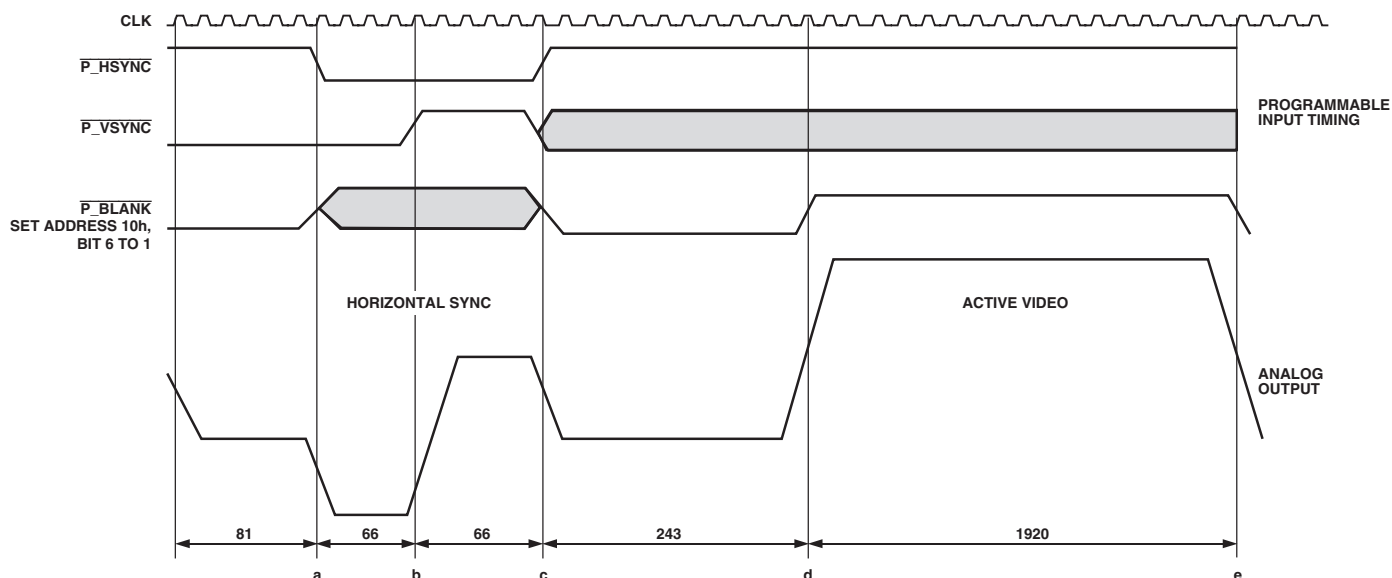


Figure 28a. Async Timing Mode—Programming Input Control Signals for SMPTE 295M Compatibility

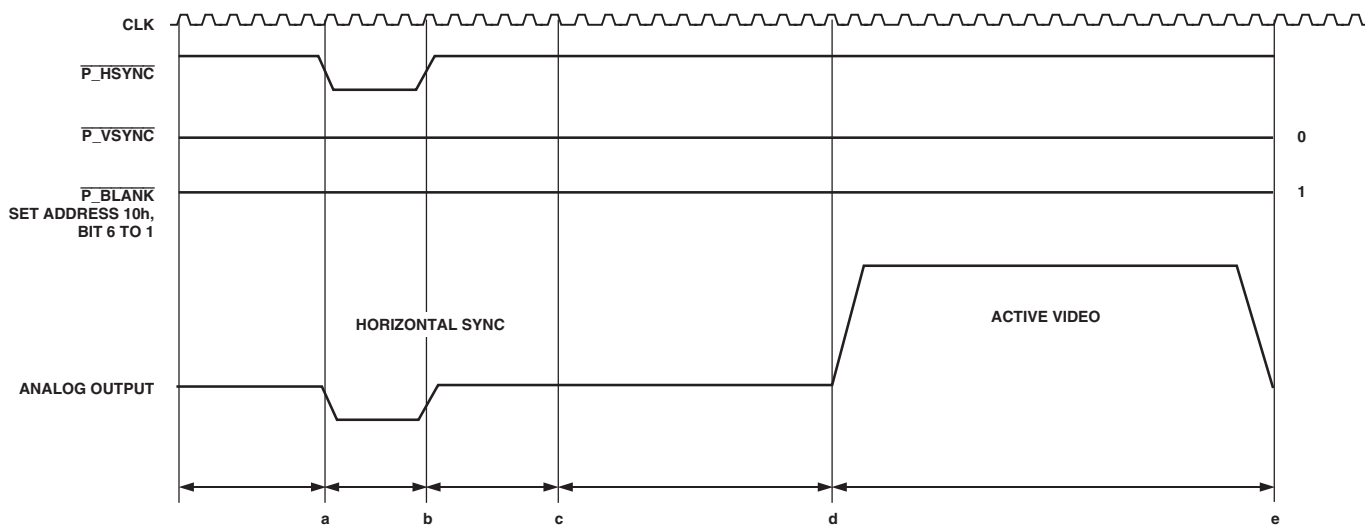


Figure 28b. Async Timing Mode—Programming Input Control Signals for Bilevel Sync Signal

ADV7314

Table V. Async Timing Mode Truth Table

| $\overline{\text{P_HSYNC}}$ | $\overline{\text{P_VSYNC}}$ | $\overline{\text{P_BLANK}}^*$ | | Reference in Figures 28a and 28b |
|------------------------------|------------------------------|--------------------------------|---|-------------------------------------|
| 1 -> 0 | 0 | 0 or 1 | 50% point of falling edge of tri-level horizontal sync signal | a |
| 0 | 0 -> 1 | 0 or 1 | 25% point of rising edge of tri-level horizontal sync signal | b |
| 0 -> 1 | 0 or 1 | 0 | 50% point of falling edge of tri-level horizontal sync signal | c |
| 1 | 0 or 1 | 0 -> 1 | 50% start of active video | d |
| 1 | 0 or 1 | 1 -> 0 | 50% end of active video | e |

*When async timing mode is enabled, $\overline{\text{P_BLANK}}$ [Pin 25] becomes an active high input. $\overline{\text{P_BLANK}}$ is set to active low at Address 10h, Bit 6. For standards that do not require a tri-sync level, $\overline{\text{P_BLANK}}$ must be tied low at all times.

HD Timing Reset

[Subaddress 14h, Bit 0]

A timing reset is achieved in setting the HD timing reset control bit at Address 14h from 0 to 1. In this state, the horizontal and vertical counters will remain reset. On setting this bit back to 0, the internal counters will commence counting again.

The minimum time the pin has to be held high is one clock cycle, otherwise this reset signal might not be recognized. This timing reset applies to the HD timing counters only.

SD Real-Time Control, Subcarrier Reset, and Timing Reset [Subaddress 44h, Bit 2,1]

Together with the RTC_SCR_TR pin and SD Mode Register 3, the ADV7314 can be used in timing reset mode, subcarrier phase reset mode, or RTC mode.

Timing Reset Mode

A timing reset is achieved in a low-to-high transition on the RTC_SCR_TR pin (Pin 31). In this state, the horizontal and vertical counters will remain reset. On releasing this pin (set to low), the internal counters will commence counting again, the field count will start on Field 1, and the subcarrier phase will be reset.

The minimum time the pin has to be held high is one clock cycle; otherwise this reset signal might not be recognized. This timing reset applies to the SD timing counters only.

Subcarrier Phase Reset

A low-to-high transition on the RTC_SCR_TR pin (Pin 31) will reset the subcarrier phase to zero on the field following the subcarrier phase reset when the SD RTC/TR/SCR control bits at Address 44h are set to 01.

This reset signal will have to be held high for a minimum of one clock cycle.

Since the field counter is not reset, it is recommended that the reset signal should be applied in Field 7 [PAL] or Field 3 [NTSC]. The reset of the phase will then occur on the next field, i.e., Field 1, being lined up correctly with the internal counters. The field count register at Address 7Bh can be used to identify the number of the active field.

RTC Mode

In RTC mode, the ADV7314 can be used to lock to an external video source. The real-time control mode allows the ADV7314 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device that outputs a digital datastream in the RTC format (such as an ADV7183A video decoder, see Figure 31), the part will automatically change to the compensated subcarrier frequency on a line by line basis. This digital datastream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. 00h should be written into all four subcarrier frequency registers when using this mode.

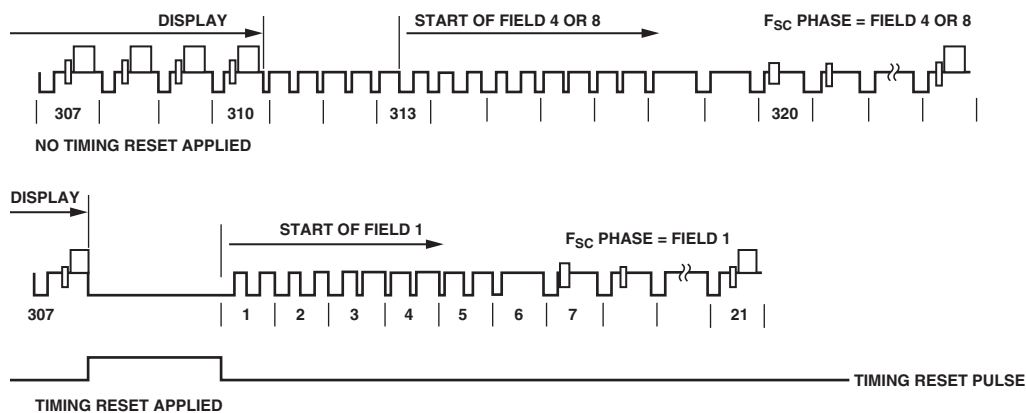


Figure 29. Timing Reset Timing Diagram

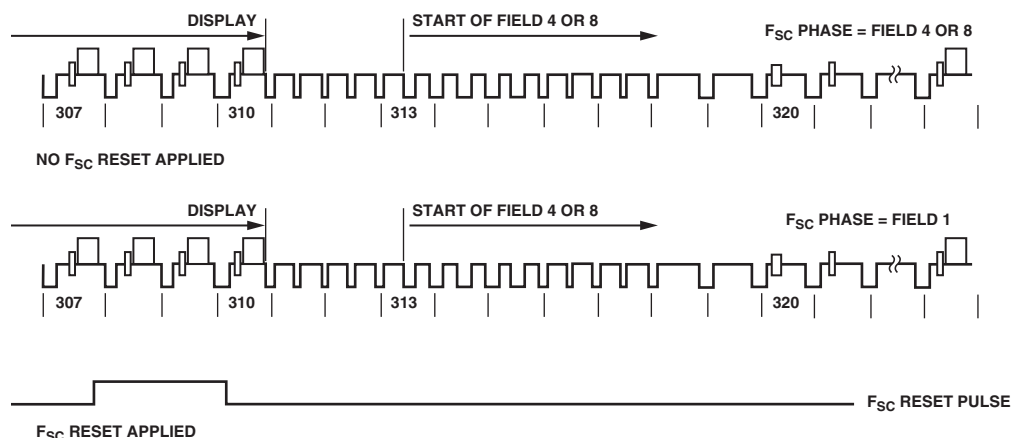


Figure 30. Subcarrier Reset Timing Diagram

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Reset Sequence

A reset is activated with a high-to-low transition on the $\overline{\text{RESET}}$ pin [Pin 33] according to the timing specifications. The ADV7314 will revert to the default output configuration. Figure 32 illustrates the $\overline{\text{RESET}}$ sequence timing.

SD VCR FF/RW Sync

[Subaddress 42h, Bit 5]

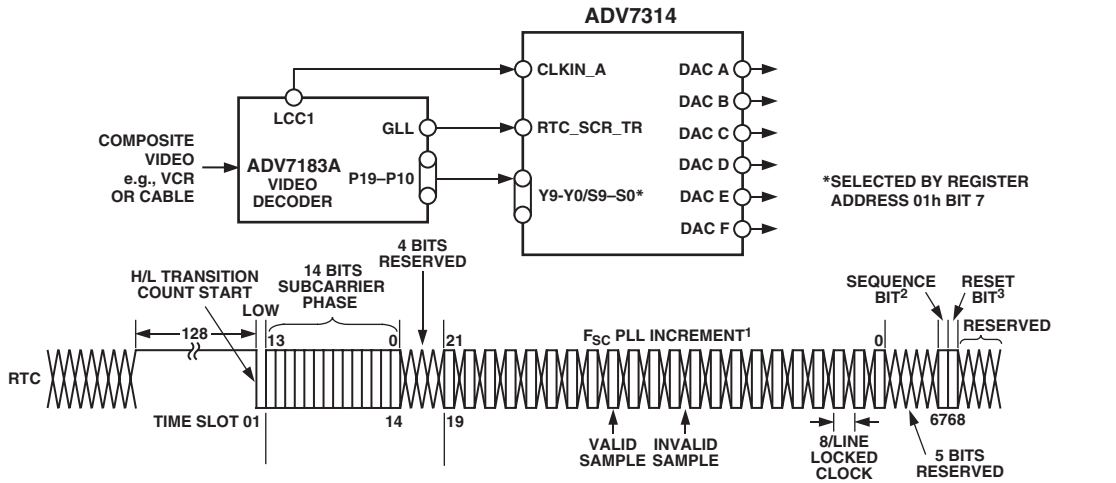
In DVD record applications where the encoder is used with a decoder, the VCR FF/RW Sync control bit can be used for non-standard input video, i.e., in fast forward or rewind modes.

In fast forward mode, the sync information at the start of a new field in the incoming video usually occurs before the correct number of lines/field are reached. In rewind mode, this sync

signal usually occurs after the total number of lines/field are reached. Conventionally this means that the output video will have corrupted field signals, one generated by the incoming video and one when the internal lines/field counters reach the end of a field.

When the VCR FF/RW sync control is enabled [Subaddress 42h, Bit 5] the lines/field counters are updated according to the incoming $\overline{\text{VSYNC}}$ signal and the analog output matches the incoming $\overline{\text{VSYNC}}$ signal.

This control is available in all slave timing modes except Slave Mode 0.



NOTES

¹F_{sc} PLL INCREMENT IS 22 BITS LONG. VALUE LOADED INTO ADV7314 F_{sc} DDS REGISTER IS F_{sc} PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7314.

²SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED; NTSC: 0 = NO CHANGE

³SEQUENCE BIT
RESET ADV7314 DDS

Figure 31. RTC Timing and Connections

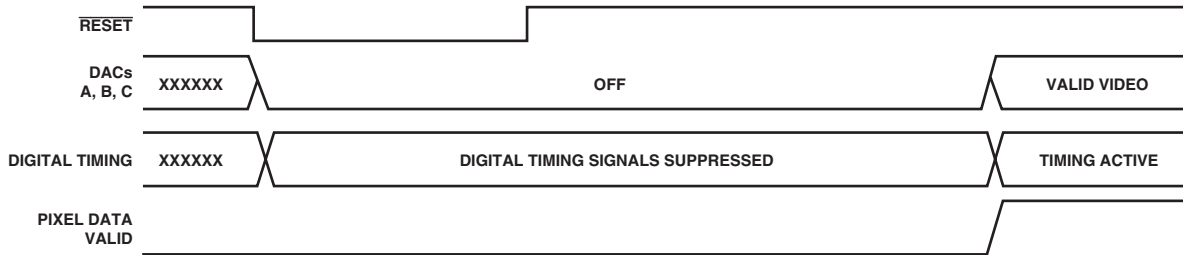


Figure 32. $\overline{\text{RESET}}$ Timing Sequence

Vertical Blanking Interval

The ADV7314 accepts input data that contains VBI data [e.g., CGMS, WSS, VITS] in SD and HD modes.

For SMPTE 293M [525p] standards, VBI data can be inserted on Lines 13 to 42 of each frame, or Lines 6 to 43 for ITU-R BT.1358 [625p] standard. For SD NTSC, this data can be present on Lines 10 to 20, and in PAL on Lines 7 to 22.

If VBI is disabled [Address 11h, Bit 4 for HD; Address 43h, Bit 4 for SD], VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave modes.

In Slave Mode 0, if VBI is enabled, the blanking bit in the EAV/SAV code is overwritten; it is possible to use VBI in this timing mode as well.

In Slave mode 1 or 2, the $\overline{\text{BLANK}}$ control bit must be set to enabled [Address 4Ah, Bit 3] to allow VBI data to pass through the ADV7314; otherwise the ADV7314 automatically blanks the VBI to standard.

If CGMS is enabled and VBI is disabled, the CGMS data will nevertheless be available at the output.

SD Subcarrier Frequency Registers

[Subaddress 4Ch-4Fh]

Four 8-bit registers are used to set up the subcarrier frequency. The value of these registers is calculated in using the following equation:

$$\text{Subcarrier Frequency Register} = \frac{\# \text{Subcarrier Frequency Value}}{\# 27 \text{ MHz clk cycles in one video line}} \times 2^{23}$$

For example, in NTSC mode,

$$\text{Subcarrier Frequency Value} = \left(\frac{227.5}{1716} \right) \times 2^{23} = 569408542$$

SD F_{SC} Register 0: 1Eh

SD F_{SC} Register 1: 7Ch

SD F_{SC} Register 2: F0h

SD F_{SC} Register 3: 21h

Refer to the MPU Port Description section for more details on how to access the subcarrier frequency registers.

Square Pixel Timing [Register 42h, Bit 4]

In square pixel mode, the following timing diagrams apply.

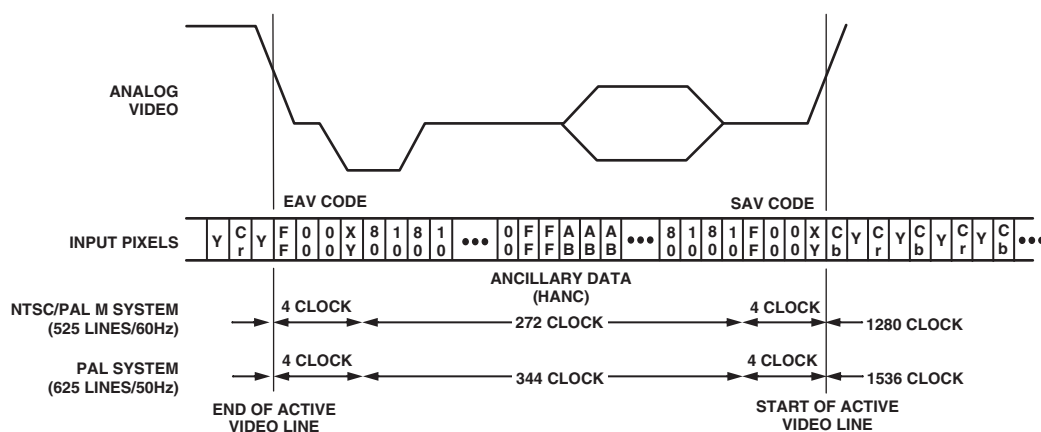


Figure 33. EAV/SAV Embedded Timing

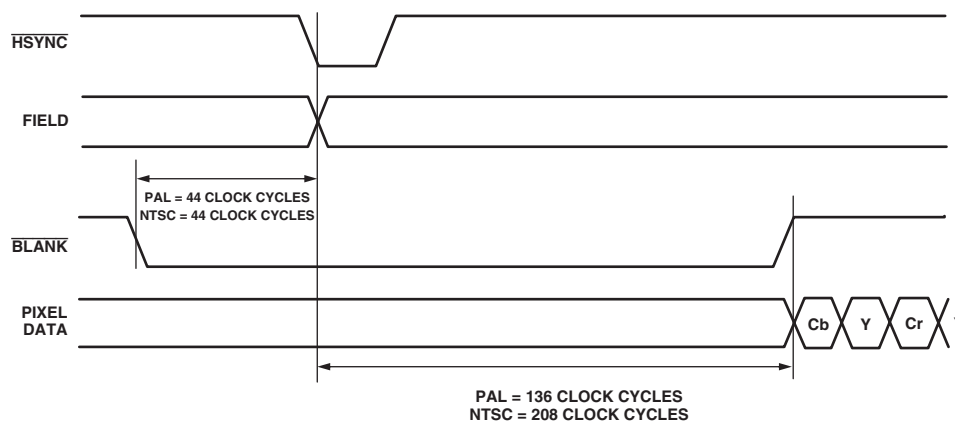


Figure 34. Active Pixel Timing

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FILTER SECTION

Table VI shows an overview of the programmable filters available on the ADV7314.

Table VI. Selectable Filters of the ADV7314

| Filter | Subaddress |
|--------------------|------------|
| SD Luma LPF NTSC | 40h |
| SD Luma LPF PAL | 40h |
| SD Luma Notch NTSC | 40h |
| SD Luma Notch PAL | 40h |
| SD Luma SSAF | 40h |
| SD Luma CIF | 40h |
| SD Luma QCIF | 40h |
| SD Chroma 0.65 MHz | 40h |
| SD Chroma 1.0 MHz | 40h |
| SD Chroma 1.3 MHz | 40h |
| SD Chroma 2.0 MHz | 40h |
| SD Chroma 3.0 MHz | 40h |
| SD Chroma CIF | 40h |
| SD Chroma QCIF | 40h |
| SD UV SSAF | 42h |
| HD Chroma Input | 13h |
| HD Sinc Filter | 13h |
| HD Chroma SSAF | 13h |

HD Sinc Filter

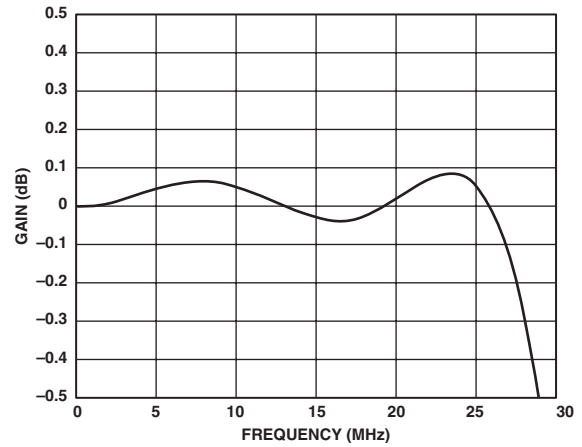


Figure 35. HD Sinc Filter Enabled

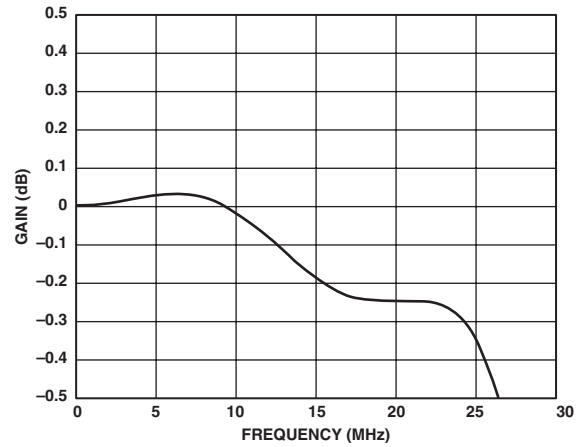


Figure 36. HD Sinc Filter Disabled

SD Internal Filter Response

[Subaddress 40h; Subaddress 42, Bit 0]

The Y filter supports several different frequency responses including two low-pass responses, two notch responses, an extended (SSAF) response, with or without gain boost/attenuation, a CIF response and a QCIF response. The UV filter supports several different frequency responses, including six low-pass responses, a CIF response and a QCIF response, as can be seen in the Typical Performance Characteristics graphs.

If SD SSAF gain is enabled, there are 12 possible responses in the range from -4 dB to +4 dB [Subaddress 47h, Bit 4]. The desired response can be chosen by the user by programming the correct value via the I²C [Subaddress 62h]. The variation of frequency responses can be seen in the Typical Performance Characteristics graphs.

Table VII. Internal Filter Specifications

| Filter | Pass-Band Ripple (dB) | 3 dB Bandwidth (MHz) |
|-----------------|-----------------------|----------------------|
| Luma LPF NTSC | 0.16 | 4.24 |
| Luma LPF PAL | 0.1 | 4.81 |
| Luma Notch NTSC | 0.09 | 2.3/4.9/6.6 |
| Luma Notch PAL | 0.1 | 3.1/5.6/6.4 |
| Luma SSAF | 0.04 | 6.45 |
| Luma CIF | 0.127 | 3.02 |
| Luma QCIF | Monotonic | 1.5 |
| Chroma 0.65 MHz | Monotonic | 0.65 |
| Chroma 1.0 MHz | Monotonic | 1 |
| Chroma 1.3 MHz | 0.09 | 1.395 |
| Chroma 2.0 MHz | 0.048 | 2.2 |
| Chroma 3.0 MHz | Monotonic | 3.2 |
| Chroma CIF | Monotonic | 0.65 |
| Chroma QCIF | Monotonic | 0.5 |

¹Pass-band ripple refers to the maximum fluctuations from the 0 dB response in the pass band, measured in dB. The pass band is defined to have 0 Hz to f_c (Hz) frequency limits for a low-pass filter, 0 Hz to f_1 (Hz) and f_2 (Hz) to infinity for a notch filter, where f_c , f_1 , f_2 are the -3 dB points.

²3 dB bandwidth refers to the -3 dB cutoff frequency.

In addition to the chroma filters listed in Table VII, the ADV7314 contains an SSAF filter specifically designed for and applicable to the color difference component outputs, U and V.

This filter has a cutoff frequency of about 2.7 MHz and -40 dB at 3.8 MHz, as can be seen in Figure 37. This filter can be controlled with Address 42h, Bit 0.

If this filter is disabled, the selectable chroma filters shown in Table VII can be used for the CVBS or Luma/Chroma signal.

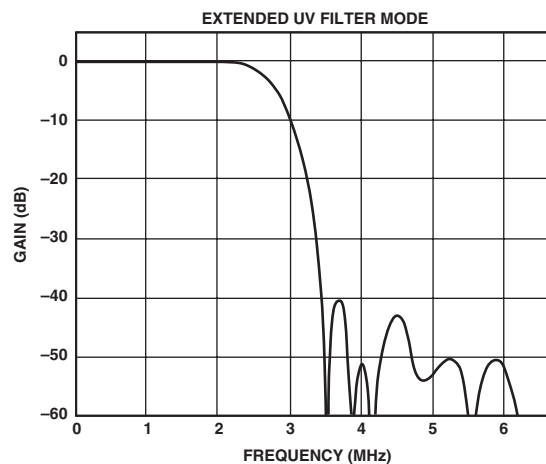
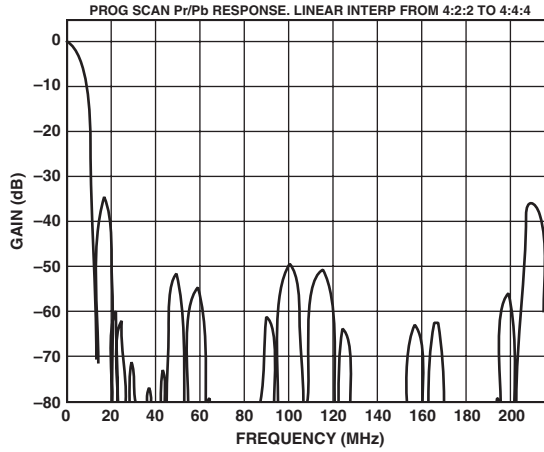
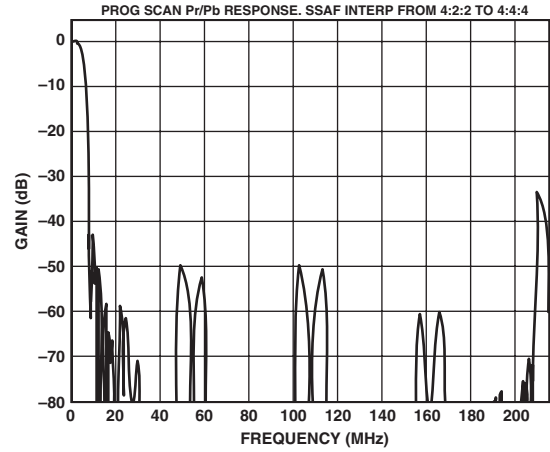


Figure 37. UV SSAF Filter

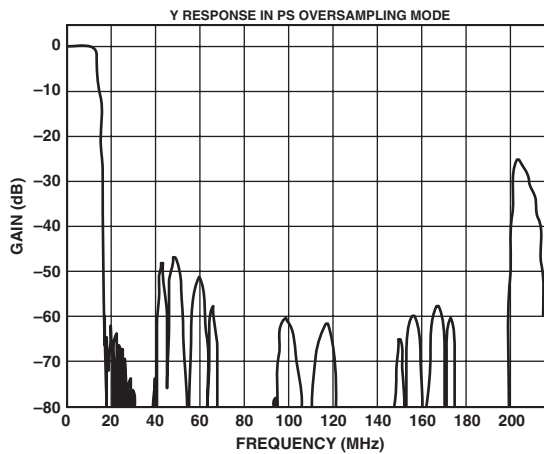
ADV7314—Typical Performance Characteristics



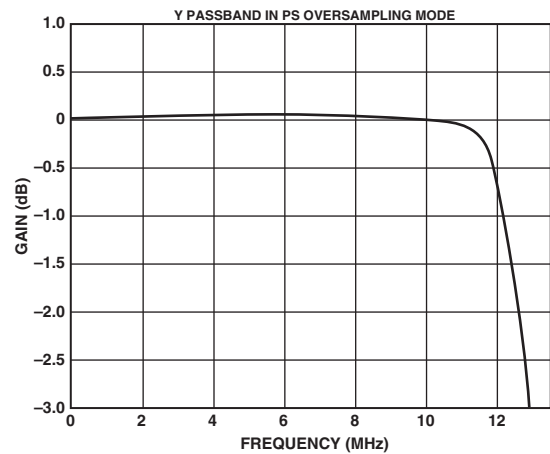
TPC 1. PS – UV 8× Oversampling Filter—Linear



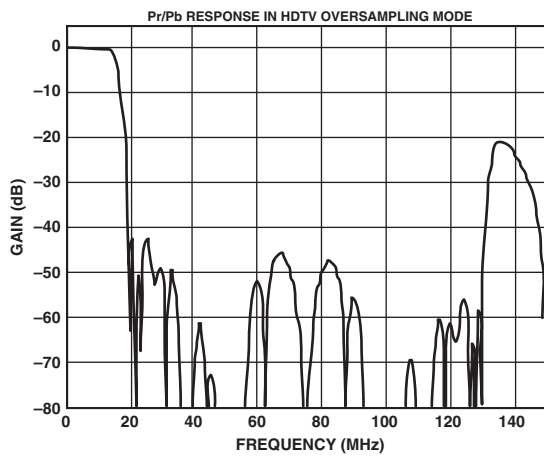
TPC 4. PS – UV 8× Oversampling Filter—SSAF



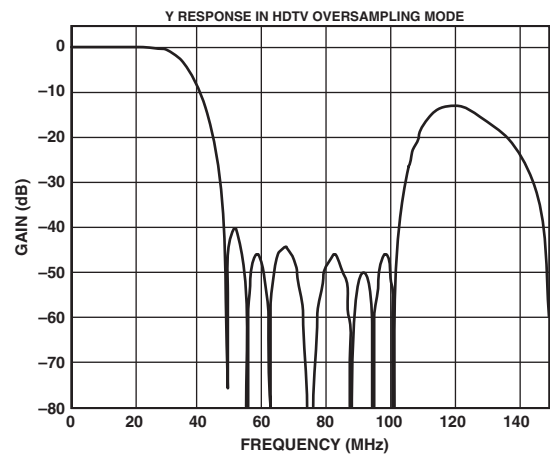
TPC 2. PS – Y 8× Oversampling Filter



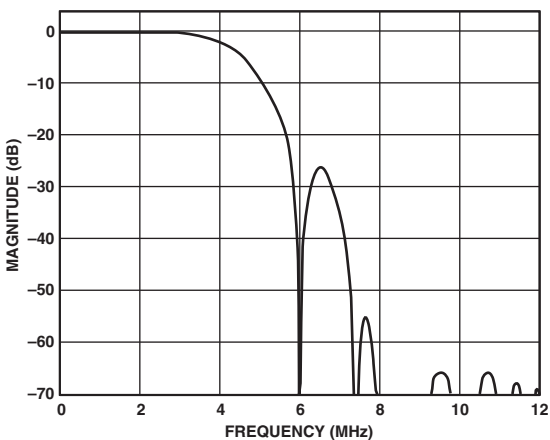
TPC 5. PS – Y 8× Oversampling Filter—Pass Band



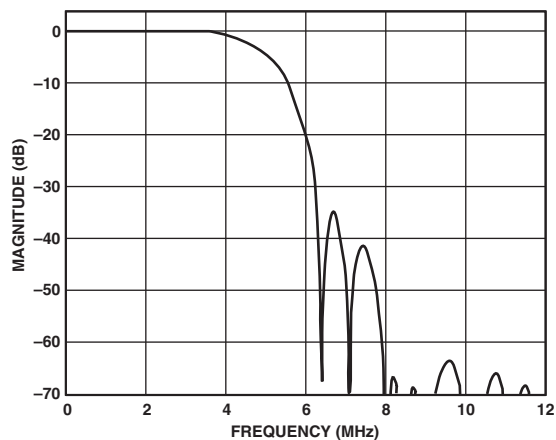
TPC 3. HDTV – UV 2× Oversampling Filter



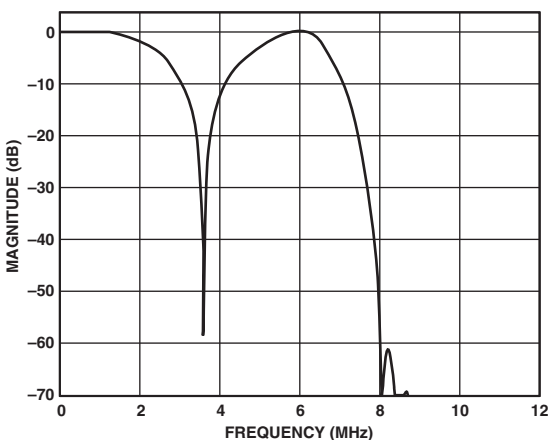
TPC 6. HDTV – Y 2× Oversampling Filter



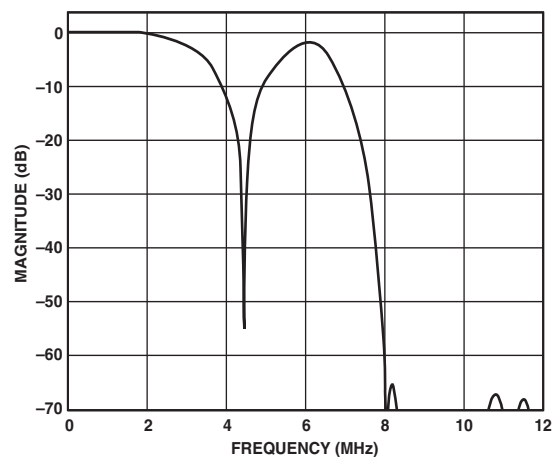
TPC 7. Luma NTSC Low-Pass Filter



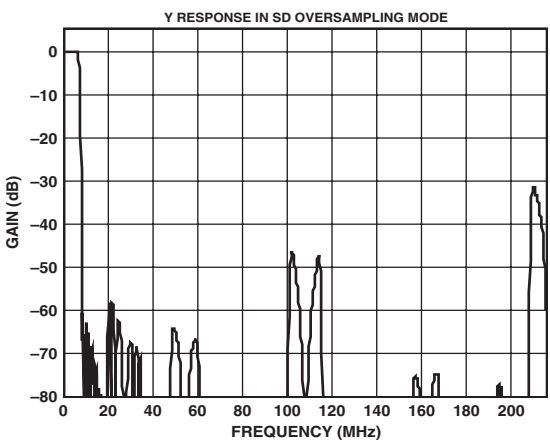
TPC 10. Luma PAL Low-Pass Filter



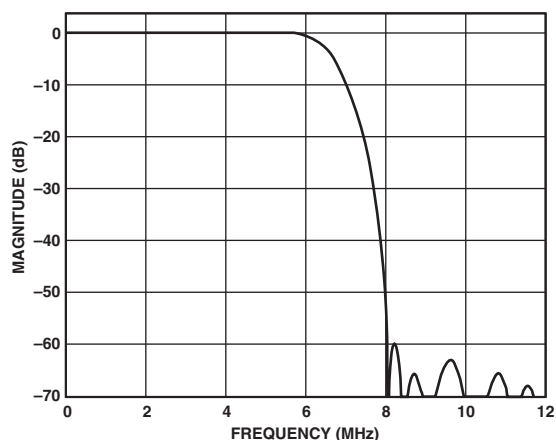
TPC 8. Luma NTSC Notch Filter



TPC 11. Luma PAL Notch Filter

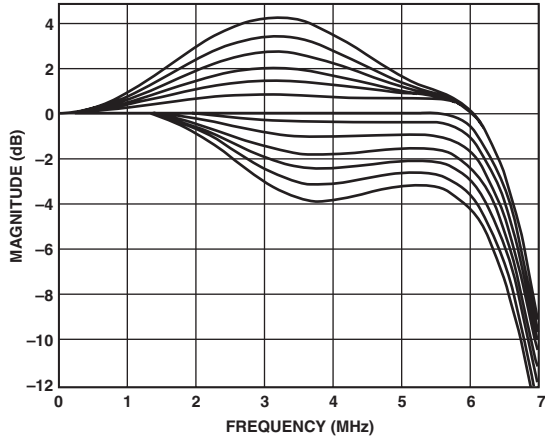


TPC 9. Y-16x Oversampling Filter

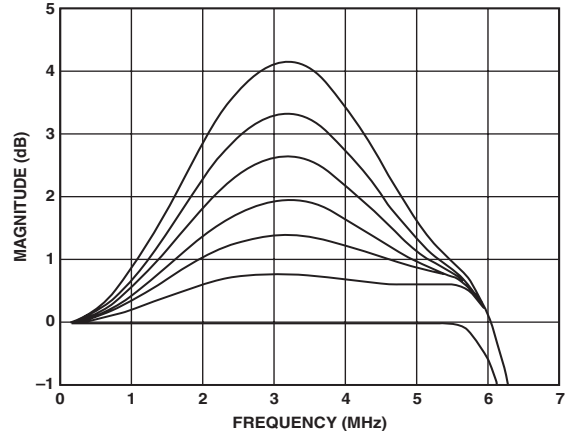


TPC 12. Luma SSAF Filter up to 12 MHz

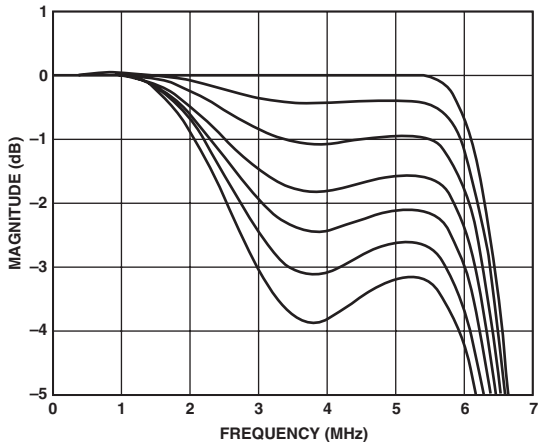
ADV7314



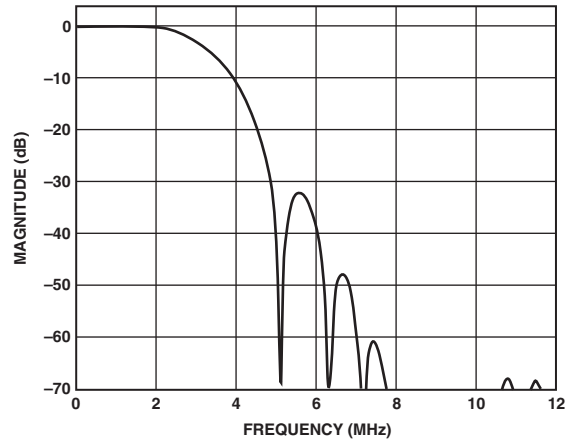
TPC 13. Luma SSAF Filter—Programmable Responses



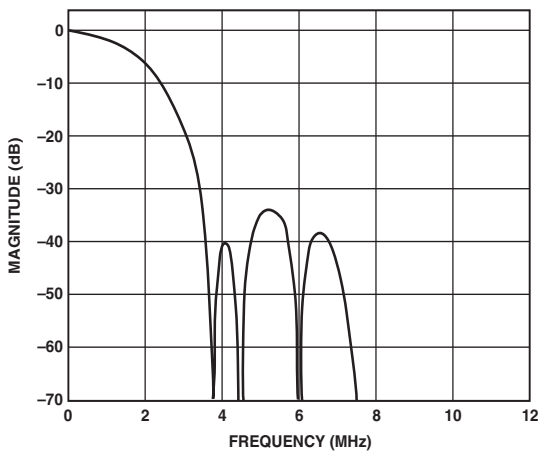
TPC 16. Luma SSAF Filter—Programmable Gain



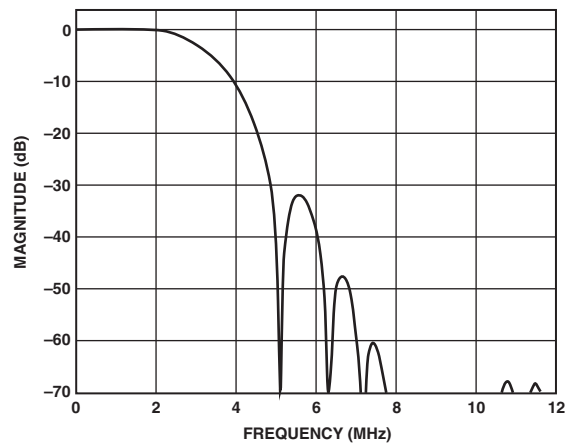
TPC 14. Luma SSAF Filter—Programmable Attenuation



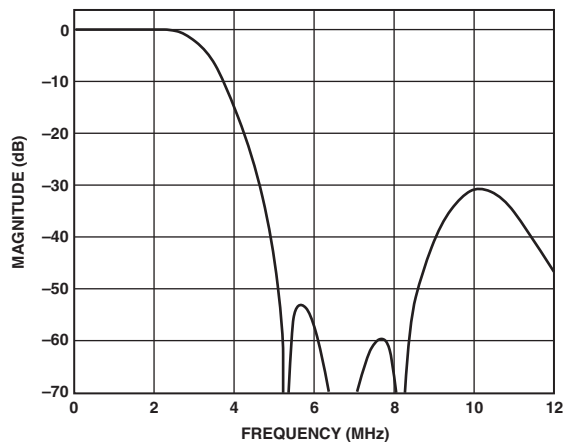
TPC 17. Luma CIF LP Filter



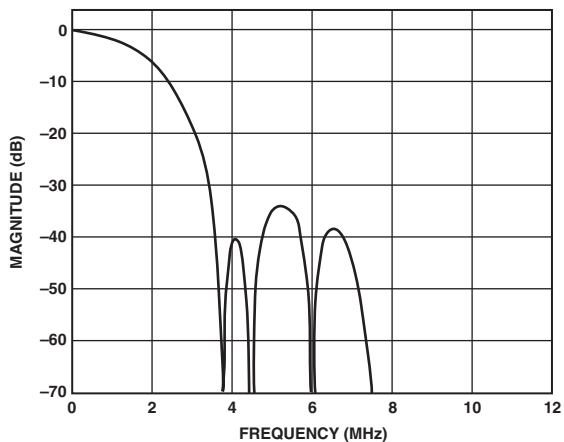
TPC 15. Luma QCIF LP Filter



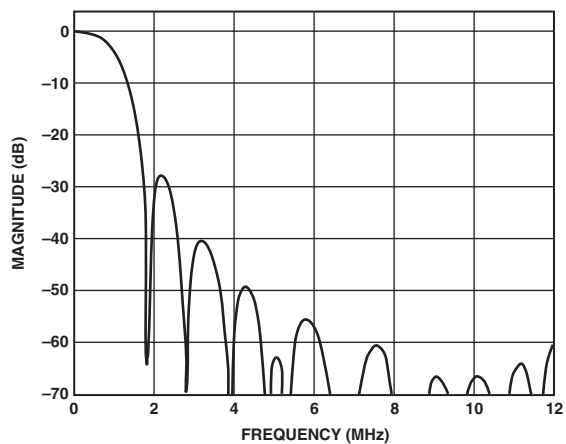
TPC 18. Chroma 3.0 MHz LP Filter



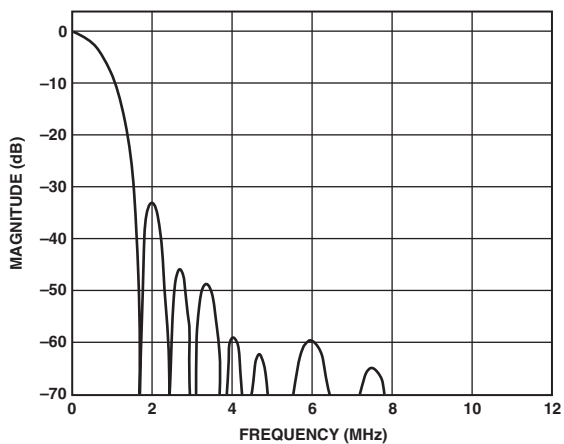
TPC 19. Chroma 2.0 MHz LP Filter



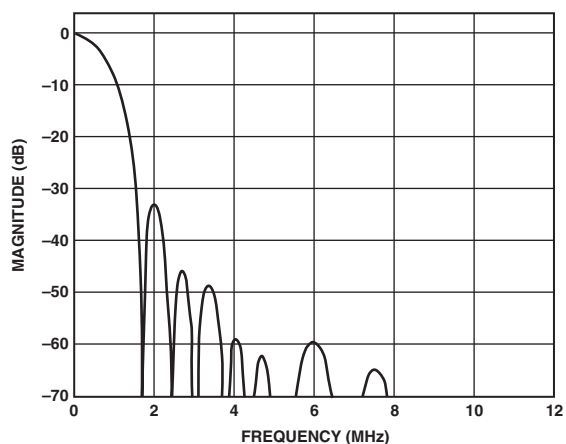
TPC 22. Chroma 1.3 MHz LP Filter



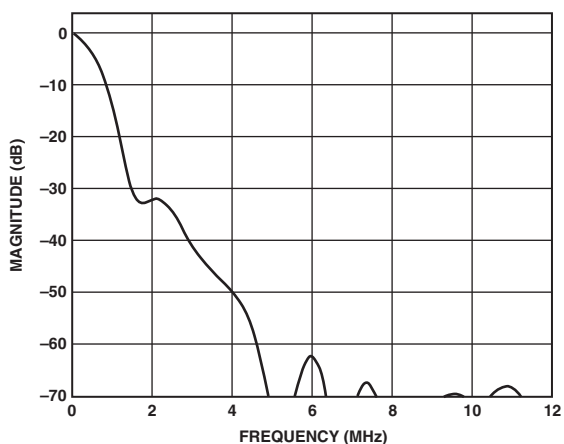
TPC 20. Chroma 1.0 MHz LP Filter



TPC 23. Chroma 0.65 MHz LP Filter



TPC 21. Chroma CIF LP Filter



TPC 24. Chroma QCIF LP Filter

ADV7314

COLOR CONTROLS AND RGB MATRIX

HD/PS Y Level, Cr Level, Cb Level

[Subaddress 16h–18h]

Three 8-bit registers at Address 16h, 17h, 18h are used to program the output color of the internal HD test pattern generator, whether it is the lines of the cross hatch pattern or the uniform field test pattern. They are not functional as color controls on external pixel data input. For this purpose, the RGB matrix is used.

The standard used for the values for Y and the color difference signals to obtain white, black, and the saturated primary and complementary colors conforms to the ITU-R BT.601–4 standard.

Table VIII shows sample color values to be programmed into the color registers when Output Standard Selection is set to EIA 770.2.

Table VIII. Sample Color Values for EIA770.2 Output Standard Selection

| Sample Color | Color Y Value | Color CR Value | Color CB Value |
|--------------|---------------|----------------|----------------|
| White | 235 (EB) | 128 (80) | 128 (80) |
| Black | 16 (10) | 128(80) | 128 (80) |
| Red | 81 (51) | 240 (F0) | 90 (5A) |
| Green | 145 (91) | 34 (22) | 54 (36) |
| Blue | 41 (29) | 110 (6E) | 240 (F0) |
| Yellow | 210 (D2) | 146 (92) | 16 (10) |
| Cyan | 170 (AA) | 16 (10) | 166 (A6) |
| Magenta | 106 (6A) | 222 (DE) | 202 (CA) |

HD RGB Matrix

[Subaddress 03h–09h]

When the programmable RGB matrix is disabled [Address 02h, Bit 3], the internal RGB matrix takes care of all YCrCb to YUV or RGB scaling according to the input standard programmed into the device.

When the programmable RGB matrix is enabled, the color components are converted according to the 1080i standard [SMPTE 274M]:

$$Y' = 0.2126R' + 0.7152 G' + 0.0722 B'$$

$$CR' = [0.5 / (1 - 0.0722)] (B' - Y')$$

$$CB' = [0.5 / (1 - 0.2126)] (R' - Y')$$

This is reflected in the preprogrammed values for GY = 138Bh, GU = 93h, GV = 3B, BU = 248h, RV = 1F0.

If another input standard is used, the scale values for GY, GU, GV, BU, and RV have to be adjusted according to this input standard. The user must consider that the color component conversion might use different scale values. For example, SMPTE 293M uses the following conversion:

$$Y' = 0.299 R' + 0.587 G' + 0.114 B'$$

$$CB' = [0.5 / (1 - 0.114)] (B' - Y')$$

$$CR' = [0.5 / (1 - 0.299)] (R' - Y')$$

The programmable RGB matrix can be used to control the HD output levels in cases where the video output does not conform to standard due to altering the DAC output stages such as termination resistors. The programmable RGB matrix is used for external HD data and is not functional when the HD test pattern is enabled.

Programming the RGB Matrix

The RGB matrix should be enabled [Address 02h, Bit 3], the output should be set to RGB [Address 02h, Bit 5], sync on PrPb should be disabled [Address 15h, Bit 2], sync on RGB is optional [Address 02h, Bit 4].

GY at Addresses 03h and 05h control the output levels on the green signal, BU at 04h and 08h control the blue signal output levels, and RV at 04h and 09h control the red output levels. To control YPrPb output levels, YUV output should be enabled [Address 02h, Bit 5]. In this case GY [Address 05h; Address 03, Bit 0–1] is used for the Y output, RV [Address 09; Address 04, Bit 0–1] is used for the Pr output and BU [Address 08h; Address 04h, Bit 2–3] is used for the Pb output.

If RGB output is selected the RGB matrix scaler uses the following equations:

$$G = GY \times Y + GU \times Pb + GV \times Pr$$

$$B = GY \times Y + BU \times Pb$$

$$R = GY \times Y + RV \times Pr$$

If YUV output is selected the following equations are used:

$$Y = GY \times Y$$

$$U = BU \times Pb$$

$$V = RV \times Pr$$

On power-up, the RGB matrix is programmed with default values:

Table IX. RGB Matrix Default Values

| Address | Default |
|---------|---------|
| 03h | 03h |
| 04h | F0h |
| 05h | 4Eh |
| 06h | 0Eh |
| 07h | 24h |
| 08h | 92h |
| 09h | 7Ch |

When the programmable RGB matrix is not enabled, the ADV7314 automatically scales YCrCb inputs to all standards supported by this part.

SD Luma and Color Control

[Subaddresses 5Ch, 5Dh, 5Eh, 5Fh]

SD Y scale, SD Cr scale, and SD Cb scale are 10-bit control registers to scale the Y, U, and V output levels.

Each of these registers represents the value required to scale the U or V level from 0.0 to 2.0 and Y level from 0.0 to 1.5 of its initial level. The value of these 10 bits is calculated using the following equation:

$$Y, U, \text{ or } V \text{ Scalar Value} = \text{Scale Factor} \times 512$$

For example:

Scale Factor = 1.18

$$Y, U, \text{ or } V \text{ Scale Value} = 1.18 \times 512 = 665.6$$

$$Y, U, \text{ or } V \text{ Scale Value} = 665 \text{ (rounded to the nearest integer)}$$

$$Y, U, \text{ or } V \text{ Scale Value} = 1010 \ 0110 \ 01b$$

Address 5Ch, SD LSB Register = 15h

Address 5Dh, SD Y Scale Register = A6h

Address 5Eh, SD V Scale Register = A6h

Address 5Fh, SD U Scale Register = A6h

SD Hue Adjust Value

[Subaddress 60h]

The hue adjust value is used to adjust the hue on the composite and chroma outputs.

These eight bits represent the value required to vary the hue of the video data, i.e., the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7314 provides a range of $\pm 22.5^\circ$ increments of 0.17578125° . For normal operation (zero adjustment), this register is set to 80h. FFh and 00h represent the upper and lower limit (respectively) of adjustment attainable.

(Hue Adjust) [°] = $0.17578125^\circ \times (\text{HCRd} - 128)$, for positive hue adjust value.

$$\left(\frac{4}{0.17578125} \right) + 128 = 151d^* = 97h$$

*Rounded to the nearest integer.

To adjust the hue by -4° , write 69h to the hue adjust value register:

$$\left(\frac{-4}{0.17578125} \right) + 128 = 105d^* = 69h$$

*Rounded to the nearest integer.

SD Brightness Control

[Subaddress 61h]

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the scaled Y data. For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and PAL, the setup can vary from -7.5 IRE to $+15$ IRE.

The brightness control register is an 8-bit register. Seven bits of this 8-bit register are used to control the brightness level. This brightness level can be a positive or negative value. For example:

Standard: NTSC with pedestal.

To add $+20$ IRE brightness level, write 28h to Address 61h, SD brightness.

$$\begin{aligned} [\text{SD Brightness Value}] H &= \\ [\text{IRE Value} \times 2.015631] H &= \\ [20 \times 2.015631] H &= [40.31262] H = 28H \end{aligned}$$

Standard: PAL.

To add -7 IRE brightness level, write 72h to Address 61h, SD brightness.

$$\begin{aligned} [|\text{IRE Value}| \times 2.015631] &= \\ [7 \times 2.015631] &= [14.109417] = 0001110b \\ [0001110] \text{into twos complement} &= [1110010] B = 72h \end{aligned}$$

Table X. Brightness Control Values*

| Setup Level In NTSC with Pedestal | Setup Level In NTSC No Pedestal | Setup Level In PAL | SD Brightness |
|-----------------------------------|---------------------------------|--------------------|---------------|
| 22.5 IRE | 15 IRE | 15 IRE | 1Eh |
| 15 IRE | 7.5 IRE | 7.5 IRE | 0Fh |
| 7.5 IRE | 0 IRE | 0 IRE | 00h |
| 0 IRE | -7.5 IRE | -7.5 IRE | 71h |

*Values in the range from 3Fh to 44h might result in an invalid output signal.

SD Brightness Detect

[Subaddress 7Ah]

The ADV7314 allows monitoring of the brightness level of the incoming video data. Brightness detect is a read-only register.

Double Buffering

[Subaddress 13h, Bit 7; Subaddress 48h, Bit 2]

Double buffered registers are updated once per field on the falling edge of the VSYNC signal. Double buffering improves the overall performance since modifications to register settings will not be made during active video, but take effect on the start of the active video.

Double buffering can be activated on the following HD registers: HD Gamma A and Gamma B curves and HD CGMS registers. Double buffering can be activated on the following SD registers: SD Gamma A and Gamma B curves, SD Y scale, SD U scale, SD V scale, SD brightness, SD closed captioning, and SD Macrovision Bits 5-0.

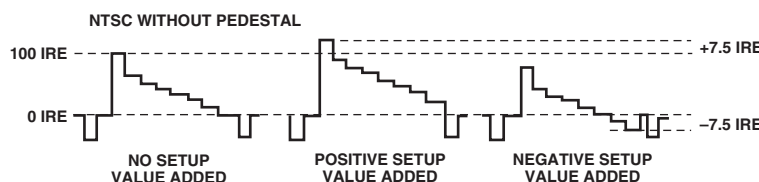


Figure 38. Examples for Brightness Control Values

ADV7314

PROGRAMMABLE DAC GAIN CONTROL

DACs A, B, and C are controlled by Register 0A.

DACs D, E, and F are controlled by Register 0B.

The I²C control registers will adjust the output signal gain up or down from its absolute level.

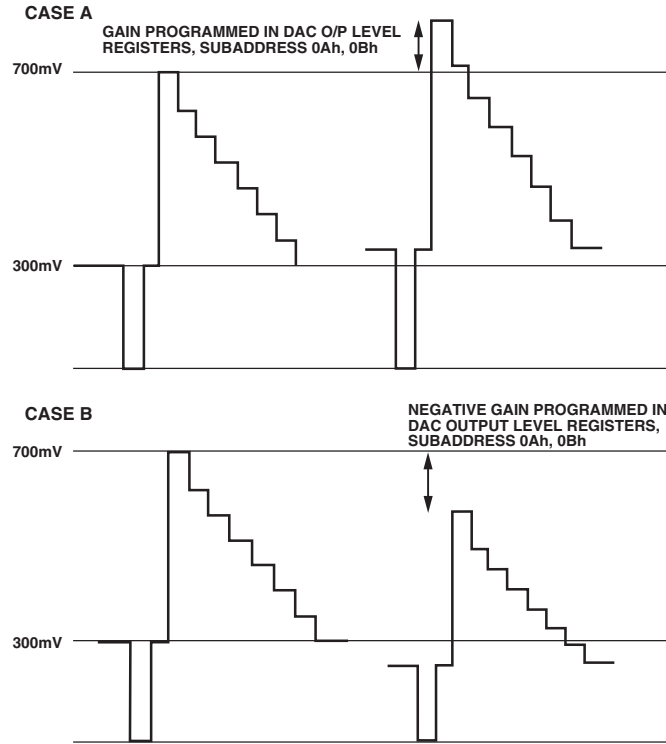


Figure 39. Programmable DAC Gain—Positive and Negative Gain

In case A, the video output signal is gained. The absolute level of the sync tip and blanking level both increase with respect to the reference video output signal. The overall gain of the signal is increased from the reference signal.

In case B, the video output signal is reduced. The absolute level of the sync tip and blanking level both decrease with respect to the reference video output signal. The overall gain of the signal is reduced from the reference signal.

The range of this feature is specified for $\pm 7.5\%$ of the nominal output from the DACs. For example, if the output current of the DAC is 4.33 mA, the DAC tune feature can change this output current from 4.008 mA (-7.5%) to 4.658 mA ($+7.5\%$).

The reset value of the vid_out_ctrl registers is 00h \rightarrow nominal DAC output current. Table XI is an example of how the output current of the DACs varies for a nominal 4.33 mA output current.

Table XI.

| Register 0Ah or 0Bh | DAC Current (mA) | % Gain |
|---------------------|------------------|---|
| 0100 0000 (40h) | 4.658 | 7.5000 |
| 0011 1111 (3Fh) | 4.653 | 7.3820 |
| 0011 1110 (3Eh) | 4.648 | 7.3640 |
| ... | ... | ... |
| ... | ... | ... |
| 0000 0010 (02h) | 4.43 | 0.0360 |
| 0000 0001 (01h) | 4.38 | 0.0180 |
| 0000 0000 (00h) | 4.33 | 0.0000 |
| | | (I ² C Reset Value, Nominal) |
| 1111 1111 (FFh) | 4.25 | -0.0180 |
| 1111 1110 (FEh) | 4.23 | -0.0360 |
| ... | ... | ... |
| ... | ... | ... |
| 1100 0010 (C2h) | 4.018 | -7.3640 |
| 1100 0001 (C1h) | 4.013 | -7.3820 |
| 1100 0000 (C0h) | 4.008 | -7.5000 |

Gamma Correction
[Subaddress 24h–37h for HD, Subaddress 66h–79h for SD]

Gamma correction is available for SD and HD video. For each standard there are 20 8-bit registers. They are used to program the gamma correction curves A and B. HD gamma curve A is programmed at Addresses 24h–2Dh, HD gamma curve B at 2Eh–37h. SD gamma curve A is programmed at addresses 66h–6Fh, and SD gamma curve B at Addresses 70h–79h.

Generally, gamma correction is applied to compensate for the nonlinear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function

$$Signal_{OUT} = (Signal_{IN})^\gamma$$

where γ = gamma power factor.

Gamma correction is performed on the luma data only. The user has the choice to use two different curves, curve A or curve B. At any time, only one of these curves can be used.

The response of the curve is programmed at 10 predefined locations. In changing the values at these locations, the gamma curve can be modified. Between these points linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the 10 locations are at 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. Location 0, 16, 240, and 255 are fixed and cannot be changed.

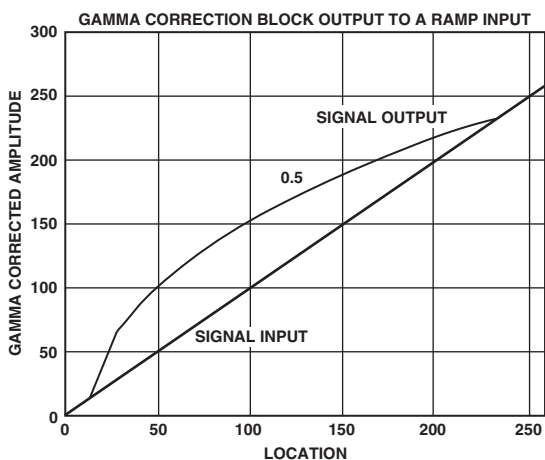


Figure 40. Signal Input (Ramp) and Signal Output for Gamma 0.5

For the length of 16 to 240, the gamma correction curve has to be calculated as follows:

$$y = x^\gamma$$

where:

y = gamma corrected output.

x = linear input signal.

γ = gamma power factor.

To program the gamma correction registers, the seven values for y have to be calculated using the following formula:

$$y_n = \left[\frac{x_{(n-16)}}{(240-16)} \right]^\gamma \times (240-16) + 16$$

where:

$x_{(n-16)}$ = value for x along x -axis at points.

$n = 24, 32, 48, 64, 80, 96, 128, 160, 192, \text{ or } 224.$

y_n = value for y along the y -axis, which has to be written into the gamma correction register.

For example:

- $y_{24} = [(8 / 224)^{0.5} \times 224] + 16 = 58^*$
- $y_{32} = [(16 / 224)^{0.5} \times 224] + 16 = 76^*$
- $y_{48} = [(32 / 224)^{0.5} \times 224] + 16 = 101^*$
- $y_{64} = [(48 / 224)^{0.5} \times 224] + 16 = 120^*$
- $y_{80} = [(64 / 224)^{0.5} \times 224] + 16 = 136^*$
- $y_{96} = [(80 / 224)^{0.5} \times 224] + 16 = 150^*$
- $y_{128} = [(112 / 224)^{0.5} \times 224] + 16 = 174^*$
- $y_{160} = [(144 / 224)^{0.5} \times 224] + 16 = 195^*$
- $y_{192} = [(176 / 224)^{0.5} \times 224] + 16 = 214^*$
- $y_{224} = [(208 / 224)^{0.5} \times 224] + 16 = 232^*$

*rounded to the nearest integer

The gamma curves in Figure 41 are examples only; any user defined curve is acceptable in the range of 16 to 240.

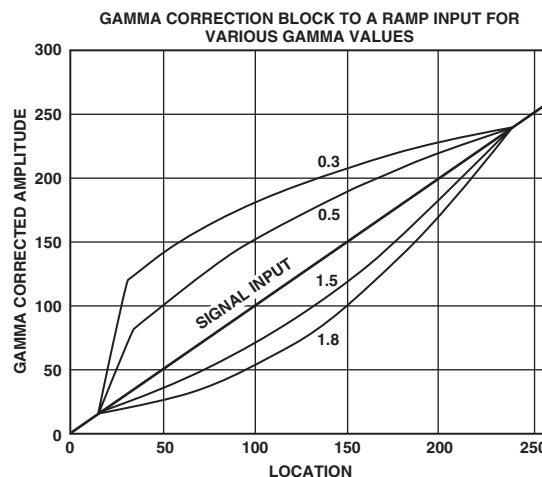


Figure 41. Signal Input (Ramp) and Selectable Gamma Output Curves

ADV7314

HD Sharpness Filter Control and Adaptive Filter Control [Subaddress 20h, 38h–3Dh]

There are three Filter modes available on the ADV7314: sharpness filter mode and two adaptive filter modes.

HD Sharpness Filter Mode

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 42, the following register settings must be used: HD sharpness filter must be enabled and HD adaptive filter enable must be disabled.

To select one of the 256 individual responses, the according gain values for each filter, which range from -8 to $+7$, must be programmed into the HD sharpness filter gain register at Address 20h.

HD Adaptive Filter Mode

The HD adaptive filter threshold A, B, C registers, the HD adaptive filter gain 1, 2, 3 registers, and the HD sharpness filter gain register are used in adaptive filter mode. To activate the adaptive filter control, HD sharpness filter must be enabled and HD adaptive filter gain must be enabled.

The derivative of the incoming signal is compared to the three programmable threshold values: HD adaptive filter threshold A, B, C. The recommended threshold range is from 16 to 235 although any value in the range of 0 to 255 can be used.

The edges can then be attenuated with the settings in HD adaptive filter gain 1, 2, 3 registers and HD sharpness filter gain register. According to the settings of the HD adaptive filter mode control, there are two adaptive filter modes available:

1. Mode A is used when adaptive filter mode is set to 0. In this case, Filter B (LPF) will be used in the adaptive filter block. Also, only the programmed values for Gain B in the HD sharpness filter gain, HD adaptive filter gain 1, 2, 3 are applied when needed. The Gain A values are fixed and cannot be changed.
2. Mode B is used when adaptive filter gain is set to 1. In this mode, a cascade of Filter A and Filter B is used. Both settings for Gain A and Gain B in the HD sharpness filter gain, HD adaptive filter gain 1, 2, 3 become active when needed.

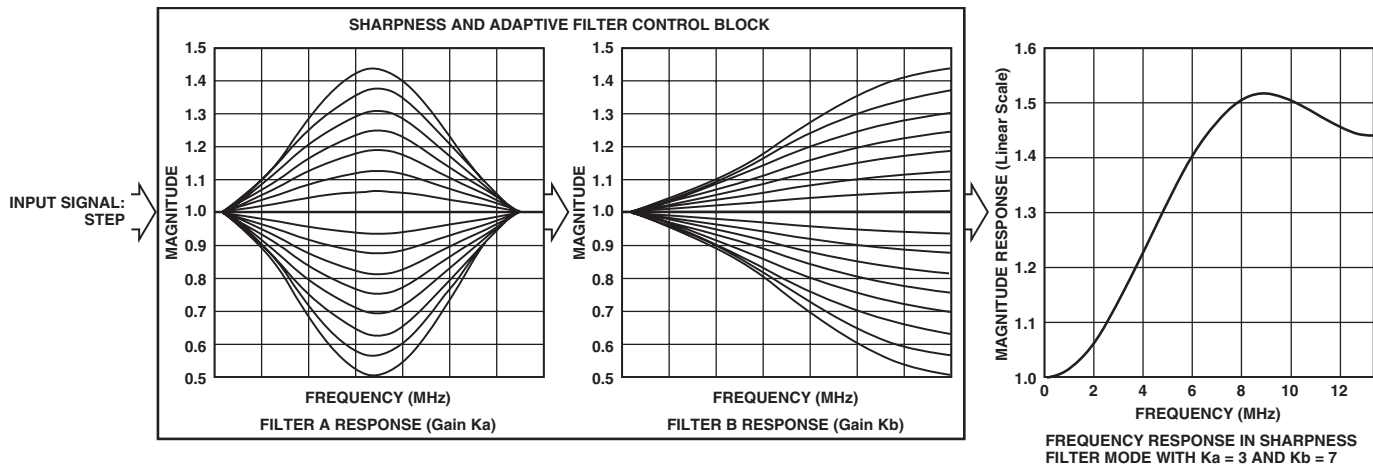


Figure 42. Sharpness and Adaptive Filter Control Block Frequency Response in Sharpness Filter Mode with $K_a = +3$ and $K_b = +7$

HD Sharpness Filter and Adaptive Filter Application Examples

HD Sharpness Filter Application

The HD sharpness filter can be used to enhance or attenuate the Y video output signal. The following register settings were used to achieve the results shown in the figures below. Input data was generated by an external signal source.

Table XII.

| Address | Register Setting | Reference in Figure 43 |
|---------|------------------|------------------------|
| 00h | FCh | |
| 01h | 10h | |
| 02h | 20h | |
| 10h | 00h | |
| 11h | 81h | |
| 20h | 00h | a |
| 20h | 08h | b |
| 20h | 04h | c |
| 20h | 40h | d |
| 20h | 80h | e |
| 20h | 22h | f |

The effect of the sharpness filter can also be seen when using the internally generated cross hatch pattern.

Table XIII.

| Address | Register Setting |
|---------|------------------|
| 00h | FCh |
| 01h | 10h |
| 02h | 20h |
| 10h | 00h |
| 11h | 85h |
| 20h | 99h |

In toggling the sharpness filter enable bit [Address 11h, Bit 7], it can be seen that the line contours of the cross hatch pattern change their sharpness.

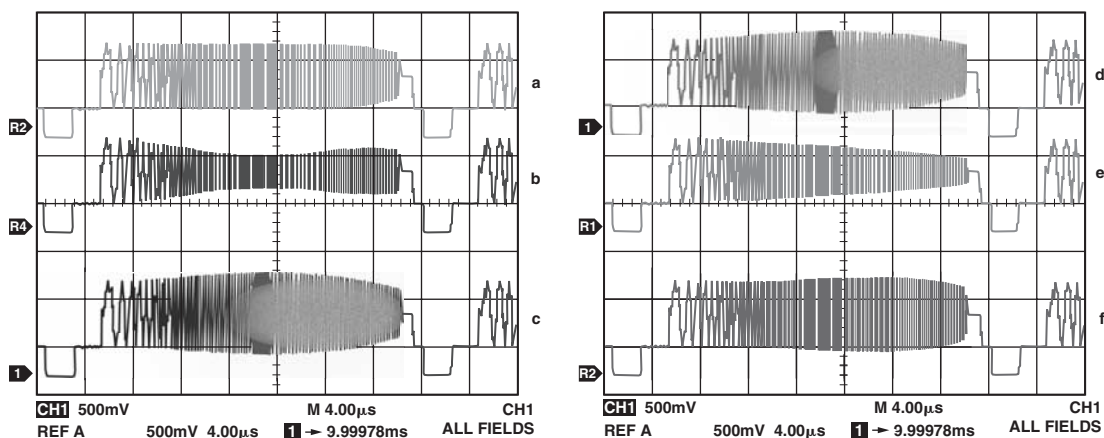


Figure 43. HD Sharpness Filter Control with Different Gain Settings for HS Sharpness Filter Gain Value

ADV7314

Adaptive Filter Control Application

Figures 44 and 45 show a typical signal to be processed by the adaptive filter control block.

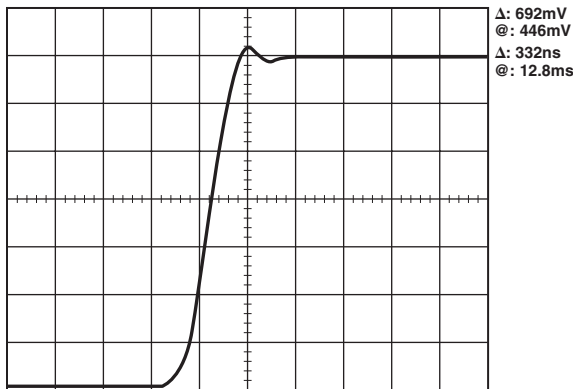


Figure 44. Input Signal to Adaptive Filter Control

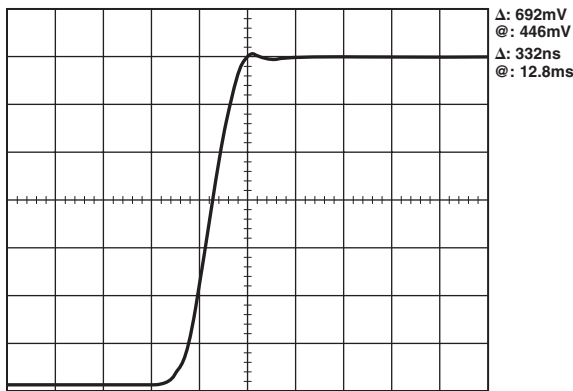


Figure 45. Output Signal after Adaptive Filter Control

The following register settings were used to obtain the results shown in Figure 45, i.e., to remove the ringing on the Y signal. Input data was generated by an external signal source.

Table XIV.

| Address | Register Setting |
|---------|------------------|
| 00h | FCh |
| 01h | 38h |
| 02h | 20h |
| 10h | 00h |
| 11h | 81h |
| 15h | 80h |
| 20h | 00h |
| 38h | ACCh |
| 39h | 9Ah |
| 3Ah | 88h |
| 3Bh | 28h |
| 3Ch | 3Fh |
| 3Dh | 64h |

*All other registers at normal settings.

When changing the adaptive filter mode to Mode B, [Address 15h, Bit 6], the following output can be obtained:

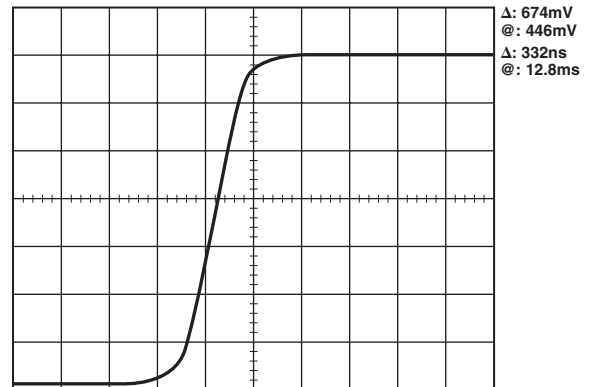


Figure 46. Output Signal from Adaptive Filter Control

The adaptive filter control can also be demonstrated using the internally generated cross hatch test pattern and toggling the adaptive filter control bit [Address 15h, Bit 7].

Table XV.

| Address | Register Setting |
|---------|------------------|
| 00h | FCh |
| 01h | 38h |
| 02h | 20h |
| 10h | 00h |
| 11h | 85h |
| 15h | 80h |
| 20h | 00h |
| 38h | ACCh |
| 39h | 9Ah |
| 3Ah | 88h |
| 3Bh | 28h |
| 3Ch | 3Fh |
| 3Dh | 64h |

SD DIGITAL NOISE REDUCTION

[Subaddress 63h, 64h, 65h]

DNR is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal [DNR input select]. The absolute value of the filter output is compared to a programmable threshold value [DNR threshold control]. There are two DNR modes available: DNR mode and DNR sharpness mode.

In DNR mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount [coring gain border, coring gain data] of this noise signal will be subtracted from the original signal.

In DNR sharpness mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise, as before. Otherwise, if the level exceeds the threshold, now being identified as a valid signal, a fraction of the signal [coring gain border, coring gain data] will be added to the original signal in order to boost high frequency components and to sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 pixels × 8 pixels for MPEG2 systems, or 16 pixels × 16 pixels for MPEG1 systems [block size control]. DNR can be applied to the resulting block transition areas that are known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels [border area].

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the [DNR block offset].

The digital noise reduction registers are three 8-bit registers. They are used to control the DNR processing.

Coring Gain Border [Address 63h, Bits 3-0]

These four bits are assigned to the gain factor applied to border areas.

In DNR mode, the range of gain values is 0-1, in increments of 1/8. This factor is applied to the DNR filter output, which lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode the range of gain values is 0-0.5, in increments of 1/16. This factor is applied to the DNR filter output which lies above the threshold range. The result is added to the original signal.

Coring Gain Data [Address 63h, Bits 7-4]

These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block.

In DNR mode the range of gain values is 0-1, in increments of 1/8. This factor is applied to the DNR filter output, which lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0-0.5, in increments of 1/16. This factor is applied to the DNR filter output, which lies above the threshold range. The result is added to the original signal.

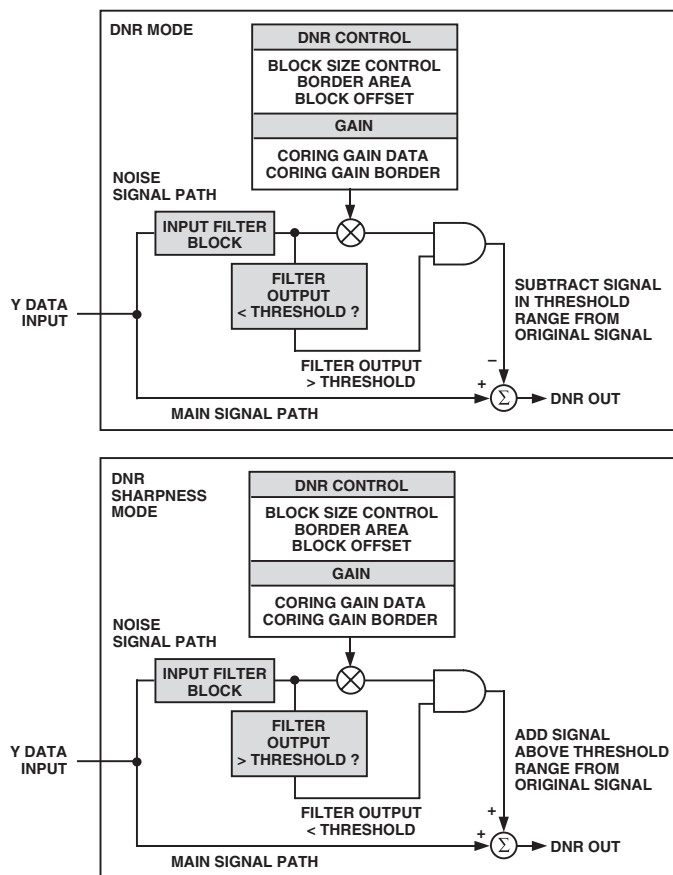


Figure 47. DNR Block Diagram

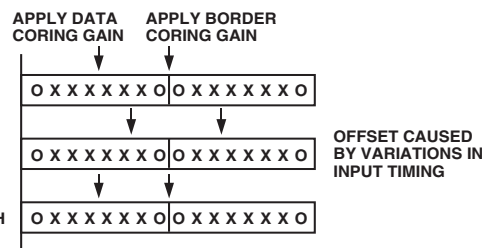


Figure 48. DNR Block Offset Control

DNR Threshold [Address 64h, Bits 5-0]

These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

Border Area [Address 64h, Bit 6]

In setting this bit to a Logic 1, the block transition area can be defined to consist of four pixels. If this bit is set to a Logic 0, the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

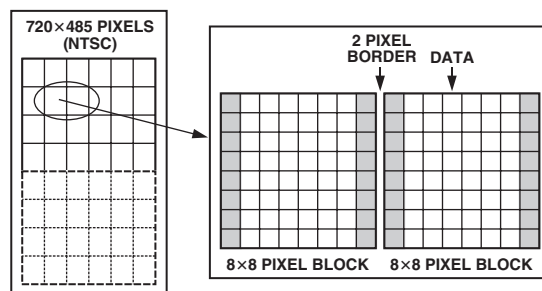


Figure 49. DNR Border Area

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Block Size Control [Address 64h, Bit 7]

This bit is used to select the size of the data blocks to be processed. Setting the block size control function to a Logic 1 defines a 16 pixel × 16 pixel data block; a Logic 0 defines an 8 pixel × 8 pixel data block, where one pixel refers to two clock cycles at 27 MHz.

DNR Input Select Control [Address 65h, Bit 2–0]

Three bits are assigned to select the filter that is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is the signal that will be DNR processed. Figure 50 shows the filter responses selectable with this control.

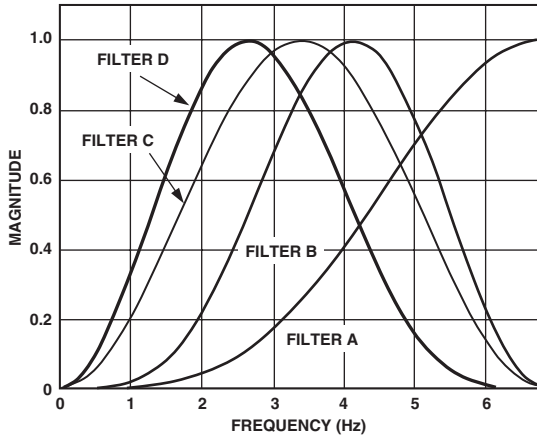


Figure 50. DNR Input Select

DNR Mode Control [Address 65h, Bit 4]

This bit controls the DNR mode selected. A Logic 0 selects DNR mode; a Logic 1 selects DNR sharpness mode.

DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR sharpness mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal, since this data is assumed to be valid data and not noise. The overall effect is that the signal will be boosted (similar to using extended SSAF filter).

Block Offset Control [Address 65h, Bits 7–4]

Four bits are assigned to this control, which allows a shift of the data block of 15 pixels maximum. Consider the coring gain positions fixed. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

SD ACTIVE VIDEO EDGE

[Subaddress 42h, Bit 7]

When the active video edge is enabled, the first three pixels and the last three pixels of the active video on the luma channel are scaled in such a way that maximum transitions on these pixels are not possible. The scaling factors are $\times 1/8$, $\times 1/2$, $\times 7/8$. All other active video passes through unprocessed.

SAV/EAV Step Edge Control

The ADV7314 can control fast rising and falling signals at the start and end of active video to minimize ringing.

An algorithm monitors SAV and EAV and governs when the edges are too fast. The result will be reduced ringing at the start and end of active video for fast transitions.

Subaddress 42h, Bit 7 = 1 enables this feature.

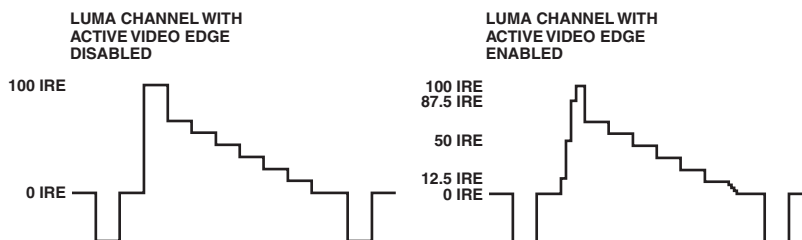


Figure 51. Example for Active Video Edge Functionality

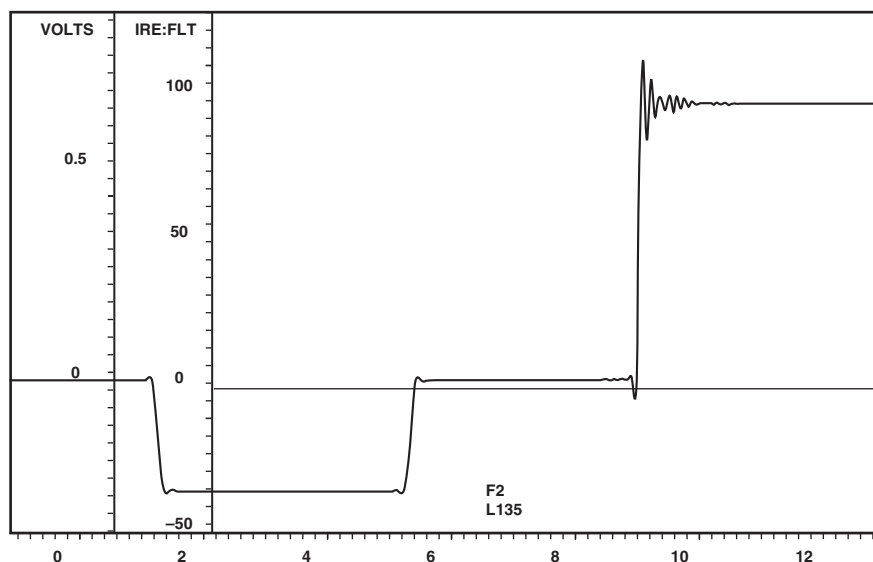


Figure 52. Address 42h, Bit 7 = 0

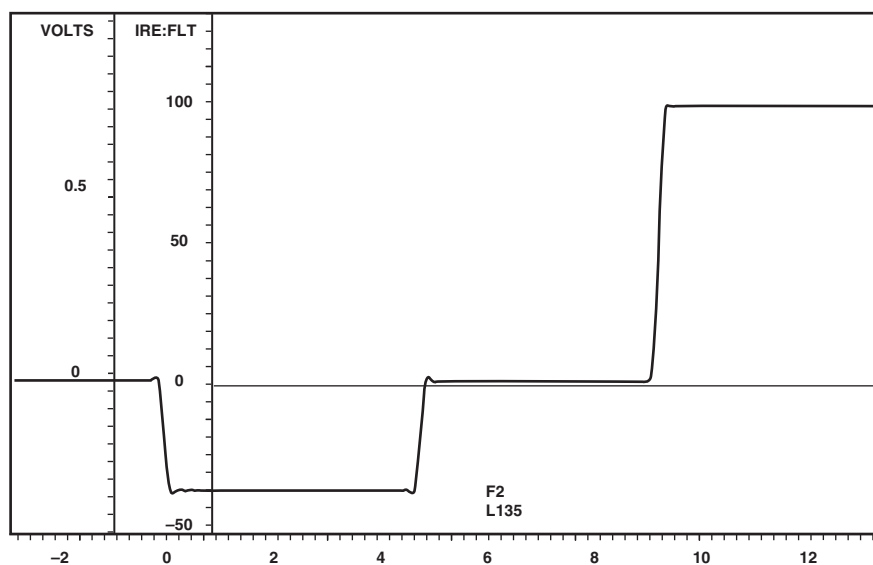


Figure 53. Address 42h, Bit 7 = 1

ADV7314

BOARD DESIGN AND LAYOUT CONSIDERATIONS

DAC Termination and Layout Considerations

The ADV7314 contains an on-board voltage reference. The ADV7314 can be used with an external V_{REF} (AD1580).

The R_{SET} resistors are connected between the R_{SET} pins and AGND and are used to control the full-scale output current and therefore the DAC voltage output levels. For full-scale output, R_{SET} must have a value of 3040 Ω . The R_{SET} values should not be changed. R_{LOAD} has a value of 150 Ω with a 4 \times gain stage for full-scale output.

Video Output Buffer and Optional Output Filter

Output buffering on all six DACs is necessary in order to drive output devices, such as SD or HD monitors. Analog Devices produces a range of suitable op amps for this application, for example the AD8061. More information on line driver buffering circuits is given in the relevant op amp data sheets.

An optional analog reconstruction low-pass filter (LPF) may be required as an anti-imaging filter if the ADV7314 is connected to a device that requires this filtering. The filter specifications vary with the application.

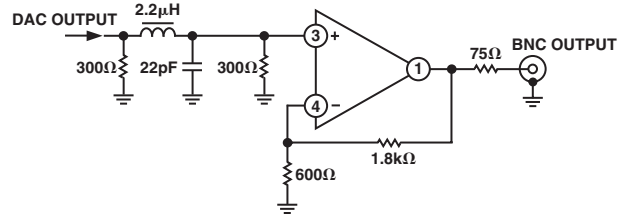


Figure 54. Example for Output Filter for SD, 16 \times Oversampling

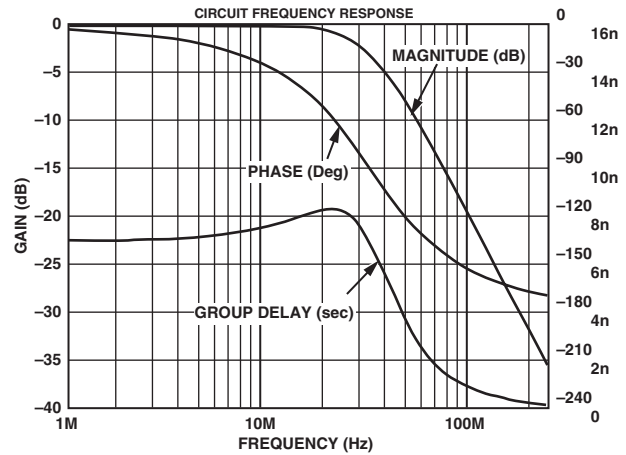


Figure 55. Filter Plot for Output Filter for SD, 16 \times Oversampling

Table XVI. External Filter Requirements

| Application | Oversampling | Cutoff Frequency (MHz) | Attenuation -50 dB @ (MHz) |
|-------------|--------------|------------------------|----------------------------|
| SD | 2 \times | >6.5 | 20.5 |
| SD | 16 \times | >6.5 | 209.5 |
| PS | 1 \times | >12.5 | 14.5 |
| PS | 8 \times | >12.5 | 203.5 |
| HDTV | 1 \times | >30 | 44.25 |
| HDTV | 2 \times | >30 | 118.5 |

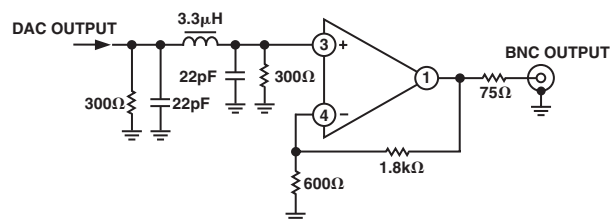


Figure 56. Example for Output Filter for PS, 8x Oversampling

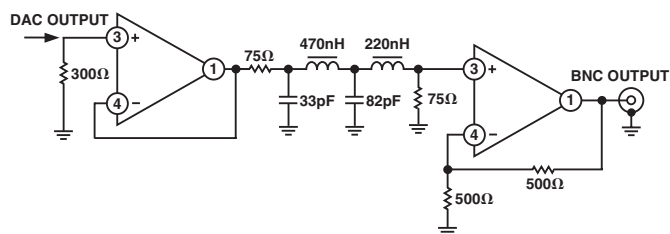


Figure 57. Example for Output Filter for HDTV, 2x Oversampling

Table XVII shows possible output rates from the ADV7314.

Table XVII.

| Input Mode Address 01h, Bit 6-4 | PLL Address 00h, Bit 1 | Output Rate |
|------------------------------------|---------------------------|----------------|
| SD Only | Off | 27 MHz (2x) |
| | On | 216 MHz (16x) |
| PS Only | Off | 27 MHz (1x) |
| | On | 216 MHz (8x) |
| HDTV Only | Off | 74.25 MHz (1x) |
| | On | 148.5 MHz (2x) |

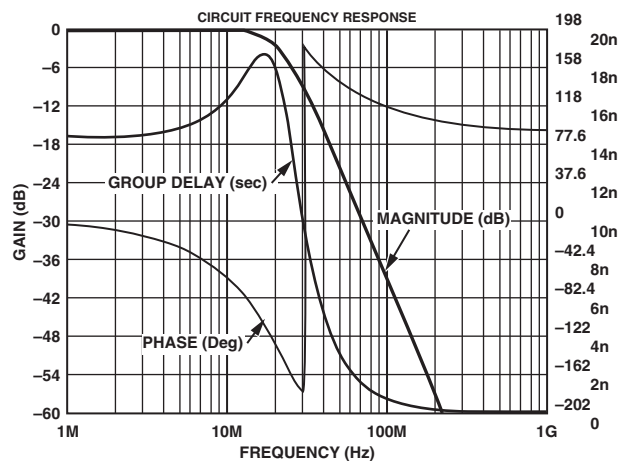


Figure 58. Filter Plot for Output Filter for PS, 8x Oversampling

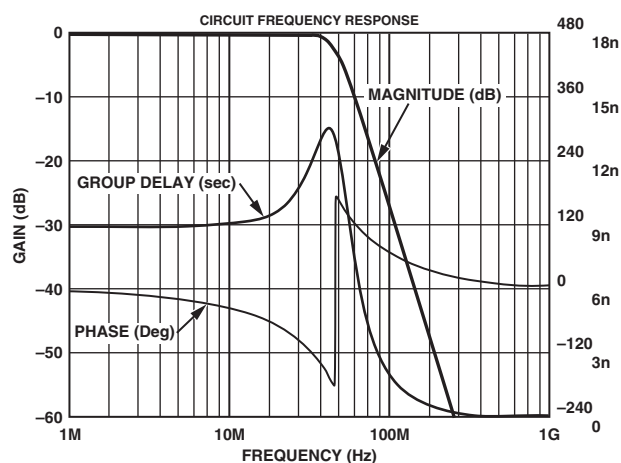


Figure 59. Example for Output Filter HDTV, 2x Oversampling

ADV7314

PC BOARD LAYOUT CONSIDERATIONS

The ADV7314 is optimally designed for lowest noise performance, for both radiated and conducted noise. To complement the excellent noise performance of the ADV7314, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7314 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND, V_{DD} and DGND, and V_{DD_IO} and GND_IO pins should be kept as short as possible to minimized inductive ringing.

It is recommended that a 4-layer printed circuit board is used with power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Component placement should be carefully considered in order to separate noisy circuits, such as crystal clocks, high speed logic circuitry, and analog circuitry.

There should be a separate analog ground plane and a separate digital ground plane.

Power planes should encompass a digital power plane and an analog power plane. The analog power plane should contain the DACs and all associated circuitry, V_{REF} circuitry. The digital power plane should contain all logic circuitry.

The analog and digital power planes should be individually connected to the common power plane at one single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces will reduce noise pickup due to neighboring digital circuitry.

To avoid crosstalk between the DAC outputs, it is recommended to leave as much space as possible between the tracks of the individual DAC output pins. The addition of ground tracks between outputs is also recommended.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors.

Optimum performance is achieved by the use of 10 nF and 0.1 μ F ceramic capacitors. Each of group of V_{AA} , V_{DD} , or V_{DD_IO} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

A 1 μ F tantalum capacitor is recommended across the V_{AA} supply in addition to a 10 nF ceramic capacitor. See Figure 60.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7314 should be avoided to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not to the analog power plane.

Analog Signal Interconnect

The ADV7314 should be located as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch.

For optimum performance, the analog outputs should each be source and load terminated, as shown in Figure 60. The termination resistors should be as close as possible to the ADV7314 to minimize reflections.

For optimum performance, it is recommended that all decoupling and external components relating to the ADV7314 be located on the same side of the PCB and as close as possible to the ADV7314.

Any unused inputs should be tied to ground.

ADV7314

APPENDIX 1—COPY GENERATION MANAGEMENT SYSTEM

PS CGMS Data Registers 2–0

[Subaddress 21h, 22h, 23h]

PS CGMS is available in 525p mode conforming to CGMS-A EIA-J CPR1204-1, transfer method of video ID information using vertical blanking interval (525p system), March 1998, and IEC61880, 1998, Video systems (525/60)—video and accompanied data using the vertical blanking interval—analogue interface.

When PS CGMS is enabled [Subaddress 12h, Bit 6 = 1], CGMS data is inserted on line 41. The PS CGMS data registers are at Addresses 21h, 22h, and 23h.

SD CGMS Data Registers 2–0

[Subaddress 59h, 5Ah, 5Bh]

The ADV7314 supports Copy Generation Management System (CGMS), conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of even fields. Bits C/W05 and C/W06 control whether or not CGMS data is output on odd and even fields. CGMS data can be transmitted only when the ADV7314 is configured in NTSC mode. The CGMS data is 20 bits long, and the function of each of these bits is as shown in Table XVIII. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit; see Figure 62.

HD/PS CGMS [Address 12h, Bit 6]

The ADV7314 supports Copy Generation Management System (CGMS) in HDTV mode (720p and 1080i) in accordance with EIAJ CPR-1204-2.

The HD CGMS data registers can be found at Address 021h, 22h, 23h.

Function of CGMS Bits

Word 0–6 bits; Word 1–4 bits; Word 2–6 bits; CRC 6 bits
CRC polynomial = $x^6 + x + 1$ (preset to 111111)

720p System

CGMS data is applied to Line 24 of the luminance vertical blanking interval.

1080i System

CGMS data is applied to Line 19 and on Line 582 of the luminance vertical blanking interval.

CGMS Functionality

If SD CGMS CRC [Address 59h, Bit 4] or PS/HD CGMS CRC [Subaddress 12h, Bit 7] is set to a Logic 1, the last six bits, C19–C14, which comprise the 6-bit CRC check sequence, are calculated automatically on the ADV7314 based on the lower 14 bits (C0–C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111. If SD CGMS CRC [Address 59h, Bit 4] or PS/HD CGMS CRC [Address 12h, Bit 7] is set to a Logic 0, all 20 bits (C0–C19) are output directly from the CGMS registers (no CRC calculated, must be calculated by the user).

Table XVIII.

| Bit | Function |
|--------------------|--|
| WORD0 | 1 0 |
| B1 | Aspect ratio 16:9 4:3 |
| B2 | Display format Letterbox Normal |
| B3 | Undefined |
| WORD0 | |
| B4, B5, B6 | Identification information about video and other signals (e.g., audio) |
| WORD1 | |
| B7, B8, B9, B10 | Identification signal incidental to Word 0 |
| WORD2 | |
| B11, B12, B13, B14 | Identification signal and information incidental to Word 0 |

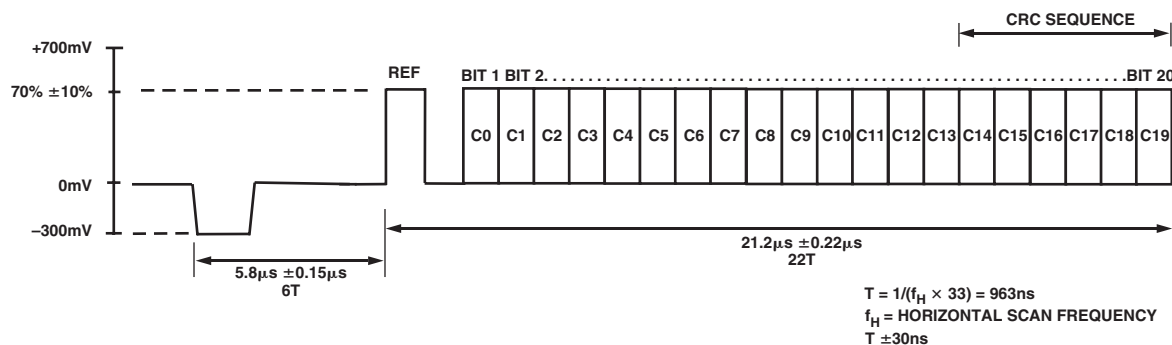


Figure 61. Progressive Scan CGMS Waveform

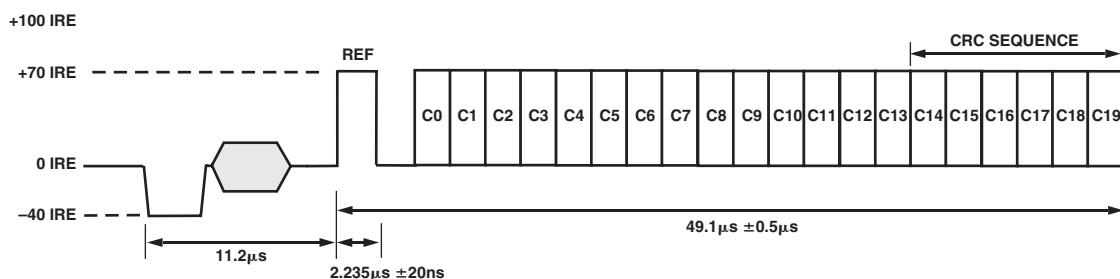


Figure 62. Standard Definition CGMS Waveform

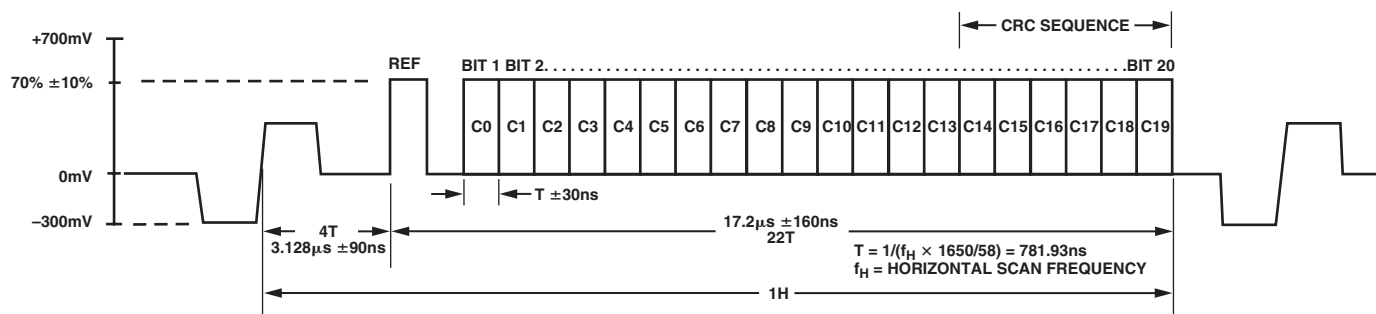


Figure 63. HDTV 720P CGMS Waveform

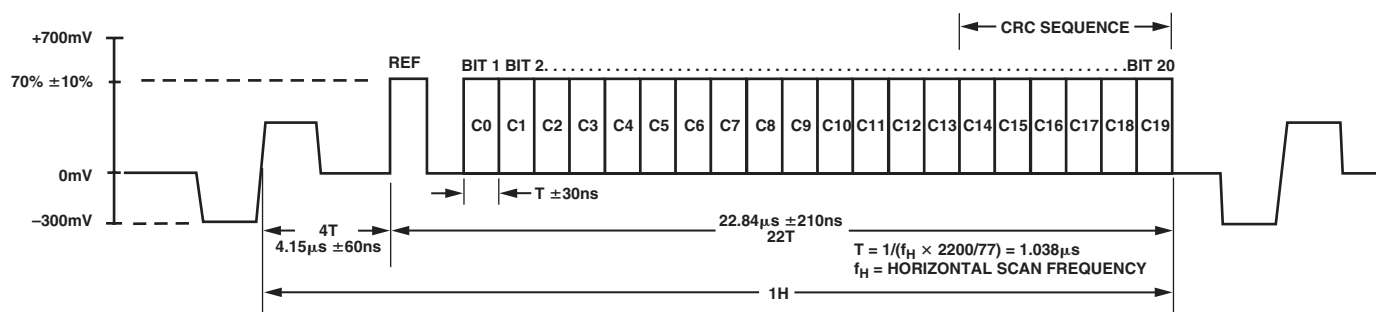


Figure 64. HDTV 1080i CGMS Waveform

ADV7314

APPENDIX 2—SD WIDE SCREEN SIGNALING

[Subaddress 59h, 5Ah, 5Bh]

The ADV7314 supports wide screen signaling (WSS) conforming to the standard. WSS data is transmitted on Line 23. WSS data can be transmitted only when the ADV7314 is configured in PAL mode. The WSS data is 14 bits long, and the function of each of these bits is as shown in Table XIX. The WSS data is preceded

by a run-in sequence and a start code (see Figure 65). If SD WSS [Address 59h, Bit 7] is set to a Logic 1, it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5 μ s from the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video.

It is possible to blank the WSS portion of Line 23 with Subaddress 61h, Bit 7.

Table XIX. Function of WSS Bits

| Bit | Description | Bit | Description |
|----------------|--------------------------------------|--------|------------------------------------|
| Bit 0–Bit 2 | Aspect Ratio/Format/Position Bits | B6 | |
| Bit 3 | IS Odd Parity Check of Bit 0–Bit 2 | 0 | No Helper |
| B0, B1, B2, B3 | Aspect Ratio Format Position | 1 | Modulated Helper |
| 0 0 0 1 | 4:3 Full Format Not applicable | B7 | Reserved |
| 1 0 0 0 | 14:9 Letterbox Center | B9 B10 | |
| 0 1 0 0 | 14:9 Letterbox Top | 0 0 | No Open Subtitles |
| 1 1 0 1 | 16:9 Letterbox Center | 1 0 | Subtitles in Active Image Area |
| 0 0 1 0 | 16:9 Letterbox Top | 0 1 | Subtitles out of Active Image Area |
| 1 0 1 1 | >16:9 Letterbox Center | 1 1 | Reserved |
| 0 1 1 1 | 14:9 Full Format Center | B11 | |
| 1 1 1 0 | 16:9 N/A N/A | 0 | No Surround Sound Information |
| B4 | | 1 | Surround Sound Mode |
| 0 | Camera Mode | B12 | Reserved |
| 1 | Film Mode | B13 | Reserved |
| B5 | | | |
| 0 | Standard Coding | | |
| 1 | Motion Adaptive Color Plus | | |

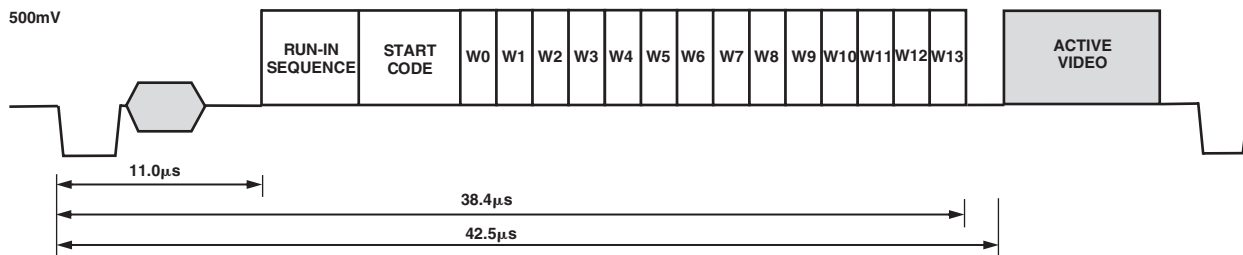


Figure 65. WSS Waveform Diagram

APPENDIX 3—SD CLOSED CAPTIONING

[Subaddress 51h–54h]

The ADV7314 supports closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency- and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic Level 1 start bit. 16 bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits, and one odd parity bit. The data for these bytes is stored in the SD closed captioning registers [Address 53h–54h].

The ADV7314 also supports the extended closed captioning operation, which is active during even fields and is encoded on Scan Line 284. The data for this operation is stored in the SD closed captioning registers [Address 51h–52h].

All clock run-in signals and timing to support closed captioning on Lines 21 and 284 are generated automatically by the ADV7314. All pixels inputs are ignored during Lines 21 and 284 if closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7314 uses a single buffering method. This means that the closed captioning buffer is only one byte deep, therefore there will be no frame delay in outputting the closed captioning data unlike other two byte deep buffering systems. The data must be loaded one line before (Line 20 or Line 283) it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn will load the new data (two bytes) every field. If no new data is required for transmission, 0s must be inserted in both data registers, which is called nulling. It is also important to load control codes, all of that are double bytes on Line 21 or a television will not recognize them. If there is a message like Hello World that has an odd number of characters, it is important to pad it out to even in order to get end-of-caption 2-byte control code to land in the same field.

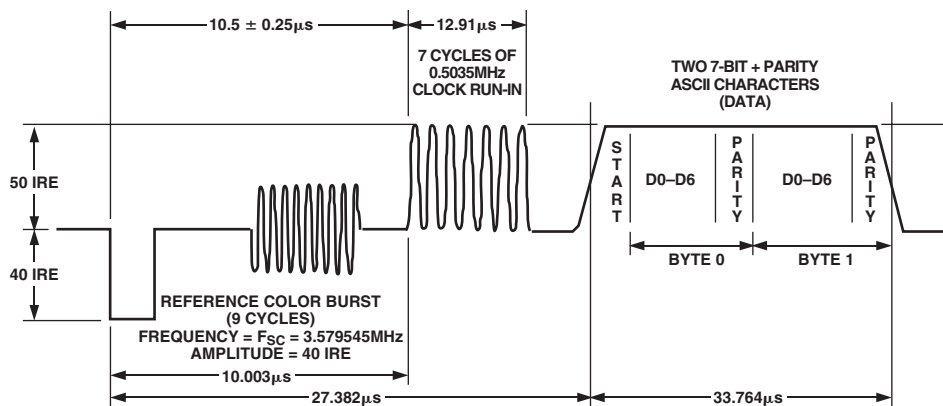


Figure 66. Closed Captioning Waveform, NTSC

ADV7314

APPENDIX 4—TEST PATTERNS

The ADV7314 can generate SD and HD test patterns.

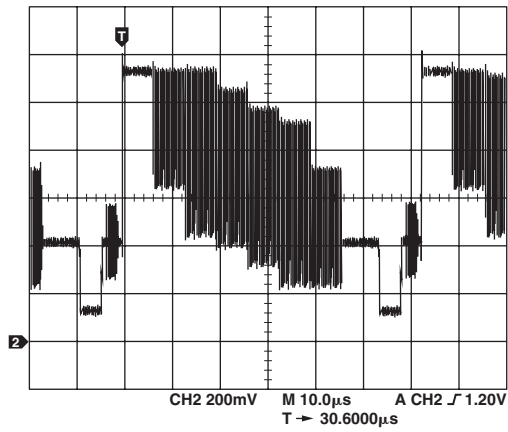


Figure 67. NTSC Color Bars

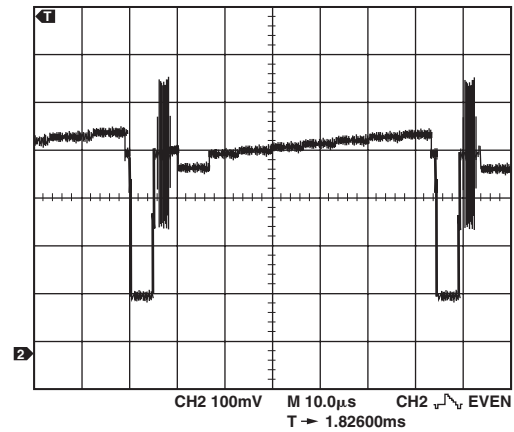


Figure 70. PAL Black Bar (–21 mV, 0 mV, 3.5 mV, 7 mV, 10.5 mV, 14 mV, 18 mV, 23 mV)

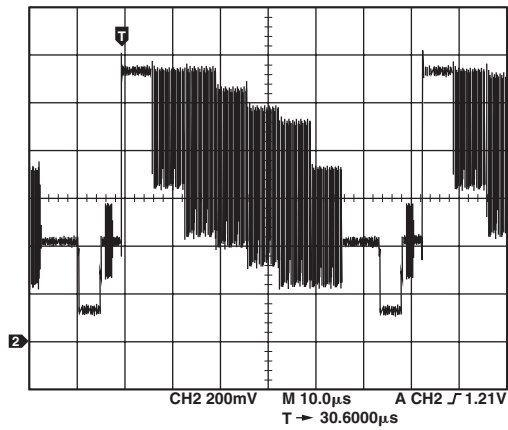


Figure 68. PAL Color Bars

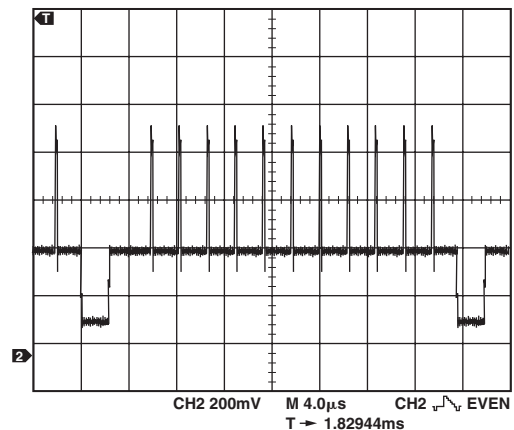


Figure 71. 525p Hatch Pattern

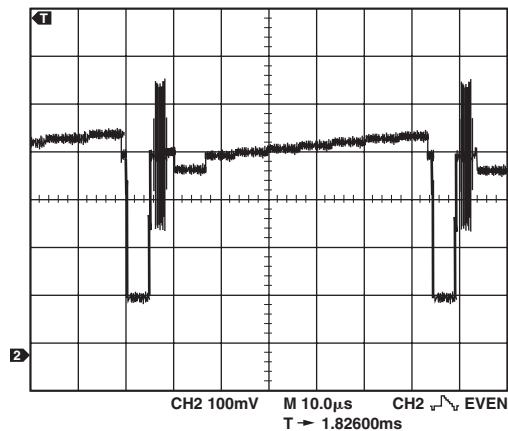


Figure 69. NTSC Black Bar (–21 mV, 0 mV, 3.5 mV, 7 mV, 10.5 mV, 14 mV, 18 mV, 23 mV)

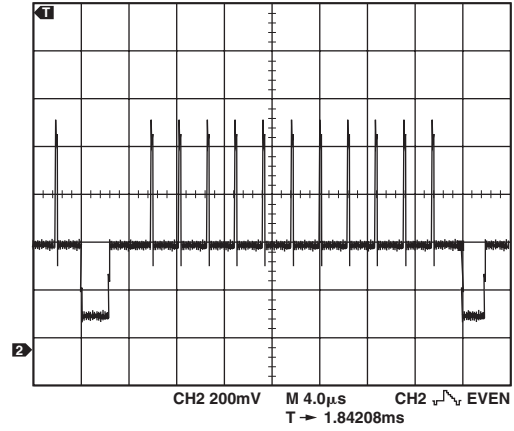


Figure 72. 625p Hatch Pattern

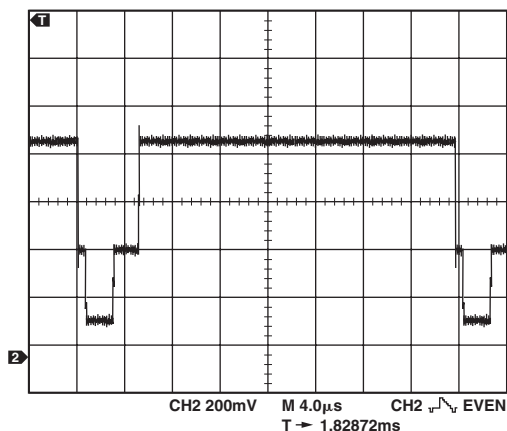


Figure 73. 525p Field Pattern

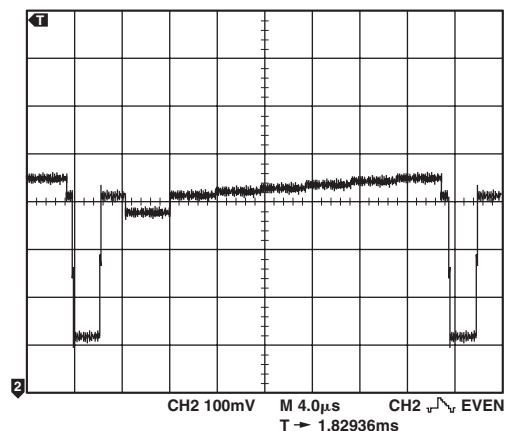


Figure 75. 625p Field Pattern

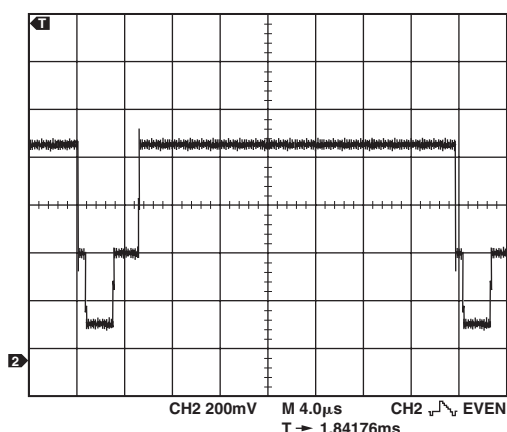


Figure 74. 525p Black Bar (-35 mV, 0 mV, 7 mV, 14 mV, 21 mV, 28 mV, 35 mV)

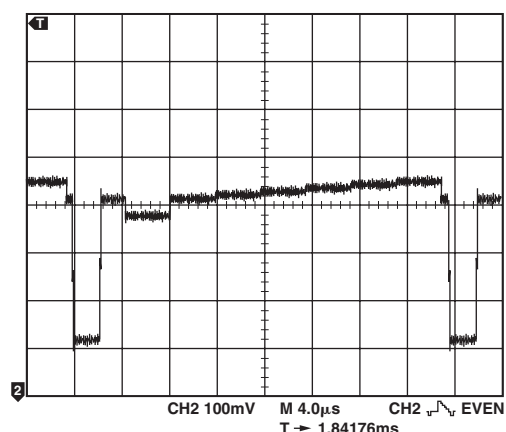


Figure 76. 625p Black Bar (-35 mV, 0 mV, 7 mV, 14 mV, 21 mV, 28 mV, 35 mV)

The following register settings are used to generate an SD NTSC CVBS output on DAC A.

| Subaddress | Register Setting |
|------------|------------------|
| 00h | 80h |
| 40h | 10h |
| 42h | 40h |
| 44h | 40h |
| 4Ah | 08h |

*All other registers are set to default/normal settings.

For PAL CVBS output on DAC A, the same settings are used except that Subaddress 40h is changed to 11h.

The following register settings are used to generate an SD NTSC black bar pattern output on DAC A.

| Subaddress | Register Setting |
|------------|------------------|
| 00h | 80h |
| 02h | 04h |
| 40h | 10h |
| 42h | 40h |
| 44h | 40h |
| 4Ah | 08h |

*All other registers are set to default/normal settings.

For PAL black bar pattern output on DAC A, the same settings are used except that subaddress = 40h and register setting = 11h.

The following register settings are used to generate a 525p hatch pattern on DAC D.

| Subaddress | Register Setting |
|------------|------------------|
| 00h | 80h |
| 01h | 10h |
| 10h | 40h |
| 11h | 05h |
| 16h | A0h |
| 17h | 80h |
| 18h | 80h |

*All other registers are set to default/normal settings.

For 625p hatch pattern on DAC D, the same register settings are used except that subaddress = 10h and register setting = 50h.

For a 525p black bar pattern output on DAC D, the same settings are used as for a 525p hatch pattern except that subaddress = 02h and register setting = 24h.

For 625p black bar pattern output on DAC D, the same settings are used as for a 625p hatch pattern except that subaddress = 02h and register setting = 24h; and subaddress = 10h and register setting = 50h.

ADV7314

APPENDIX 5—SD TIMING MODES

[Subaddress 4Ah]

Mode 0 (CCIR-656)—Slave Option

(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7314 is controlled by the SAV (start active video) and EAV (end active video) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. $\overline{S_VSYNC}$, $\overline{S_HSYNC}$, and $\overline{S_BLANK}$ (if not used) pins should be tied high during this mode. Blank output is available.

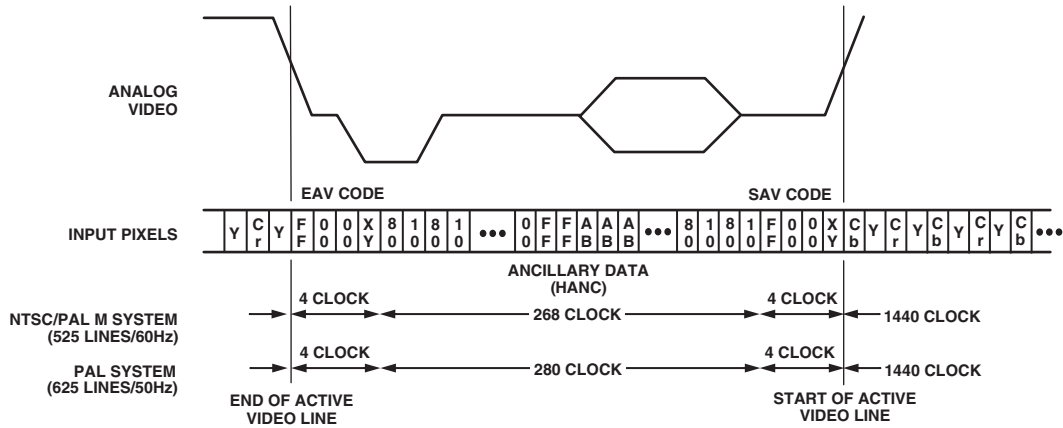


Figure 77. SD Slave Mode 0

Mode 0 (CCIR-656)—Master Option

(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7314 generates H, V, and F signals required for the SAV (start active video) and EAV (end active video) time codes in the CCIR656 standard. The H bit is output on $\overline{S_HSYNC}$, the V bit is output on $\overline{S_BLANK}$, and the F bit is output on $\overline{S_VSYNC}$ pin.

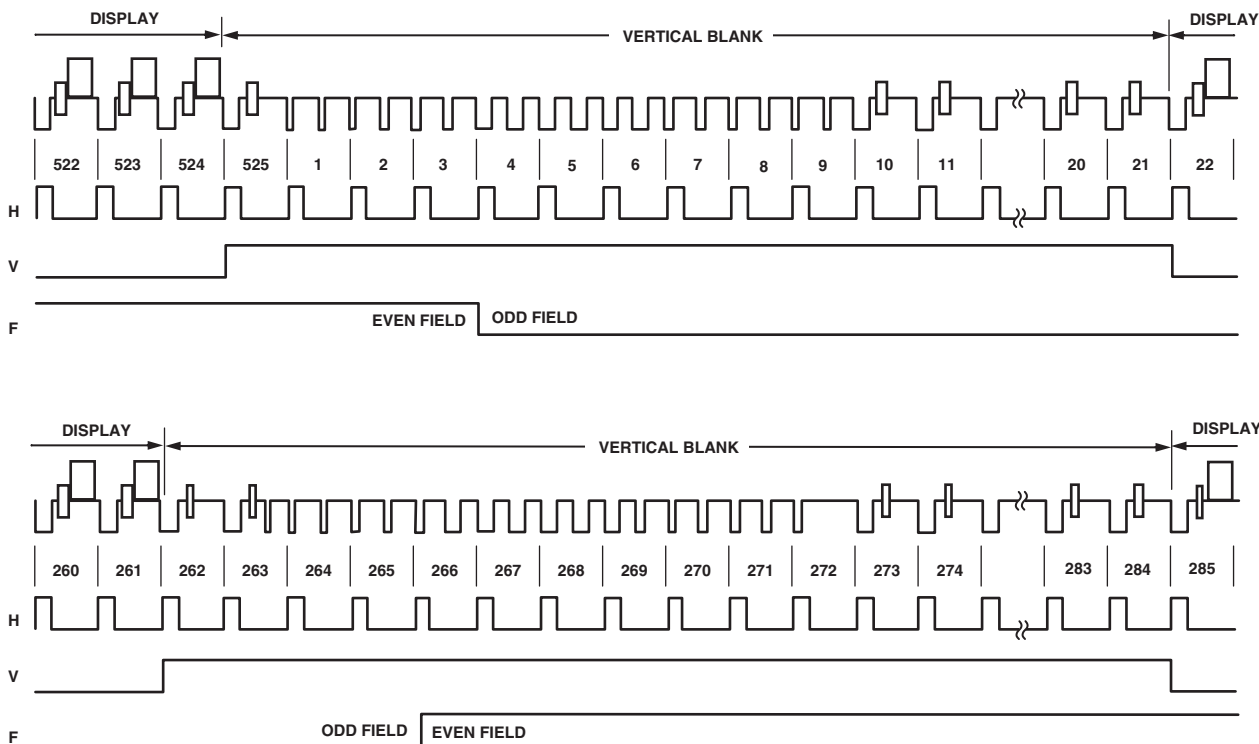


Figure 78. SD Master Mode 0 (NTSC)

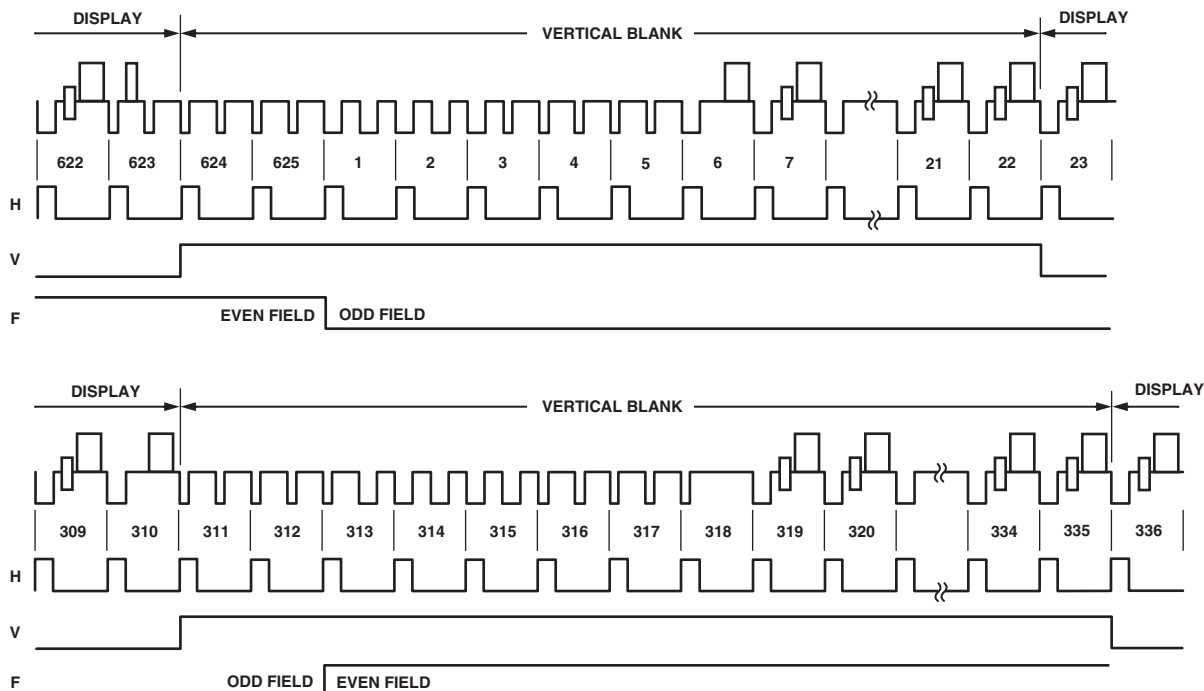


Figure 79. SD Master Mode 0 (PAL)

ADV7314

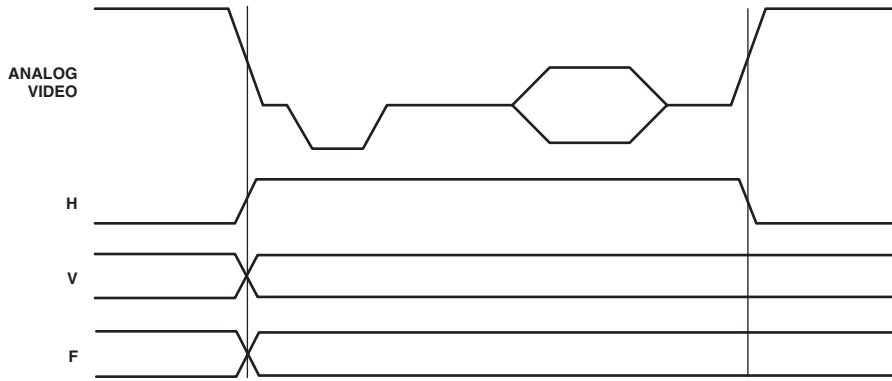


Figure 80. SD Master Mode 0, Data Transitions

Mode 1—Slave Option

(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode, the ADV7314 accepts horizontal SYNC and odd/even field signals. A transition of the field input when $\overline{\text{HSYNC}}$ is low indicates a new frame, i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7314 automatically blanks all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ is input on $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ on $\overline{\text{S_BLANK}}$, and FIELD on $\overline{\text{S_VSYNC}}$.

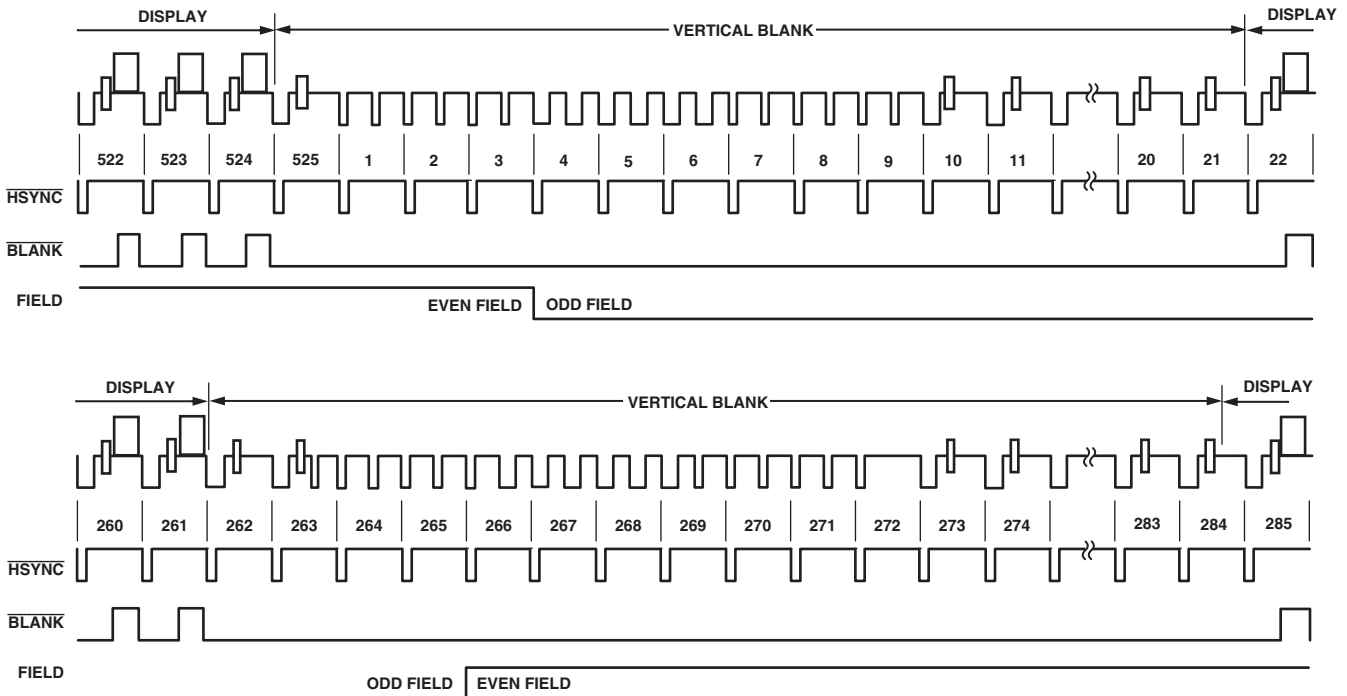


Figure 81. SD Slave Mode 1 (NTSC)

Mode 1—Master Option

(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode, the ADV7314 can generate horizontal sync and odd/even field signals. A transition of the field input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7314 automatically blanks all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$ is output on the $\overline{\text{S_HSYNC}}$, $\overline{\text{BLANK}}$ on $\overline{\text{S_BLANK}}$, and FIELD on $\overline{\text{S_VSYNC}}$.

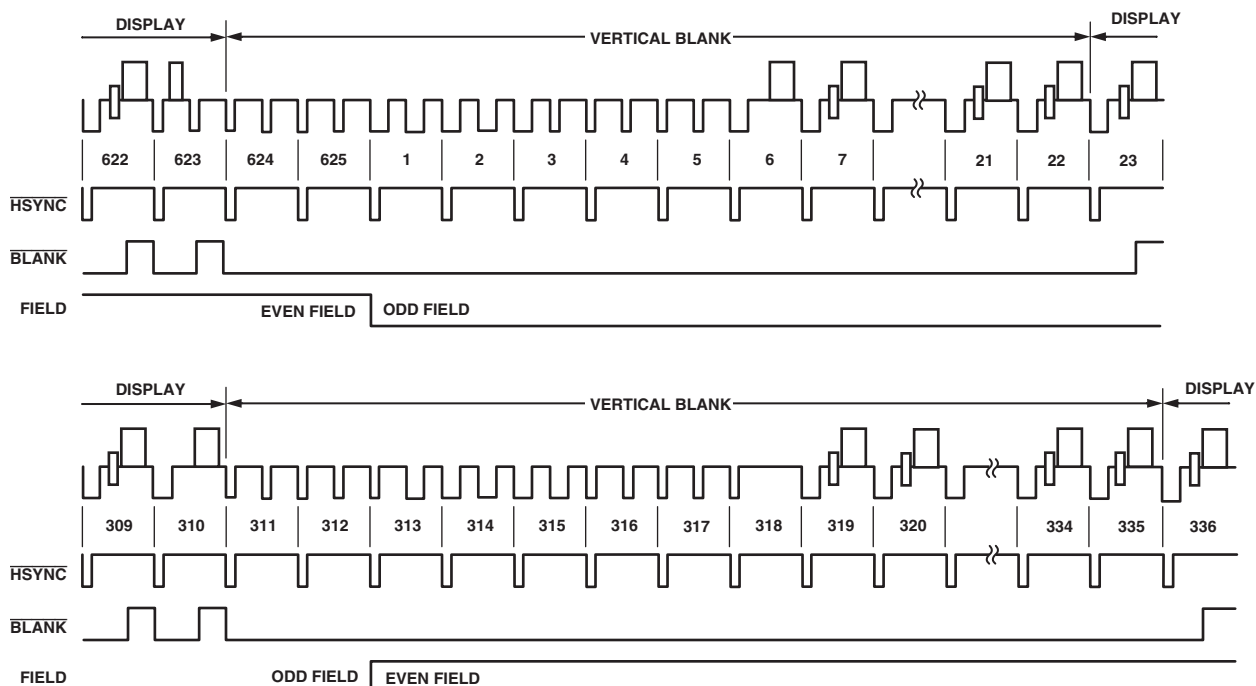


Figure 82. SD Slave Mode 1 (PAL)

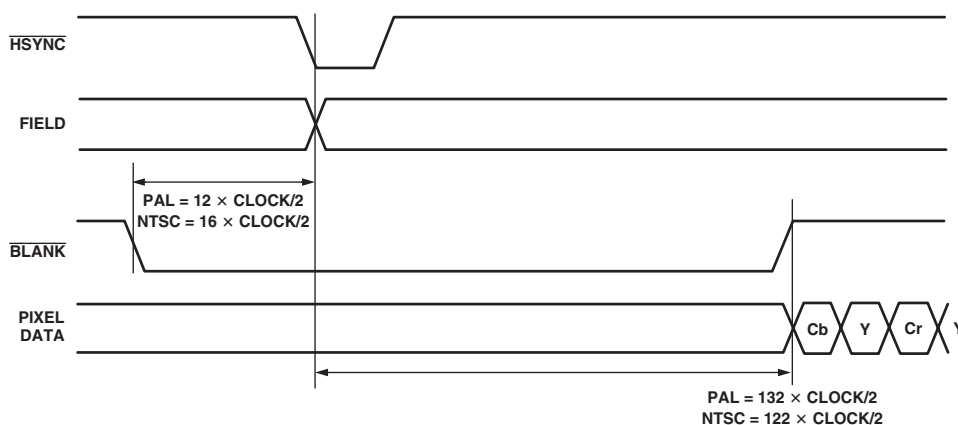


Figure 83. SD Timing Mode 1—Odd/Even Field Transitions Master/Slave

ADV7314

Mode 2—Slave Option

(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode, the ADV7314 accepts horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The BLANK signal is optional. When the BLANK input is disabled the ADV7314 automatically blanks all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ is input $\overline{\text{S_HSYNC}}$, BLANK on $\overline{\text{S_BLANK}}$, and $\overline{\text{VSYNC}}$ on $\overline{\text{S_VSYNC}}$.

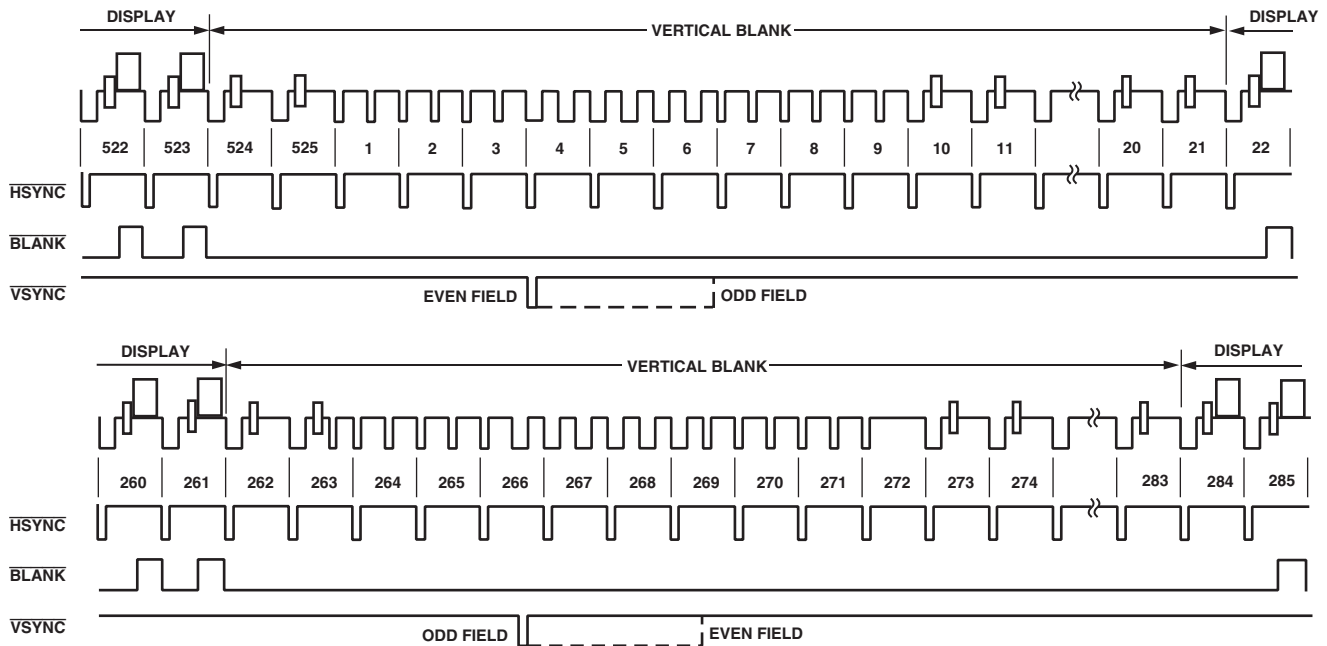


Figure 84. SD Slave Mode 2 (NTSC)

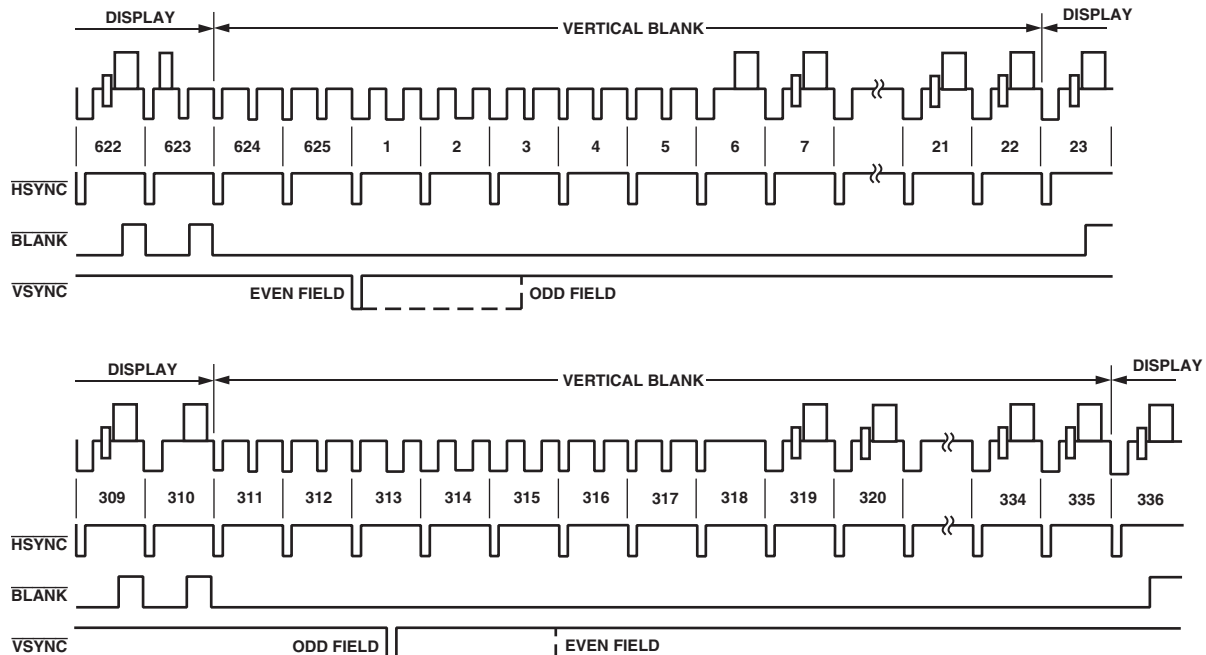


Figure 85. SD Slave Mode 2 (PAL)

Mode 2—Master Option

(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode, the ADV7314 can generate horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7314 automatically blanks all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ is output on $\overline{\text{S_HSYNC}}$, $\overline{\text{BLANK}}$ on $\overline{\text{S_BLANK}}$, and $\overline{\text{VSYNC}}$ on $\overline{\text{S_VSYNC}}$.

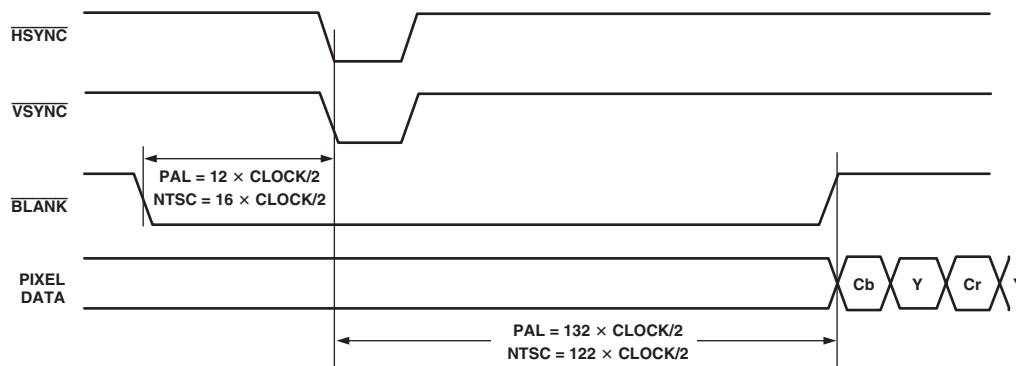


Figure 86. SD Timing Mode 2 Even-to-Odd Field Transition Master/Slave

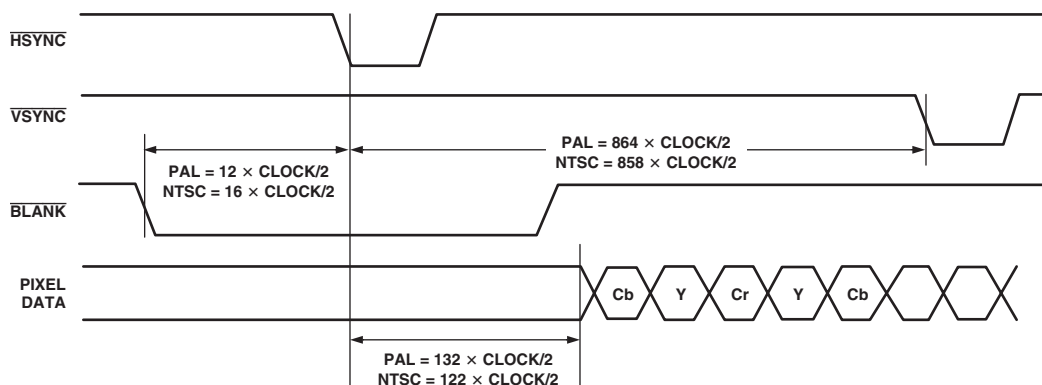


Figure 87. SD Timing Mode 2 Odd-to-Even Field Transition Master/Slave

ADV7314

Mode 3—Master/Slave Option

(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode, the ADV7314 accepts or generates horizontal sync and odd/even field signals. A transition of the field input when $\overline{\text{HSYNC}}$ is high indicates a new frame i.e., vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7314 automatically blanks all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$ is output in master mode and input in slave mode on $\overline{\text{S_HSYNC}}$, $\overline{\text{BLANK}}$ on $\overline{\text{S_BLANK}}$, and $\overline{\text{VSYNC}}$ on $\overline{\text{S_VSYNC}}$.

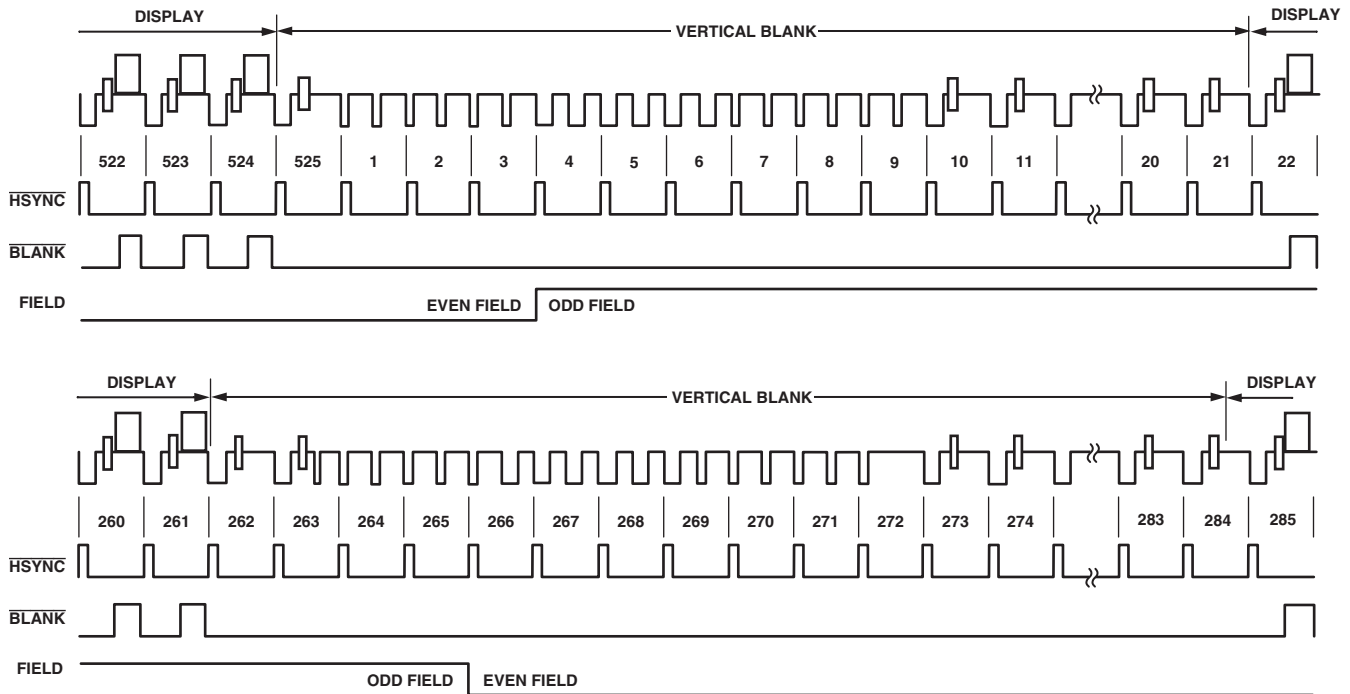


Figure 88. SD Timing Mode 3 (NTSC)

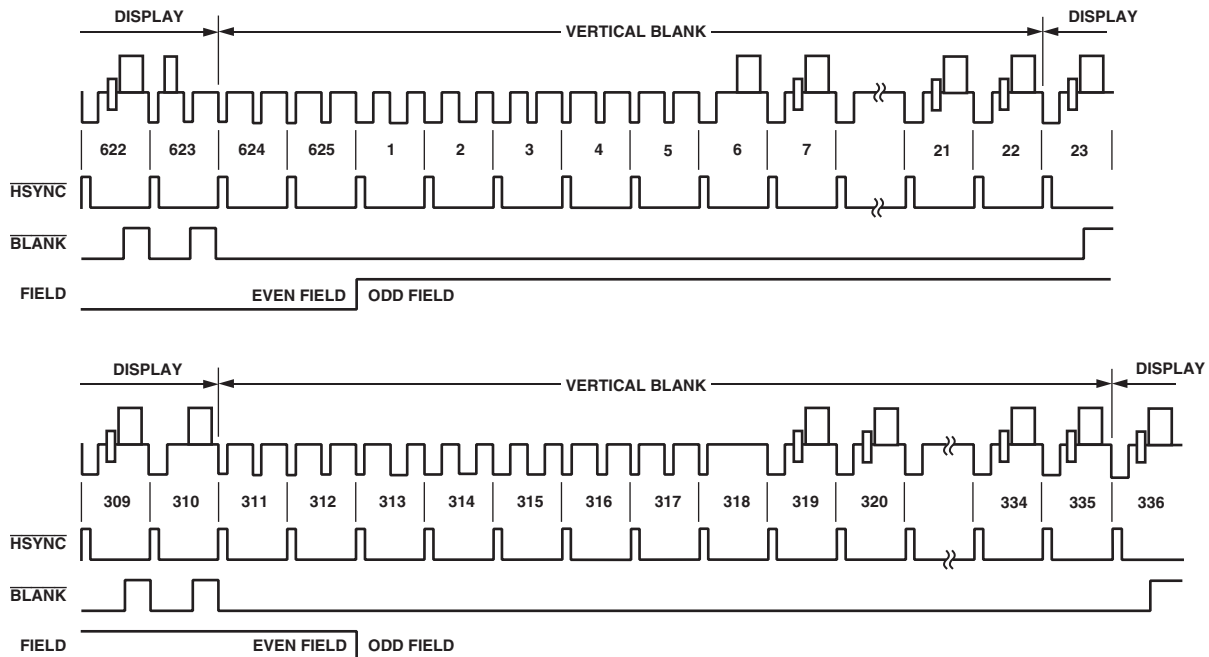


Figure 89. SD Timing Mode 3 (PAL)

APPENDIX 6—HD TIMING

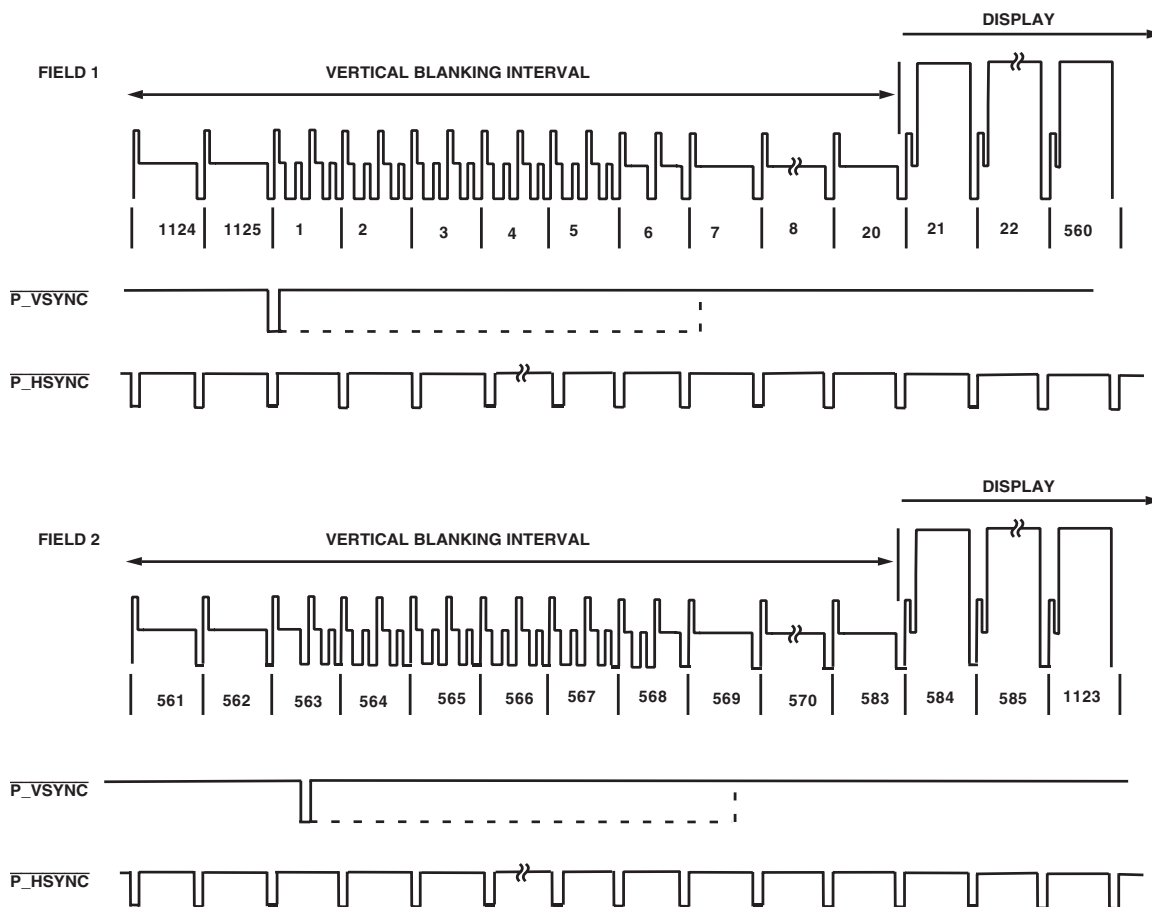


Figure 90. 1080i HSYNC and VSYNC Input Timing

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APPENDIX 7—VIDEO OUTPUT LEVELS HD YPrPb Output Levels

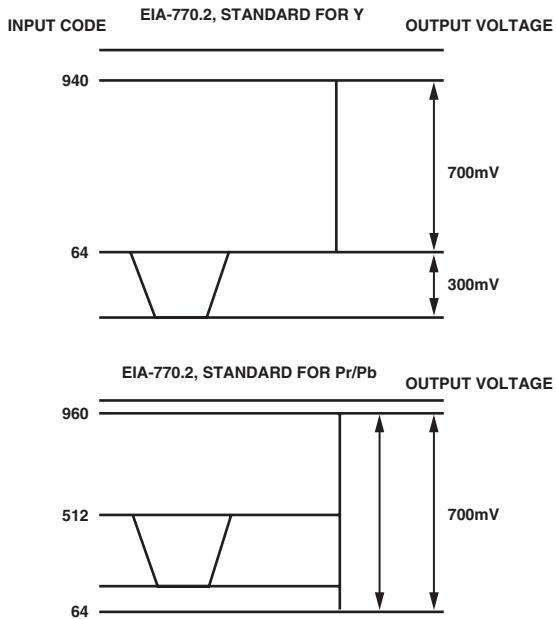


Figure 91. EIA 770.2 Standard Output Signals (525p/625p)

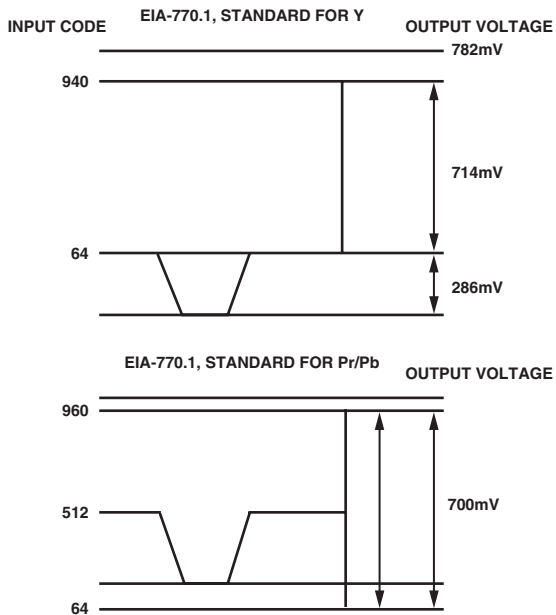


Figure 92. EIA 770.1 Standard Output Signals (525p/625p)

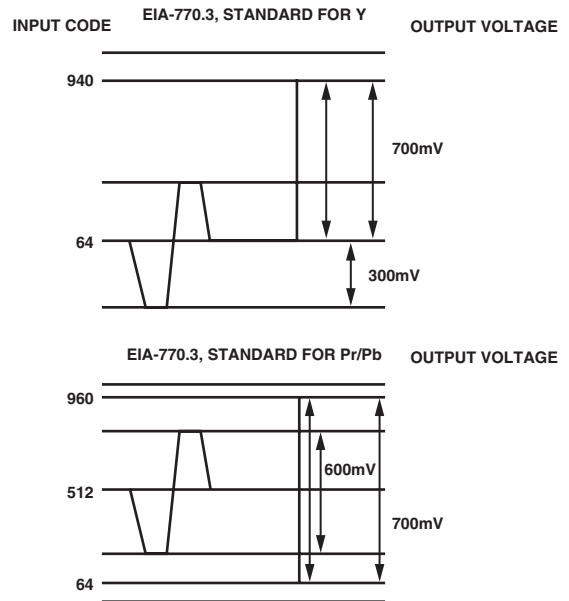


Figure 93. EIA 770.3 Standard Output Signals (1080i, 720p)

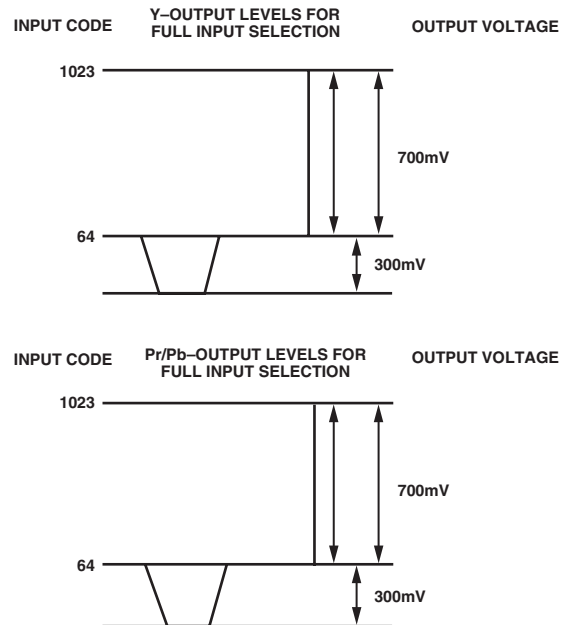


Figure 94. Output Levels for Full Input Selection

RGB Output Levels

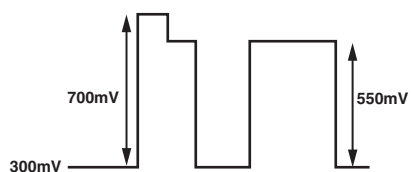
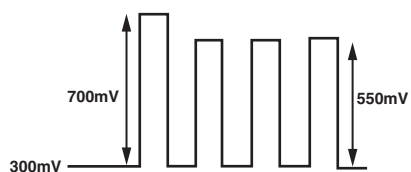
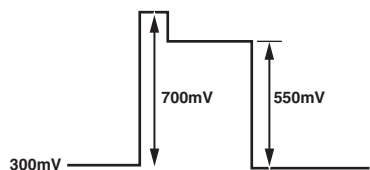


Figure 95. HD RGB Output Levels

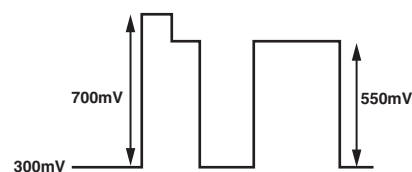
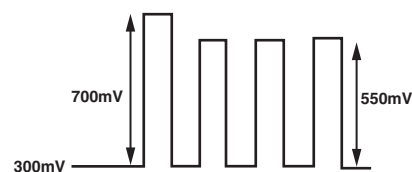
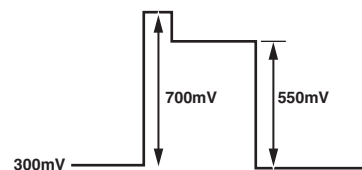


Figure 97. SD RGB Output Levels—RGB Sync Disabled

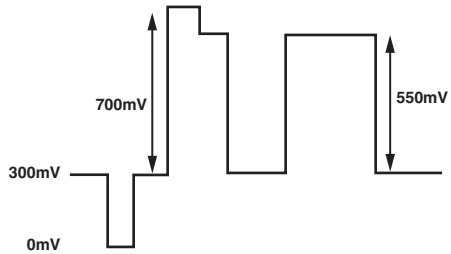
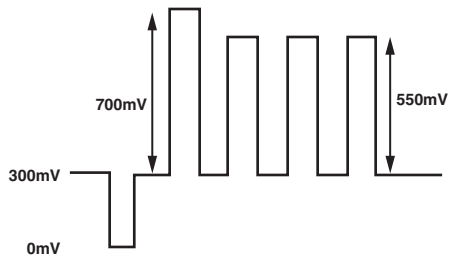
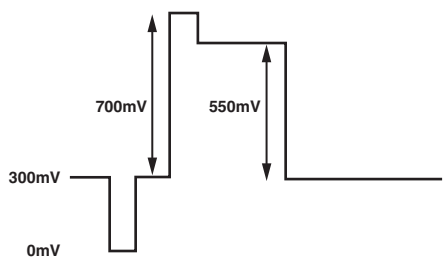


Figure 96. HD RGB Output Levels—RGB Sync Enabled

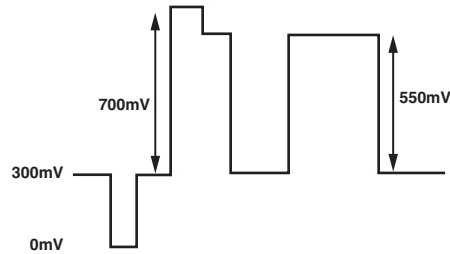
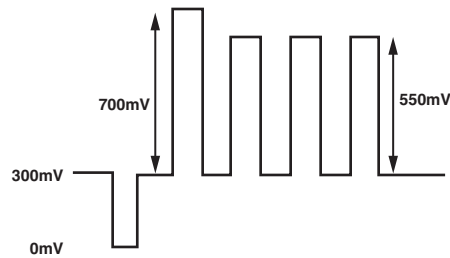
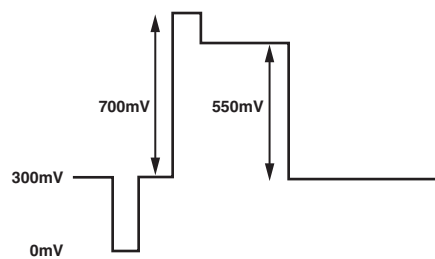


Figure 98. SD RGB Output Levels—RGB Sync Enabled

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YPrPb Output Levels

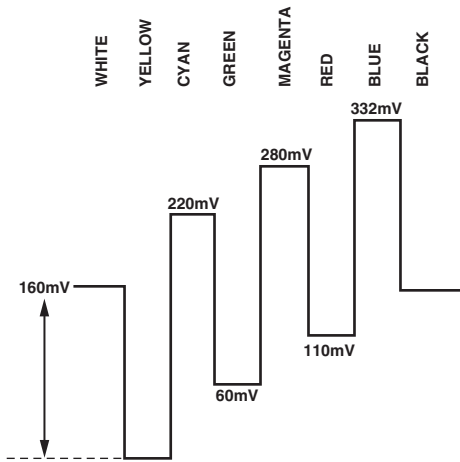


Figure 99. U Levels—NTSC

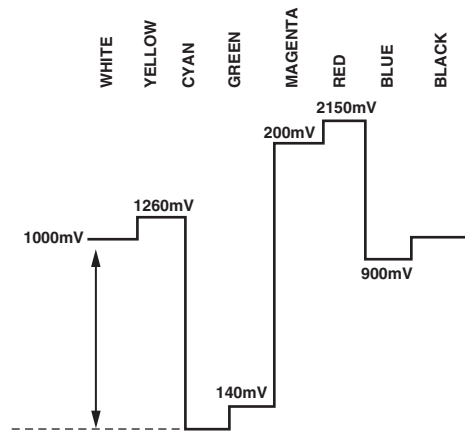


Figure 102. U Levels—PAL

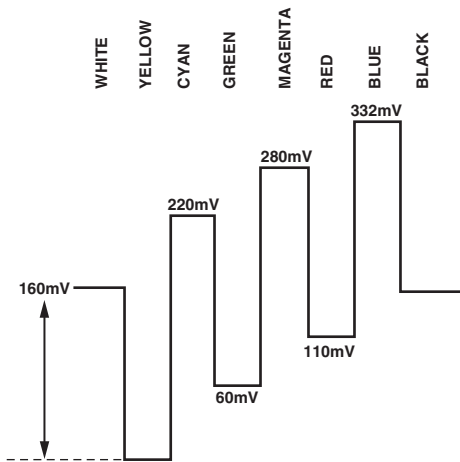


Figure 100. U Levels—PAL

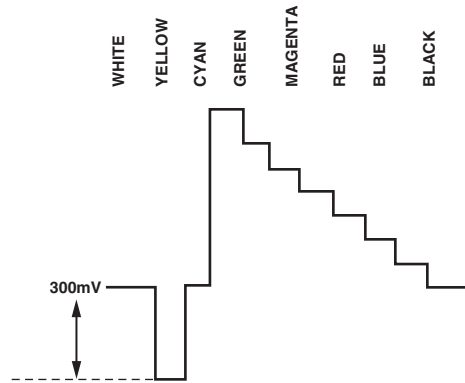


Figure 103. Y Levels—NTSC

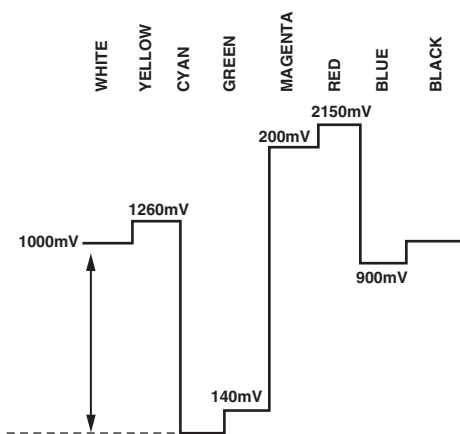


Figure 101. U Levels—NTSC

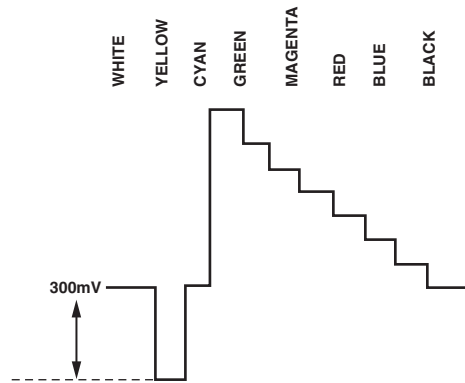


Figure 104. Y Levels—PAL

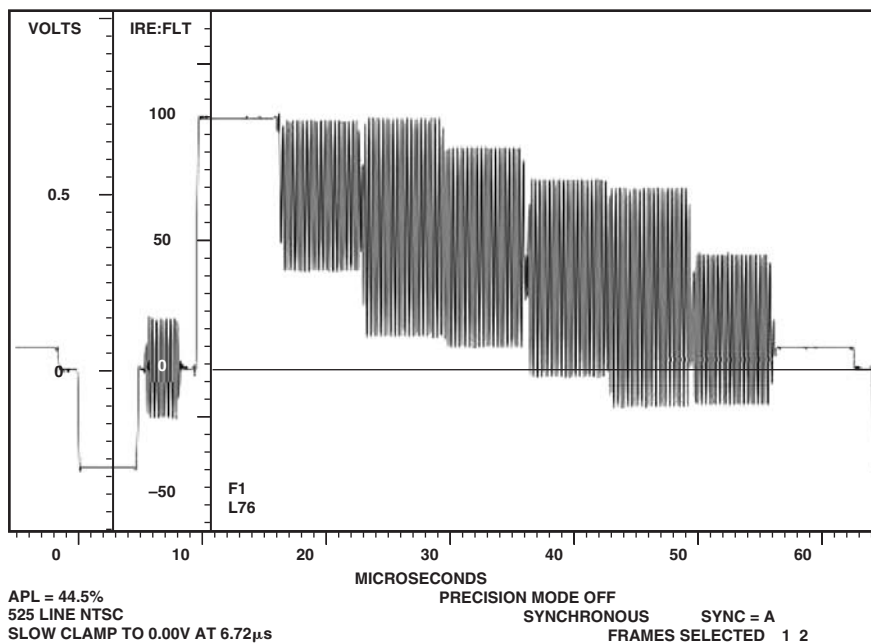


Figure 105. NTSC Color Bars 75%

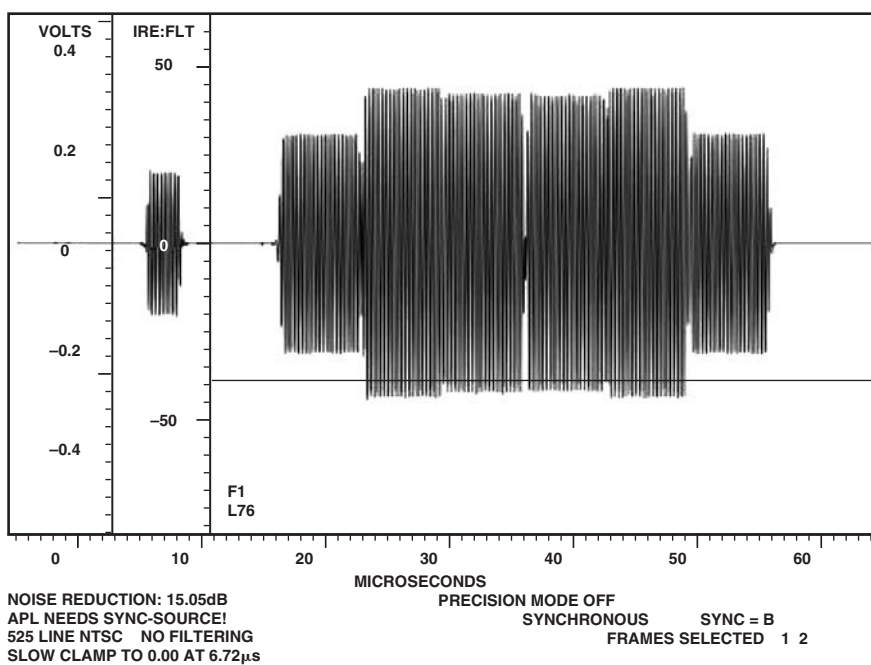


Figure 106. NTSC Chroma

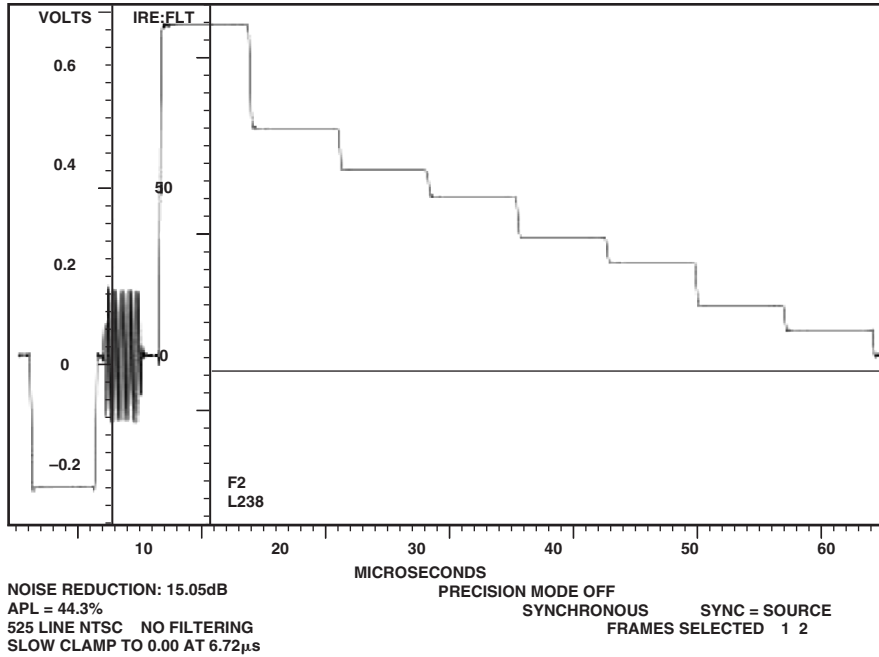


Figure 107. NTSC Luma

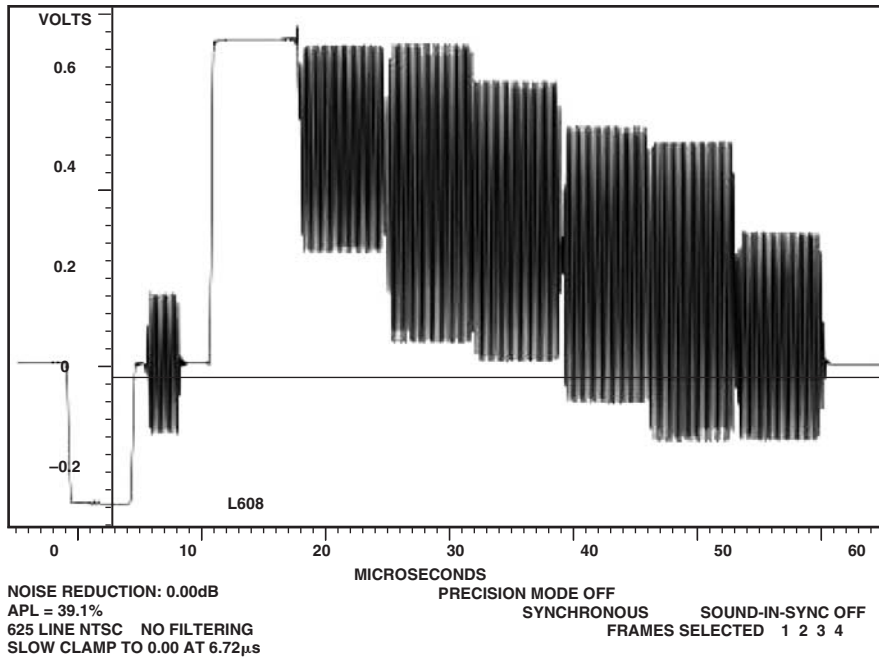


Figure 108. PAL Color Bars 75%

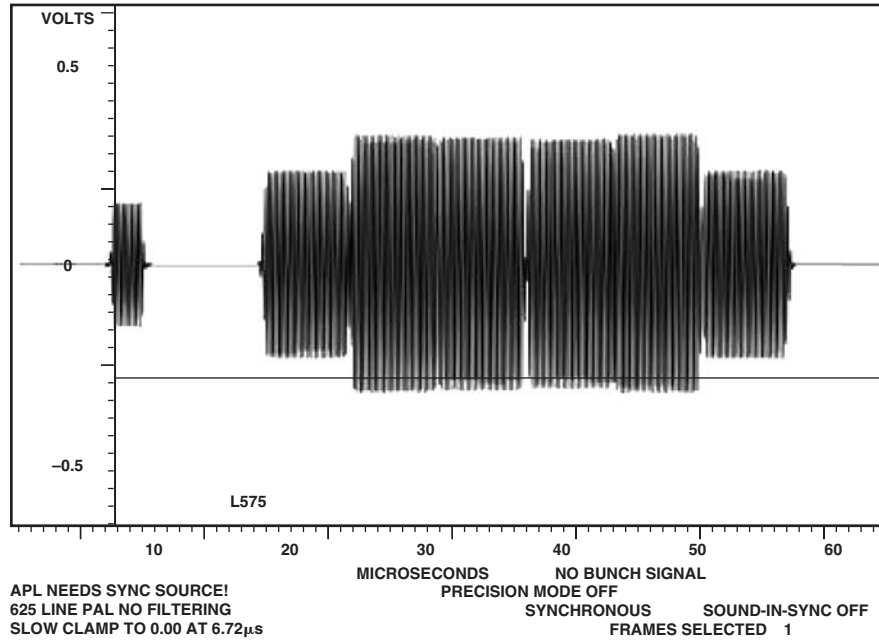


Figure 109. PAL Chroma

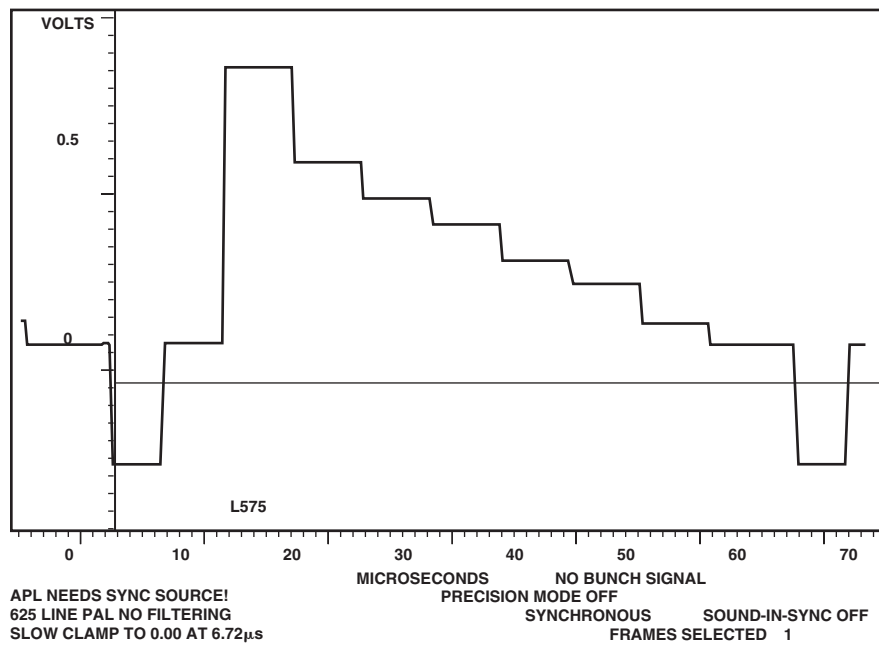


Figure 110. PAL Luma

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APPENDIX 8—VIDEO STANDARDS

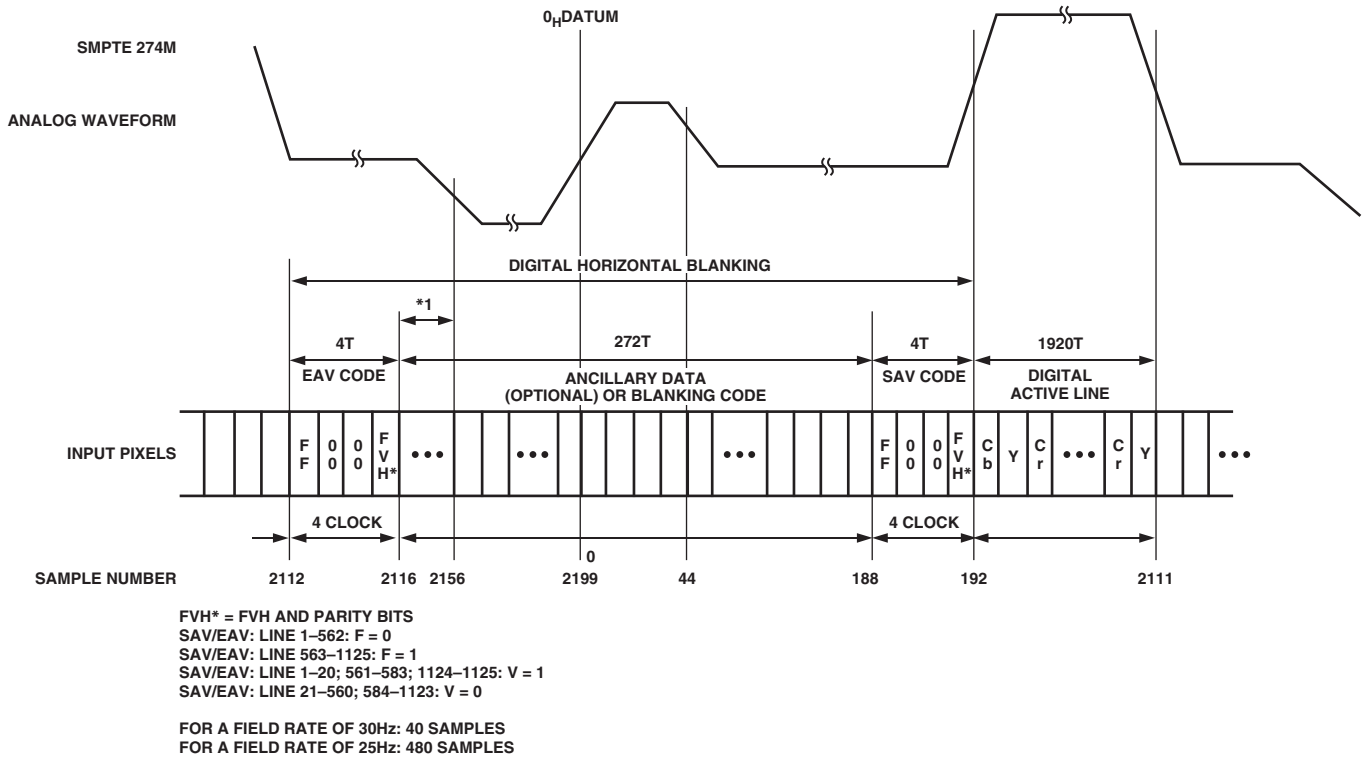


Figure 111. EAV/SAV Input Data Timing Diagram—SMPTE 274M

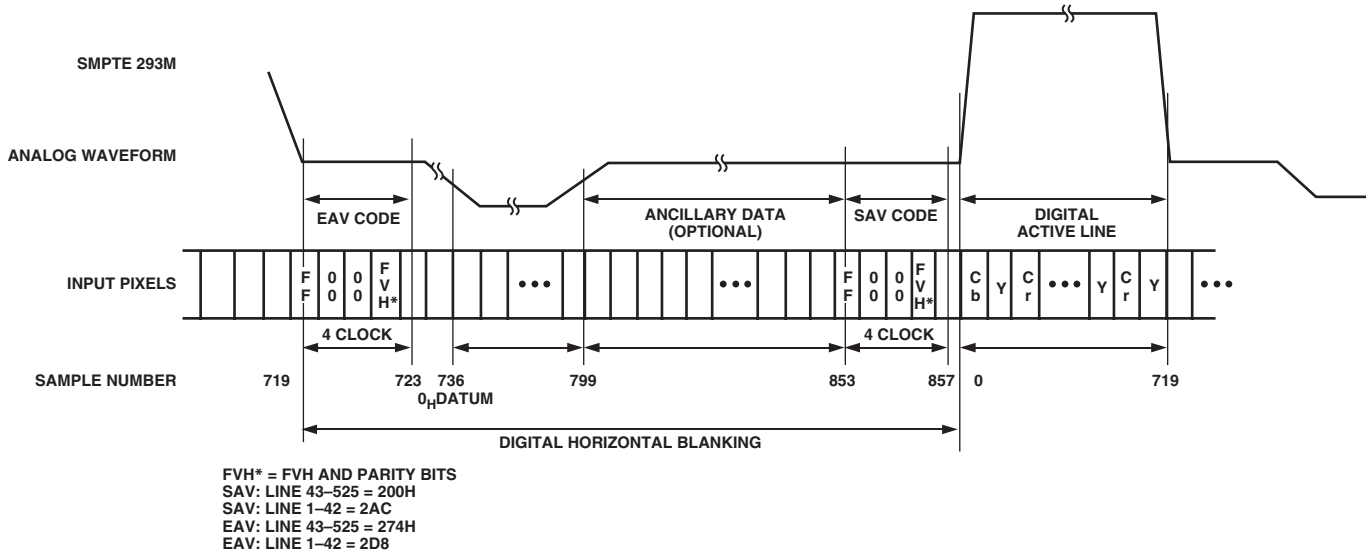


Figure 112. EAV/SAV Input Data Timing Diagram—SMPTE 293M

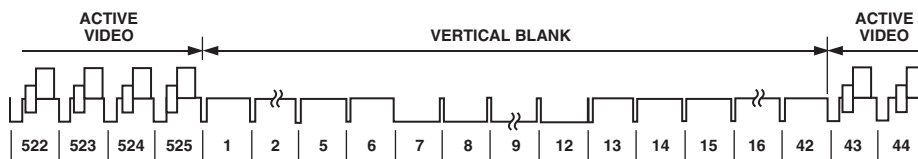


Figure 113. SMPTE 293M (525p)

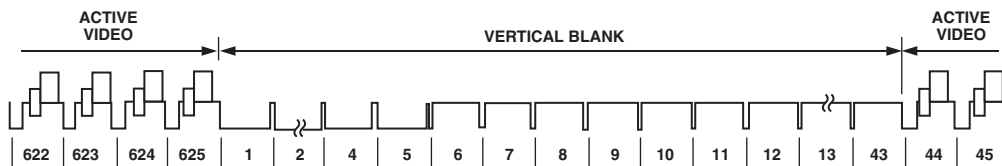


Figure 114. ITU-R BT.1358 (625p)

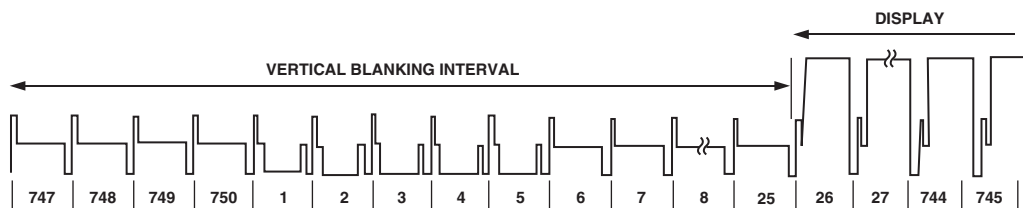


Figure 115. SMPTE 296M (720p)

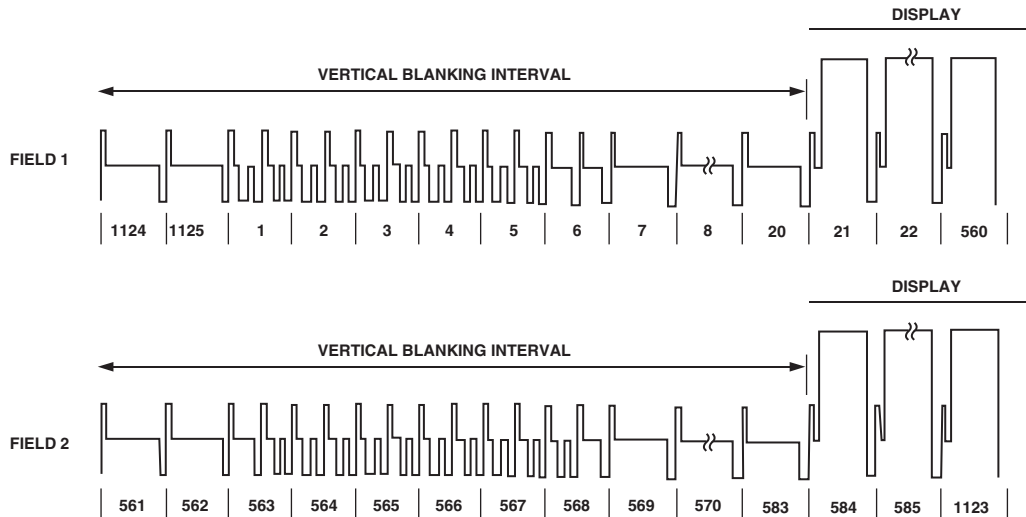
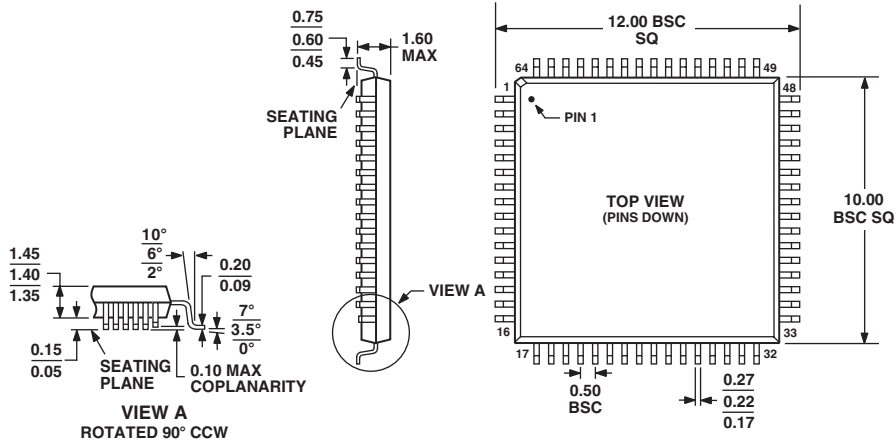


Figure 116. SMPTE 274M (1080i)

OUTLINE DIMENSIONS

64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BCD

