PC104-73LD1
FOUR LVDT "PROGRAMMABLE" TRACKING CONVERTERS
WITH WRAP-AROUNDSELF TEST. +5 VDC ONLY

FEATURES:
- Only +5 VDC.
- 16 bit Resolution
- Accuracy 0.025% FS
- Continuous background bit testing with Reference and Signal loss detection
- 360 Hz to 10 Khz
- Transformer isolated
- Programmable reference and signal voltages
- Accurate Digital Velocity outputs
- Latch feature
- Synthetic reference compensates for ±60° phase shift
- No adjustments or trimming required
- 8 bit or 16 bit data bus versions

DESCRIPTION:

This PC104 compliant stackthrough module offers four (4) separate transformer isolated "PROGRAMMABLE" LVDT/RVDT-to-Digital tracking converters with extensive diagnostics, digital velocity, and (A+B) outputs. Instead of buying cards that are set for specific inputs, the uniqueness of this design makes it possible to order our generic card that is Autoranging between 2.0 and 28 volts for 4-wire LVTD input. For 2-wire inputs, the card can be programmed and reprogrammed in the field for any excitation and signal voltage between 2.0 and 28 volts. This card uses a derived reference ratiometric design approach that is insensitive to magnitude, temperature, frequency and phase shift effects. The conversion technique assures that the output will change only when the LVDT position changes and will ignore excitation voltage variations. The "Latch" feature permits the user to read all channels at the same time. Reading will unlatch that channel. The converters utilize a Type II servo loop processing technique that enables tracking, at full accuracy, up to the specified rate. Intermediate transparent latches, on all data and velocity outputs, guarantee that current valid data is always available for any channel without effecting the tracking performance of the converters. The optional on–board excitation supply can be factory set for a particular voltage and frequency, or can be supplied as field programmable. To simplify logistics, Part number, S/N, Date code, & Rev. are stored in permanent memory locations.

Major diagnostic are incorporated that offer substantial improvements to system reliability because user is immediately alerted to channel malfunctions. Self-Test (POST) diagnostic can immediately initiate (D3) test. **See Programming Instructions for further details.** Three different tests (one on-line and two off-line) can be selected:

The (D2) test initiates automatic background bit testing. Each channel is checked over the Signal range to a measuring accuracy 0.1% FS, and each Signal and Excitation is monitored. Results are available in registers The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The (D3) or POST test, if enabled, starts an initiated bit test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.1%FS. Results can be read from Status registers. External excitation is not required. The testing is totally transparent to the user, requires no external programming, and can be enabled or disabled via the bus. Power-On (POST) test can be enabled or disabled via the bus.

The (D0) test is used to check the card and the interface. All channels are disconnected from the outside world allowing user to write any number of input voltages to the card and then read the data from the interface. External excitation is not required.

SPECIFICATIONS:

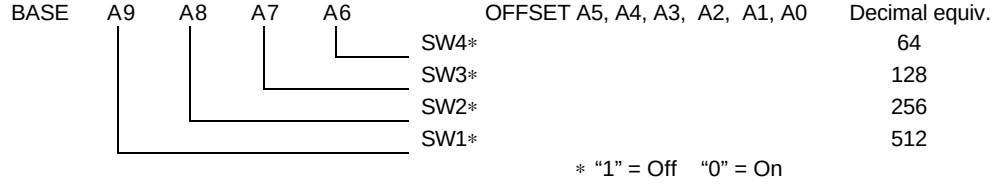
Number of channels:	8 or 16 (see part number)
Resolution:	16 bit
Accuracy:	0.025% FS
Band width:	40 Hz at 400 Hz; 200Hz >100 Hz. BW and tracking rate can easily be customized.
Input format:	LVDT or RVDT
Input voltage (4-wire):	Autoranging from 2.0 to 28 Vrms. Transformer isolated.
Input voltage (2-wire):	2.0 to 28 Vrms programmable with 0.01 V resolution. Transformer isolated.
Excitation voltage (4-wire):	Not required
Excitation voltage (2-wire):	2.0 to 28 Vrms programmable with 0.01 V resolution. Transformer isolated.
Input Impedance:	40 kΩ min. at 360 Hz
Frequency:	360 Hz to 10 Khz, broadband
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60°
Velocity, Digital:	16 bit resolution; Linearity: 0.1%
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Power:	+ 5 VDC at 0.35 A ±12 VDC at 0.1 A without Excitation; 1.1 A for 5 VA Excitation Output
Temperature, operating:	-40°C to +80°C
Storage temperature:	-55°C to +105°C
Size:	4.5 x 13.5 x 0.74
Weight:	12 oz.

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:

This card requires 64 consecutive addresses in the I/O address space on a 64 byte boundary. The base address is switch settable in the 000-3E0 hex (0 to 992) address range.

ADDRESS= BASE + OFFSET



NOTE: Base addresses to avoid:

320-32F	Hard Disk	3B0-3BF	Monochrome Display	3F8-3FF	Asynch Comm I/O
378-37F	Parallel Printer Port	3F0-3F7	Floppy Disk		

Offset: Page 1 (Offset 1F = 0)

00	Ch.1 Lo read	09	Vel.1 Hi read	12	Status, Test read	1A	Test angle Hi read/write
01	Ch.1 Hi read	0A	Vel.2 Lo read	13	Status, Test read	1F	0 read/write
02	Ch.2 Lo read	0B	Vel.2 Hi read	14	Test Enable read/write		
03	Ch.2 Hi read	10	Status, Lo read	16	Test (D2) verify read/write		
08	Vel.1 Lo read	11	Status, Hi read	19	Test angle Lo read/write		

Offset: Page 2 (Offset 1F = 1)

08	Velocity, scale Ch.1 Lo read/write	12	Ref. Freq. Lo read/write	18	Date code Lo read
09	Velocity, scale Ch.1 Hi read/write	13	Ref. Freq. Hi read/write	19	Date code Hi read
0A	Velocity, scale Ch.2 Lo read/write	14	P/N Lo read	1A	Rev. level Lo read
0B	Velocity, scale Ch.2 Hi read/write	15	P/N Hi read	1B	Rev. level Hi read
10	Ref. Eo Lo read/write	16	S/N Lo read	1C	Active channels read/write
11	Ref. Eo Hi read/write	17	S/N Hi read	1F	1 read/write

Offset: Page 3 (Offset 1F = 2)

00 Save	write	07 Exc. Ch.2 Hi	read/write	0C Sig. Ch.1 Lo	read/write	11 Sig. Ch.3 Hi	read/write
02 Latch	write	08 Exc. Ch.3 Lo	read/write	0D Sig. Ch.1 Hi	read/write	12 Sig. Ch.4 Lo	read/write
04 Exc. Ch.1 Lo	read/write	09 Exc. Ch.3 Hi	read/write	0E Sig. Ch.2 Lo	read/write	13 Sig. Ch.4 Hi	read/write
05 Exc. Ch.1 Hi	read/write	0A Exc. Ch.4 Lo	read/write	0F Sig. Ch.2 Hi	read/write	14 Power-On (POST) enable	read/write
06 Exc. Ch.2 Lo	read/write	0B Exc. Ch.4 Hi	read/write	10 Sig. Ch.3 Lo	read/write	1F 2	read/write

	Hi byte								Lo byte							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	Sign	5.000	2.500	1.250	.6250	.3125	.1563	.0781	.0391	.0195	.0098	.0049	.0024.	.0012	.0006	.0003
Data, Velocity (rps)	Sign	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Active channels	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1
Status, signal	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1
Status, excitation	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Power ON or system reset, **unless POST (Page 3, 1Eh is set to ("1") and saved,** disables D3 test, all channels unlatched, excitation supply frequency to 400 Hz and output voltage to zero. Program required frequency before increasing output voltage.

Enter all active channels at Page 3, 1Ah "1" =active; "0" =not used. Omitting this step will produce false alarms because unused channels will set faults. To **save** when all channels are programmed, write 5555h at Page 1, 1Ah. Board will clear to hex 00 when save is completed. These settings will repeat until changed. Saving is optional. If not saved, reenter at each power on. To restore factory shipped parameters, write AAAAh at Page 1, 1Ah, wait until board writes 00, then do a system reset.

Data Format: Two's complement. Sign: (D15) 0=In Phase; 1= Out of Phase. Offset Binary (two's complement with MSB inverted) can be specified. (see part number) The output represents A-B/A+B. Max. positive excursion is 7FFF, 0=0, and max. negative excursion is 8000.

Programming Signal and Reference: The LVDT primary, as usual, is energized by either the excitation output from this card or from an external excitation.

The **signal voltage** to be programmed represents the max. output voltage of the LVDT. The 4-wire LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs no scaling is required because the inputs are Autoranging. For 2-wire LVDT's scaling is required as follows:

Set Excitation and Signal voltages by writing a 16 bit binary word to the appropriate address.

Ex: 27.11 V Signal to Ch.2 = 0000101010010111 to Page 2, 02h/03h
26.00 V Excitation to Ch.2 = 0000101000101000 to Page 3, 02h/03h.

(A+B) output: Read binary number and multiply by 0.01 Volt.

Velocity: 16 bit resolution, (15 bit+sign, 2's compliment); Linearity: 0.1%.

If velocity scale factor is set to max. (FFFFh), then 1 bit of velocity output = 0.4% FS/sec. Ex: If full stroke is ±3" (6" total) and you read a velocity output of 630h, then the velocity is 630 x 0.004 x 6 = 15.12 inches/sec

Status, Test: "1" Accuracy OK; "0" failed. **Status:** "1" Exc. & Signal are On; "0" Exc. and/or Signal loss.

Test Enable (D2): Writing "1" to D2 at Page 2, 1Eh, initiates automatic background bit testing Each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS, and each Signal and Excitation is monitored. The results are available in status registers. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Card will write hex 55 at Page 3, 18h when (D2) is enabled. User can periodically clear to hex 00 and then read Page 3, 18h again to verify that background bit testing is activated.

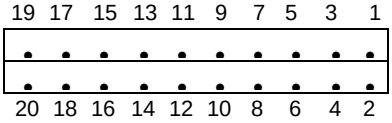
Test Enable (D3): Power-on (POST) if enabled, or writing "1" to D3 at Page 2, 1Eh, starts an initiated bit test that disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple test voltages that are measured to a test accuracy and of 0.1%FS. Test cycle takes about 10 seconds and results can be read from registers when D3 changes from "1" to "0". External excitation is not required. Testing is totally transparent to the user, requires no external programming, and can be enabled or disabled (by setting D3 to "0") via the bus.

Test Enable (D0): Checks the card and the interface. Writing "1" to D0 at Page 2, 1Eh, disconnects all channels from the outside world, allowing user to write any number of input voltages to the card at Page 1, 18h/19h, and then read the data from the interface (allow 50 ms after writing). External excitation is not required.

CONNECTOR: Samtec
TSW-110-25TDRA

Pin	Sig. Lo	Sig. Hi	Exc. Lo	Exc. Hi
CH. 1	5	6	8	7
CH. 2	9	10	12	11
CH. 3	13	14	16	15
CH. 4	17	18	20	19

Pin numbers (Facing pins from component side of board)



PART NUMBER DESIGNATION

73LD1- 4 X X X

Options
0 = none
9 = custom (see separate spec)

BUS
1 = 8-bit ISA bus
2 = 16-bit ISA bus

Environmental
C = No conformal coating
K = Removable conformal coating
L = Permanent conformal coating

Total number Channels