

# VS12G476

Registered I/O,  
Self-Timed, 1K x 4 Static RAM

## Features

- 1024 by 4-bit static RAM for cache or control store applications
- Very fast Read/Write cycle time ..... 2.5 ns
- Single power supply (2 Volts)
- Completely static operation
- Very low sensitivity to total dose radiation
- 'Native' GaAs compatible inputs and outputs for ultra high speed interface
- Registered data inputs and outputs
- 28-pin leaded or leadless ceramic packages
- Fully decoded synchronous operation
- Low power dissipation ..... < 1 W Typ

## Functional Description

The Vitesse VS12G476 is a very high speed, fully decoded synchronous 1024 x 4-bit read/write static random access memory. The VS12G476 is self-timed and all data inputs and outputs are registered. The product needs only a single 2 Volt power supply. It is compatible in ECL board environments between -2 and 0 Volts, or in GaAs circuit board environments between 0 and +2 Volts. Input and output signal levels are shifted accordingly.

This product is designed to interface with other GaAs I/O products such as the FURY Series of gate arrays for ultra high speed chip to chip communication. The inputs and outputs of the VS12G476 utilize I/O levels which are 'native' to E/D GaAs technology and are consistent with 50 transmission line circuit board environments.

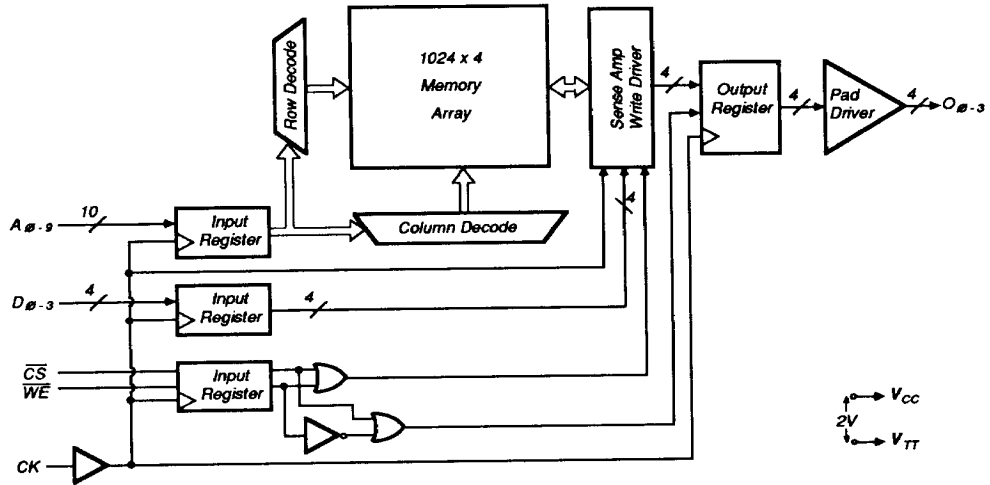
Memory cell selection is achieved through a 10-bit address designated  $A_0 - A_9$ . The address inputs, as well as the four data inputs, chip select and write enable are registered and

held at the rising edge of the clock input. During a read, data out is valid after the clock access time ( $t_{CO}$ ), and is registered and held into the next clock cycle, until the data change for the read cycle. During a write, data out is not driven. Data outputs are open source followers which provide maximum flexibility in a wired-OR application. The minimum cycle time for a read or write is 2.5 ns.

The VS12G476 is packaged in a 28-pin ceramic LDCC or LCC. Its high speed makes it ideal for new designs in cache memory, signal processing, and video applications where access time is the critical parameter. Its low sensitivity to total dose radiation makes it well-suited to the harsh environments encountered in military and aerospace applications.

The VS12G476 is fabricated in gallium arsenide using Vitesse's proprietary enhancement/depletion mode technology for high speed, low power operation.

# Block Diagram



## Truth Table

Inputs		Output	Mode
$\overline{CS}$	$\overline{WE}$		
H	X	L	Chip not selected, Output disabled
L	H	Data Out	Read
L	L	L	Write, Output disabled

H = HIGH Voltage L = LOW Voltage X = Don't Care (HIGH or LOW)

## Absolute Maximum Ratings <sup>(1)</sup>

Power Supply Voltage ( $V_{TT} = GND [V_{CC} - V_{TT}]$ ) <sup>(2)</sup>	4.0 V to -0.5 V
Power Supply Voltage ( $V_{CC} = GND [V_{TT} - V_{CC}]$ ) <sup>(3)</sup>	-4.0 V to 0.5 V
Input Voltage Applied, ( $V_{TT} = GND$ ) <sup>(2)</sup>	-0.5 V to $V_{CC} + 0.5$ V
Input Voltage Applied, ( $V_{CC} = GND$ ) <sup>(3)</sup>	0.5 V to $V_{TT} - 0.5$ V
Output Current, ( $I_{OUT}$ )	30 mA
Maximum Junction Temperature, ( $T_j$ )	150 C
Case Temperature Under Bias, ( $T_C$ )	-55 to +125 C
Storage Temperature, ( $T_{STG}$ ) <sup>(4)</sup>	-65 to +150 C

## Recommended Operating Conditions

Power Supply Voltage ( $V_{TT} = GND$ ) <sup>(2)</sup>	2.2 V to 1.8 V
Power Supply Voltage ( $V_{CC} = GND$ ) <sup>(3)</sup>	-2.2 V to -1.8 V
Operating Temperature Range <sup>(4)</sup>	0 to +70 C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) For operation in a +2 V GaAs circuit board environment.

(3) For operation in a -2 V ECL circuit board environment.

(4) Lower limit of specification is ambient temperature and upper limit is case temperature.

## DC Characteristics

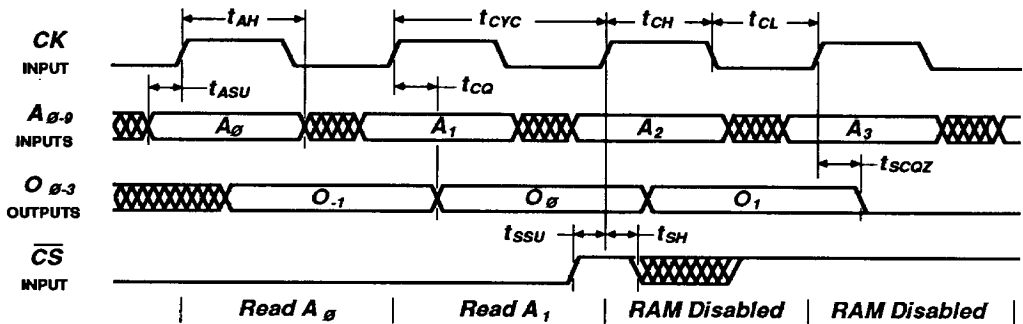
(Over recommended operating conditions Outputs terminated to  $V_{TT}$  through 50 .)

Parameters	Description	Min	Max	Units
$V_{OH}$	Output HIGH voltage	$V_{TT} + 700$	$V_{TT} + 1100$	mV
$V_{OL}$	Output LOW voltage	$V_{TT}$	$V_{TT} + 100$	mV
$V_{IH}$	Input HIGH voltage	$V_{TT} + 800$	$V_{TT} + 1200$	mV
$V_{IL}$	Input LOW voltage	$V_{TT} - 400$	$V_{TT} + 200$	mV
$I_{TT}, I_{CC}^{(1)}$	Power supply current	—	500	mA

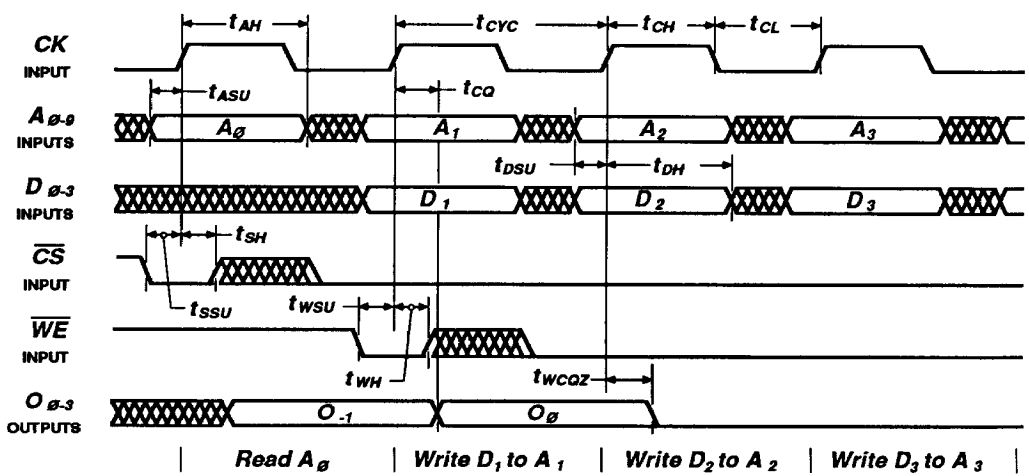
## AC Characteristics<sup>(2)</sup>

(Over recommended operating conditions; Outputs terminated to  $V_{TT}$  through 50 .)

### 1. Read Mode:



### 2. Write Mode:



= DONT CARE

NOTES: (1) The power supply can be configured in two ways: a)  $V_{CC} = 0\text{ V (GND)}$ ,  $V_{TT} = -2\text{ V}$ , or b)  $V_{CC} = +2\text{ V}$ ,  $V_{TT} = 0\text{ V (GND)}$ .

(2) Input edge rates are 500 ps or less. Timing is referenced to  $V_{TT} + 400\text{ mV}$  on inputs and outputs. Outputs terminated to 50 to  $V_{TT}$  and loaded by 30 pF.

**AC Characteristics (continued) <sup>(1)</sup>**(Over recommended operating conditions; Outputs terminated to  $V_{TT}$  through 50 ohms.)

Parameters	Description	Min	Max	Units
$t_{ASU}$	Address setup time	—	0.7	ns
$t_{DSU}$	Data in setup time	—	0.7	ns
$t_{SSU}$	$\overline{CS}$ setup time	—	0.7	ns
$t_{WSU}$	$\overline{WE}$ setup time	—	0.7	ns
$t_{AH}$	Address hold time	0	—	ns
$t_{DH}$	Data hold time	0	—	ns
$t_{SH}$	$\overline{CS}$ hold time	0	—	ns
$t_{WH}$	$\overline{WE}$ hold time	0	—	ns
$t_{CQ}$	Clock to output	0	1.0	ns
$t_{CYC}$	Clock cycle time (read, write)	2.5	—	ns
$t_{CH}$	Clock HIGH time	1.0	—	ns
$t_{CL}$	Clock LOW time	1.0	—	ns
$t_{SCQZ}$	Clock to output disable (result of rising $\overline{CS}$ input)	—	1.0	ns
$t_{WCQZ}$	Clock to output disable (result of falling $\overline{WE}$ input)	—	1.0	ns

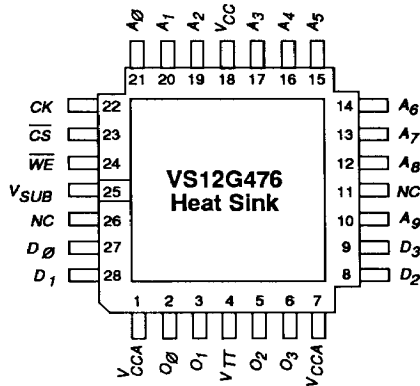
NOTES: (1) Input edge rates are 500 ps or less. Timing is referenced to  $V_{TT} + 400$  mV on inputs and outputs. Outputs terminated to 50  $\Omega$  to  $V_{TT}$  and loaded by 30 pF.

**Pin Description**

Pin #	Name	I/O	Description
10, 12-17, 19-21	$A_0 - A_2$	I	Address inputs
8, 9, 27, 28	$D_0 - D_3$	I	Data inputs
23	$\overline{CS}$	I	Chip select input (active LOW)
24	$\overline{WE}$	I	Write enable input (active LOW)
22	$\overline{CK}$	I	Clock input
2, 3, 5, 6	$O_0 - O_3$	O	Data outputs
18	VCC		Most positive power supply voltage <sup>(1)</sup>
4	VTT		Most negative power supply voltage <sup>(2)</sup>
25	VSUB		Substrate voltage, connect to $V_{TT}$
1, 7	VCCA		Output driver supply voltage
26, 11	NC		No connect, leave floating

NOTES: (1)  $V_{CC} = 0$  V in ECL environments; +2 V in GaAs environments.  
(2)  $V_{TT} = -2$  V in ECL environments; 0 V in GaAs environments.

**Connection Diagram (28-pin LCC - Top View)**



**Connection Diagram (28-pin LDCC - Top View)**

