LH1538

128-output LCD Common Driver IC

DESCRIPTION

The LH1538 is a 128-output common driver IC suitable for driving large/medium scale dot matrix LCD panels with low voltage segment drive method, and is used in personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of LCD module. When combined with the LH1581 segment driver, it can create a low power consuming, high-resolution LCD.

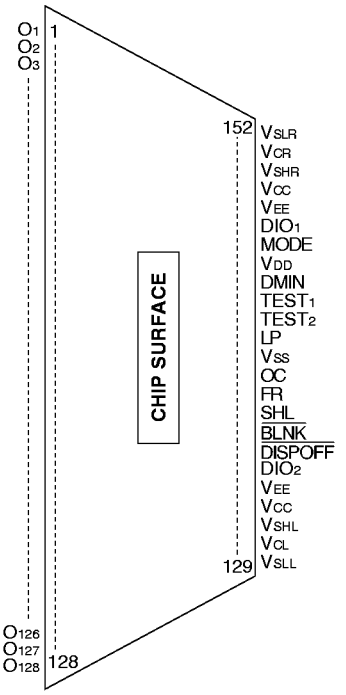
FEATURES

- Selectable number of LCD drive outputs : 128/120
- Supply voltage for LCD drive : +30.0 to +80.0 V
- Supply voltage for the logic system : +2.5 to +5.5 V
- Shift clock frequency
  - 4 MHz (MAX.) : V_{DD} = +5.0±0.5 V
  - 3 MHz (MAX.) : V_{DD} = +2.5 to +4.5 V
- Low power consumption
- Low output impedance
- Level of LCD drive outputs : 3
- Controllable input signal directly from controller
- Built-in control function for blanking period
- Built-in 128-bit bi-directional shift register (divisible into 64 bits x 2)
- Available in a single mode (128-bit shift register or 120-bit shift register) or in a dual mode (64-bit shift register x 2 or 60-bit shift register x 2)
  - ① $O_1 \rightarrow O_{128}$ ($O_5 \rightarrow O_{124}$) Single mode
  - ② $O_{128} \rightarrow O_1$ ($O_{124} \rightarrow O_5$) Single mode
  - ③ $O_1 \rightarrow O_{64}$, $O_{65} \rightarrow O_{128}$ ($O_5 \rightarrow O_{64}$, $O_{65} \rightarrow O_{124}$) Dual mode
  - ④ $O_{128} \rightarrow O_{65}$, $O_{64} \rightarrow O_1$ ($O_{124} \rightarrow O_{65}$, $O_{64} \rightarrow O_5$) Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when $\overline{DISPOFF}$ active
- Package : 152-pin TCP (Tape Carrier Package)

PIN CONNECTIONS

152-PIN TCP TOP VIEW

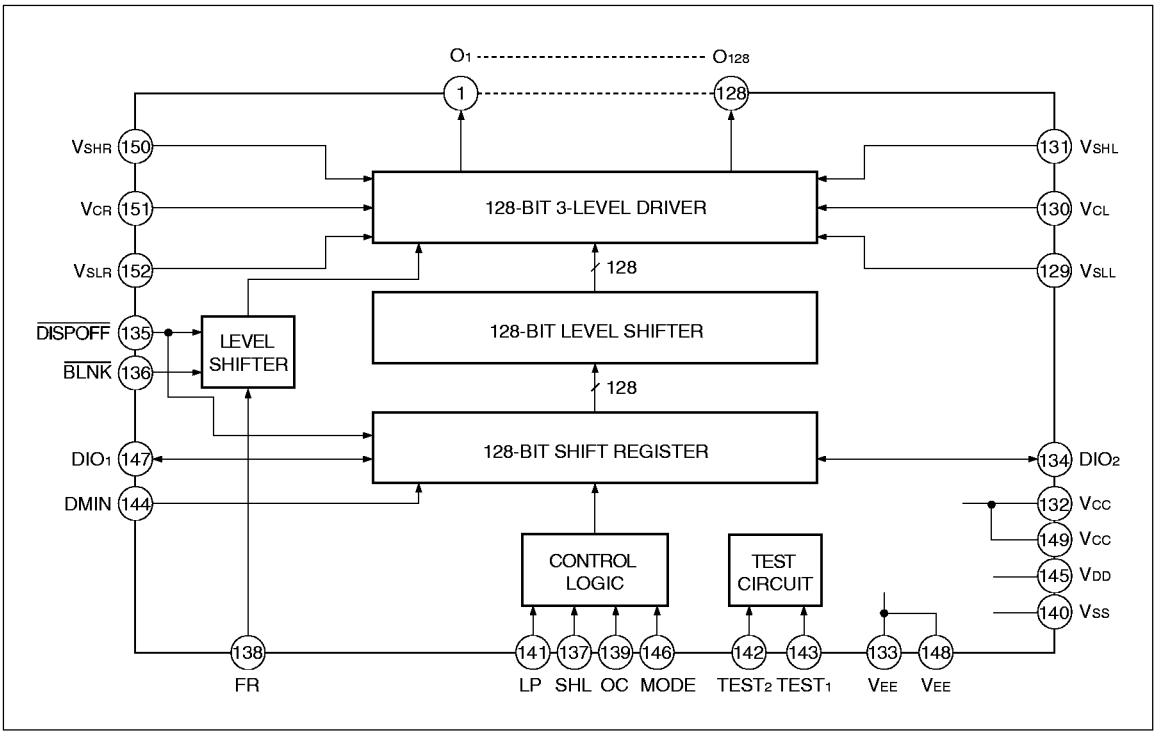


NOTE :
Doesn't prescribe TCP outline.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1 to 128	O_1-O_{128}	O	LCD drive output
129, 152	V_{SLL}, V_{SLR}	–	Power supply for LCD drive
130, 151	V_{CL}, V_{CR}	–	Power supply for LCD drive
131, 150	V_{SHL}, V_{SHR}	–	Power supply for LCD drive
132, 149	V_{CC}	–	Power supply for LCD drive
133, 148	V_{EE}	–	Power supply for LCD drive
134, 147	DIO_2, DIO_1	I/O	Shift data input/output for shift register
135	$\overline{DISPOFF}$	I	Control input for output of non-select level
136	$\overline{BLNK}$	I	Control input for blanking period
137	SHL	I	Input for selecting the shift direction of shift register
138	FR	I	AC-converting signal input for LCD drive waveform
139	OC	I	Input for selecting the number of LCD drive outputs
140	V_{SS}	–	Ground (0 V)
141	LP	I	Shift clock input for shift register
142, 143	$TEST_2$, $TEST_1$	I	Test mode selection input
144	DMIN	I	Dual mode data input
145	V_{DD}	–	Power supply for logic system (+2.5 to +5.5 V)
146	MODE	I	Mode selection input

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Shifts data from the data input pin at the falling edge of the LP signal, based on the data shift direction and mode setting received from the control logic block.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
3-Level Driver	Drives the LCD drive output pins from the shift register data, and selects one of 3 levels (V_{SH}, V_C or V_{SL}) based on the FR, $\overline{DISPOFF}$ and $\overline{BLNK}$ signals.
Control Logic	Controls the shift register's direction of data shift, mode setting and number of LCD drive outputs in response to SHL, MODE and OC signal inputs.
Test Circuit	The circuit for testing. During normal operation, it isn't activated.

INPUT/OUTPUT CIRCUITS

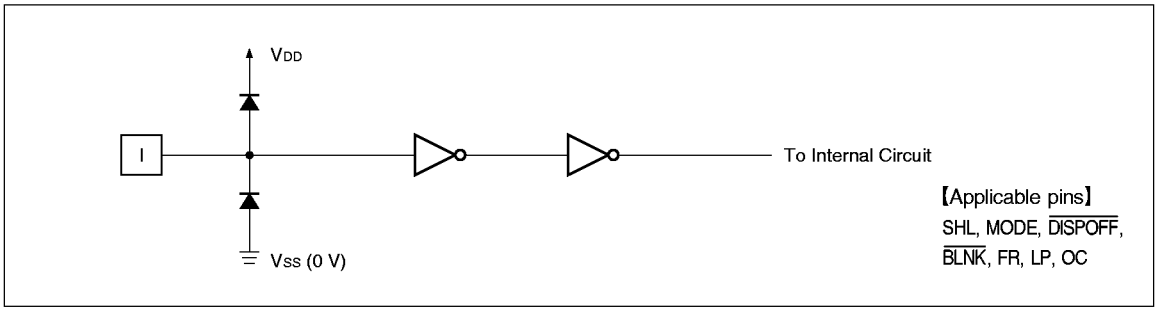


Fig. 1 Input Circuit (1)

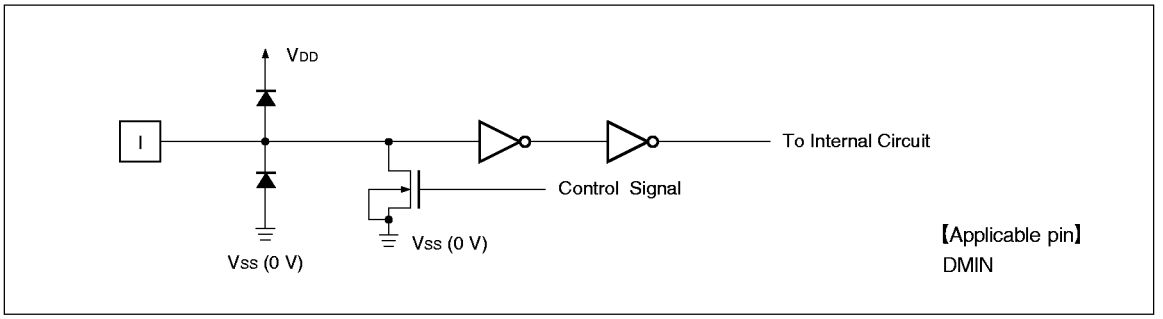


Fig. 2 Input Circuit (2)

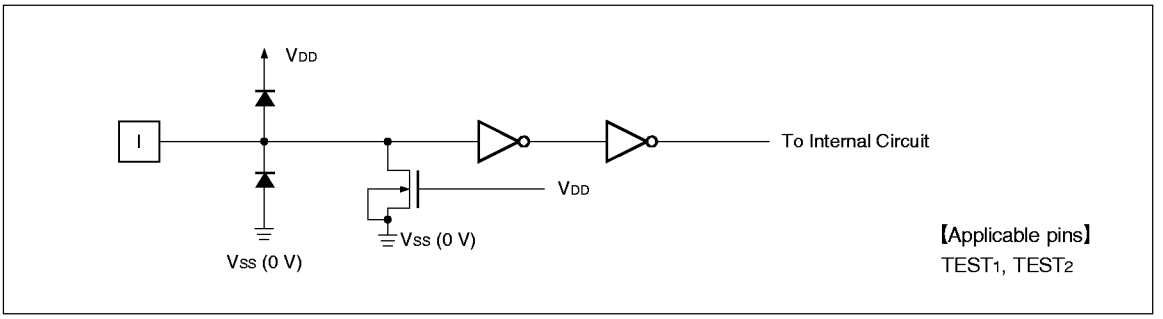


Fig. 3 Input Circuit (3)

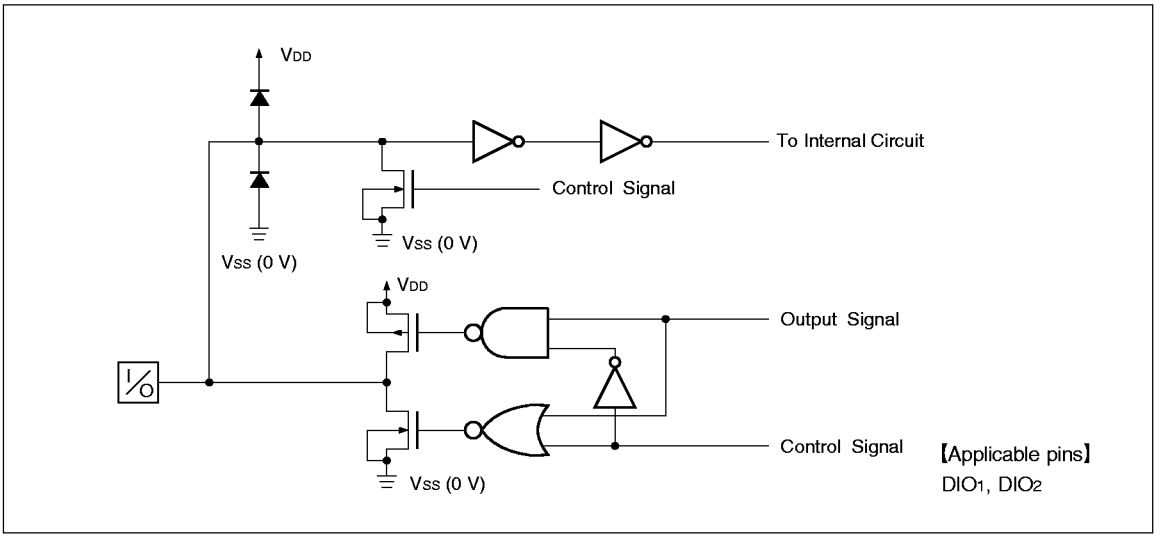


Fig. 4 Input/Output Circuit

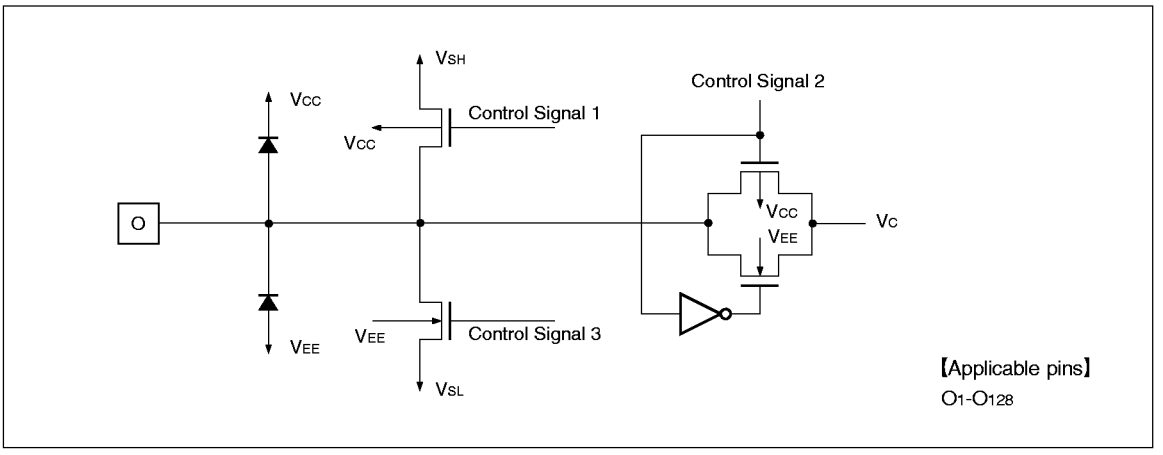


Fig. 5 LCD Drive Output Circuit

FUNCTIONAL DESCRIPTION

Pin Functions

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Logic system power supply pin, connected to 0 V.
V_{EE}	Power supply pin for LCD drive
V_{CC}	Power supply pin for LCD drive
V_{SHL}, V_{SHR} V_{CL}, V_{CR} V_{SLL}, V_{SLR}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{EE} \leq V_{SL} < V_C < V_{SH} \leq V_{CC}$. • V_{iL} and V_{iR} (i = SH, C, SL) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
DIO_1	Shift data input/output pin for bi-directional shift register • Input pin when SHL = L, output pin when SHL = H. When SHL = L, DIO_1 is used as input pin, it will be pulled down. When SHL = H, DIO_1 is used as output pin, it won't be pulled down. • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.
DIO_2	Shift data input/output pin for bi-directional shift register • Input pin when SHL = H, output pin when SHL = L. When SHL = H, DIO_2 is used as input pin, it will be pulled down. When SHL = L, DIO_2 is used as output pin, it won't be pulled down. • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse.
SHL	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from O_1 to O_{128} when set to V_{SS} level "L", and data is shifted from O_{128} to O_1 when set to V_{DD} level "H". • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.
OC	Input pin for selecting the number of LCD drive outputs • Selectable 128-output mode or 120-output mode. • When set to V_{SS} level "L", 120-output mode is selected; when set to V_{DD} level "H", 128-output mode is selected. • When 120-output mode, output pins which aren't used (O_1 to O_4, O_{125} to O_{128}) output the non-select level V_C. • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.

SYMBOL	FUNCTION
$\overline{DISPOFF}$	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (O_1-O_{128}) are set to level V_C. • When set to "L", the contents of the shift register are reset to not reading data. When the $\overline{DISPOFF}$ function is canceled, the driver outputs non-select level (V_C), and the shift data is read at the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
$\overline{BLNK}$	Control input pin for blanking period • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", blanking period mode is selected, the LCD drive output pins (O_1 to O128) are set to level V_C. At this time shift registers are active (not reset).
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MODE	Mode selection pin • When set to V_{SS} level "L", single mode is selected; when set to V_{DD} level "H", dual mode is selected. • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.
DMIN	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 65th bit. When the chip is used in dual mode, DMIN will be pulled down. When the chip is used in single mode, DMIN won't be pulled down. • Refer to "RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION" in Functional Operations.
$TEST_1$ $TEST_2$	Test mode selection pins • During normal operation, fix to V_{SS} level "L".
O_1-O_{128}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_{SH}, V_C or V_{SL}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

Functional Operations

TRUTH TABLE

FR	LATCH DATA	$\overline{\text{DISPOFF}}$	$\overline{\text{BLNK}}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (O_1-O_{128})
L	L	H	H	V_C
L	H	H	H	V_{SH}
H	L	H	H	V_C
H	H	H	H	V_{SL}
X	X	H	L	V_C
X	X	L	X	V_C

NOTES :

- $V_{EE} \leq V_{SL} < V_C < V_{SH} \leq V_{CC}$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.
  Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DATA I/O PINS AND DATA TRANSFER DIRECTION

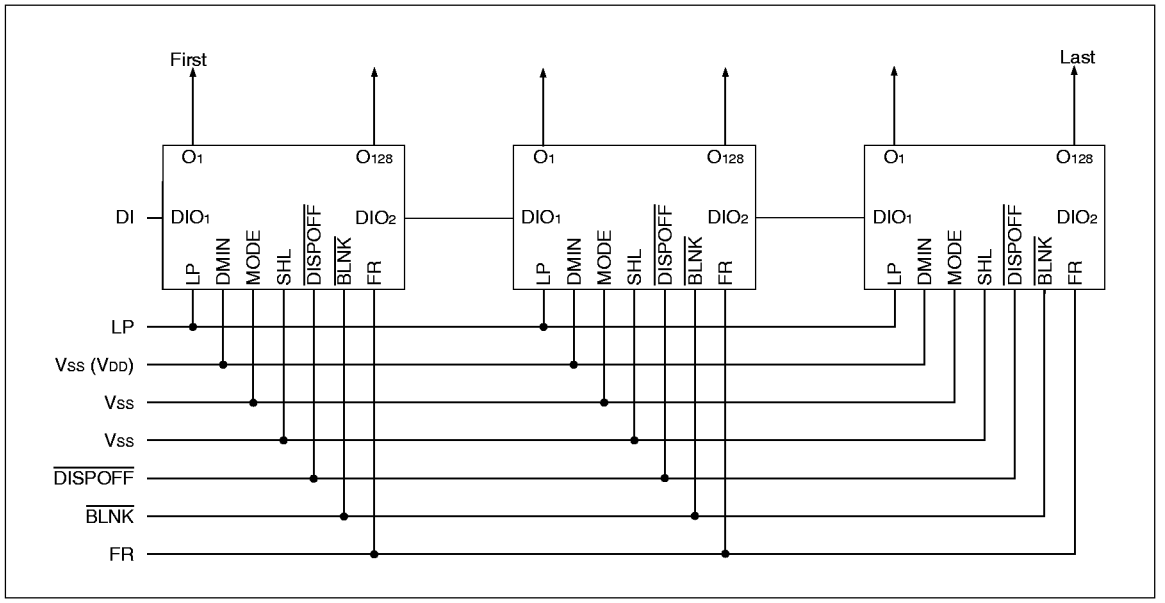
OC	MODE	SHL	DATA TRANSFER DIRECTION	DIO_1	DIO_2	DMIN
L (120 outputs)	L (Single)	L	$O_5 \rightarrow O_{124}$	INPUT	OUTPUT	X
		H	$O_{124} \rightarrow O_5$	OUTPUT	INPUT	X
	H (Dual)	L	$O_5 \rightarrow O_{64}$ $O_{65} \rightarrow O_{124}$	INPUT	OUTPUT	INPUT
		H	$O_{124} \rightarrow O_{65}$ $O_{64} \rightarrow O_5$	OUTPUT	INPUT	INPUT
H (128 outputs)	L (Single)	L	$O_1 \rightarrow O_{128}$	INPUT	OUTPUT	X
		H	$O_{128} \rightarrow O_1$	OUTPUT	INPUT	X
	H (Dual)	L	$O_1 \rightarrow O_{64}$ $O_{65} \rightarrow O_{128}$	INPUT	OUTPUT	INPUT
		H	$O_{128} \rightarrow O_{65}$ $O_{64} \rightarrow O_1$	OUTPUT	INPUT	INPUT

NOTES :

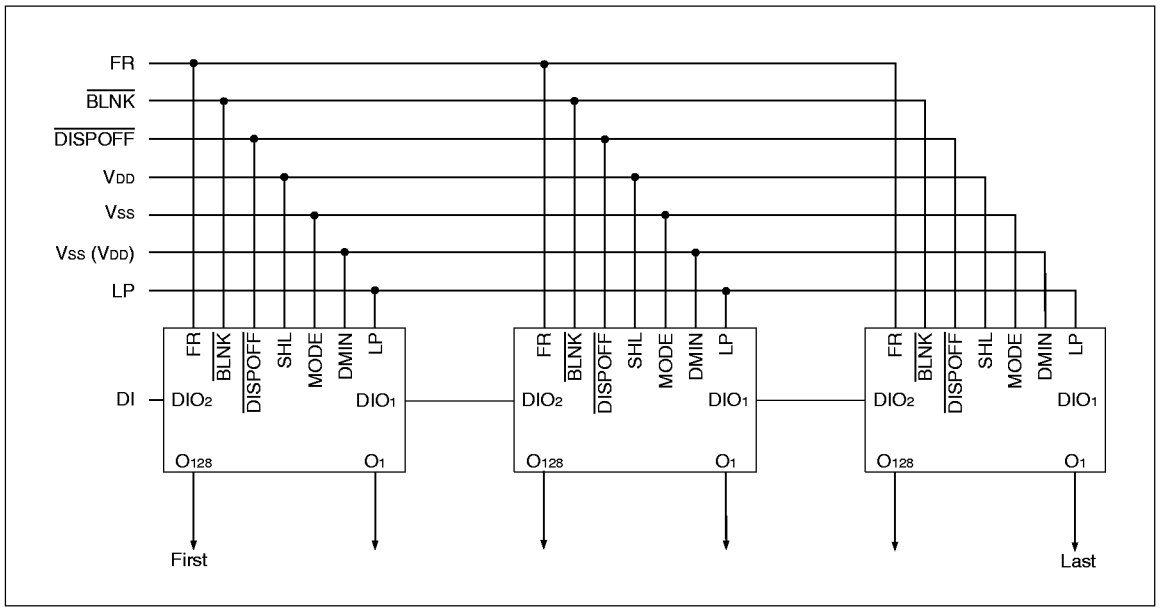
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

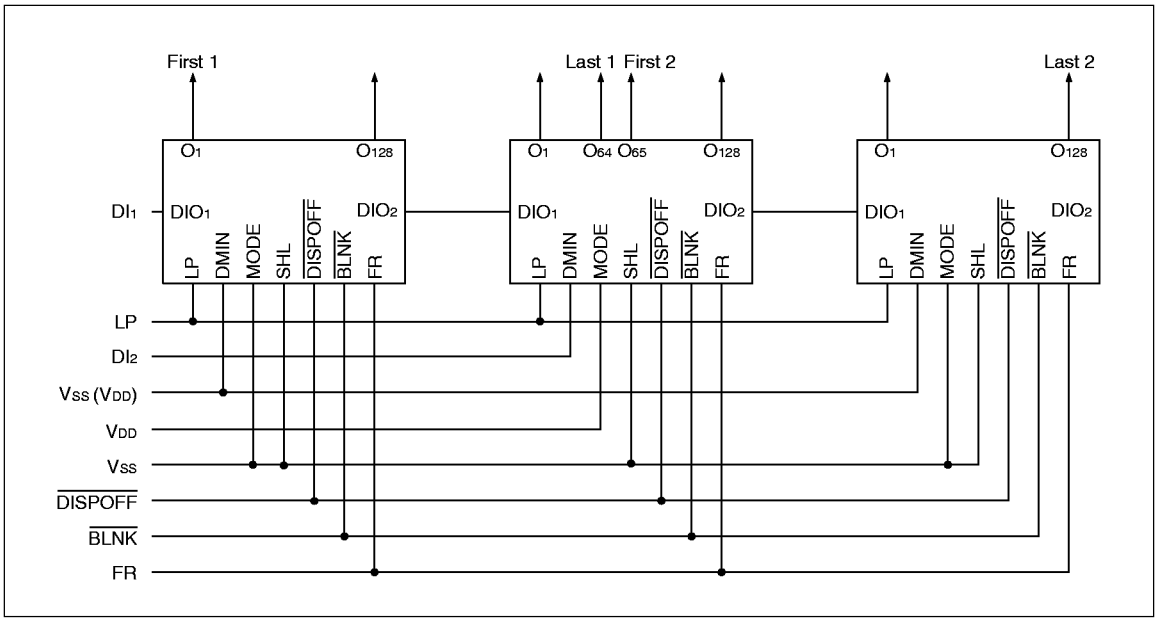
(a) Single Mode (SHL = "L")



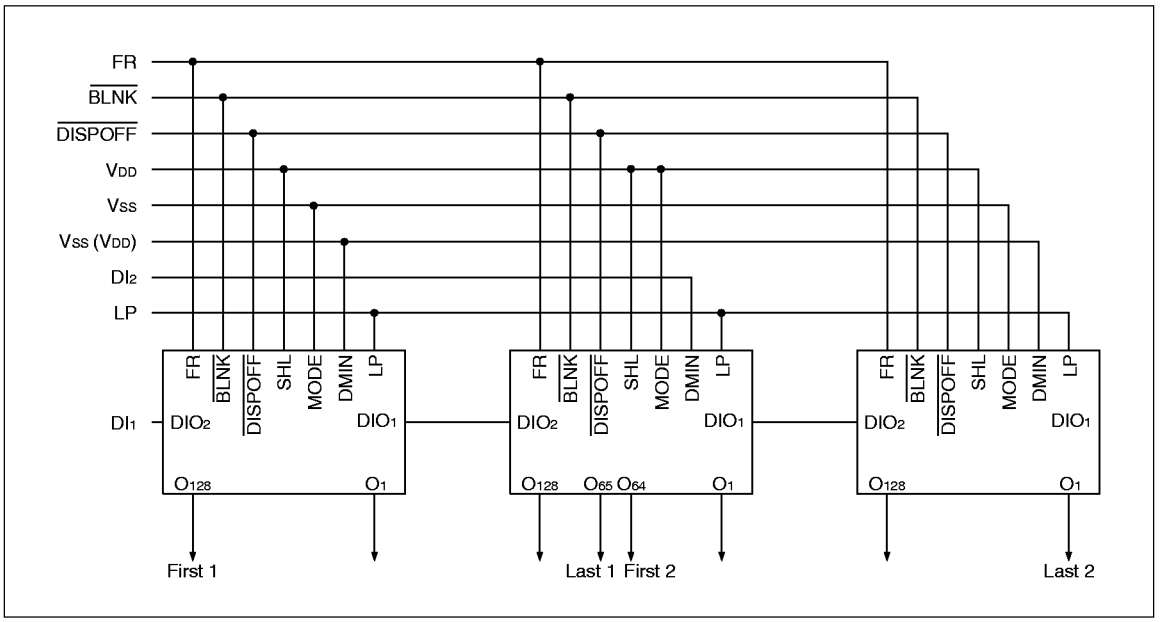
(b) Single Mode (SHL = "H")



(c) Dual Mode (SHL = "L")



(d) Dual Mode (SHL = "H")



PRECAUTIONS

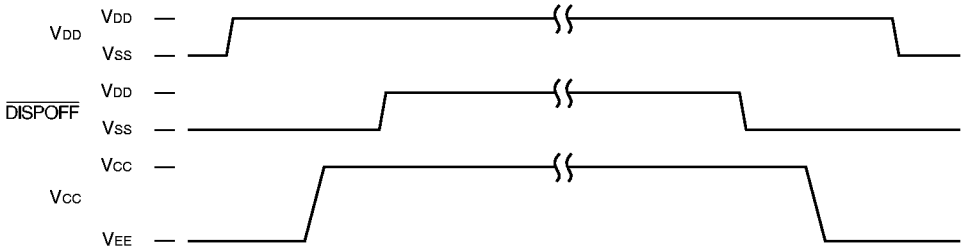
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_{CC} of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_C on $\overline{DISPOFF}$ function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	V_{EE} – 0.3 to V_{EE} + 47.0	V	1, 2
	V_{SS}	V_{SS}	V_{EE} – 0.3 to V_{EE} + 47.0	V	
	V_{DD} – V_{SS}	V_{DD}, V_{SS}	–0.3 to +7.0	V	1
Supply voltage (2)	V_{CC}	V_{CC}	V_{EE} – 0.3 to V_{EE} + 85.0	V	1, 2
	V_{SH}	V_{SHL}, V_{SHR}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
	V_C	V_{CL}, V_{CR}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
	V_{SL}	V_{SLL}, V_{SLR}	V_{EE} – 0.3 to V_{CC} + 0.3	V	
Input voltage	V_I	DIO_1, DIO_2, DMIN, SHL, MODE, LP, FR, OC, $\overline{DISPOFF}$, $\overline{BLNK}$, $TEST_1$, $TEST_2$	V_{SS} –0.3 to V_{DD} + 0.3	V	1
Storage temperature	T_{STG}		–45 to +125	°C	

NOTES :

1. T_A = +25 °C
2. The maximum applicable voltage on any pin with respect to V_{EE}.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	V_{SS} + 2.5		V_{SS} + 5.5	V	1, 2
Supply voltage (2)	V_{CC}	V_{CC}	V_{SS} + 17.5		V_{SS} + 42.5	V	
Supply voltage (3)	V_{EE}	V_{EE}	V_{SS} – 37.5		V_{SS} – 12.5	V	
Operating temperature	T_{OPR}		–20		+85	°C	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{EE} \leq V_{SL} < V_C < V_{SH} \leq V_{CC}$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_{CC} – V_{EE} = +30.0 to +80.0 V, T_{OPR} = –20 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DIO_1, DIO_2, DMIN, SHL, MODE, LP, FR, OC, $\overline{DISPOFF}$, $\overline{BLNK}$			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	DIO_1, DIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = –0.4 mA		V_{DD} – 0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DIO_1, DIO_2, DMIN, SHL, MODE, LP, FR, OC, $\overline{DISPOFF}$, $\overline{BLNK}$			–10.0	µA	
	I_{LIH}	V_I = V_{DD}	SHL, MODE, LP, FR, OC, $\overline{DISPOFF}$, $\overline{BLNK}$			+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DIO_1, DIO_2, DMIN			100.0	µA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ = 0.5 V	O_1-O_{128}		0.6	1.0	kΩ	1
Standby current (1)	I_{STB1}		V_{DD}			50	µA	2
Standby current (2)	I_{STB2}		V_{CC}			50	µA	2
Supply current (1)	I_{DD}		V_{DD}			80	µA	3
Supply current (2)	I_{CC}		V_{CC}			120	µA	3

NOTES :

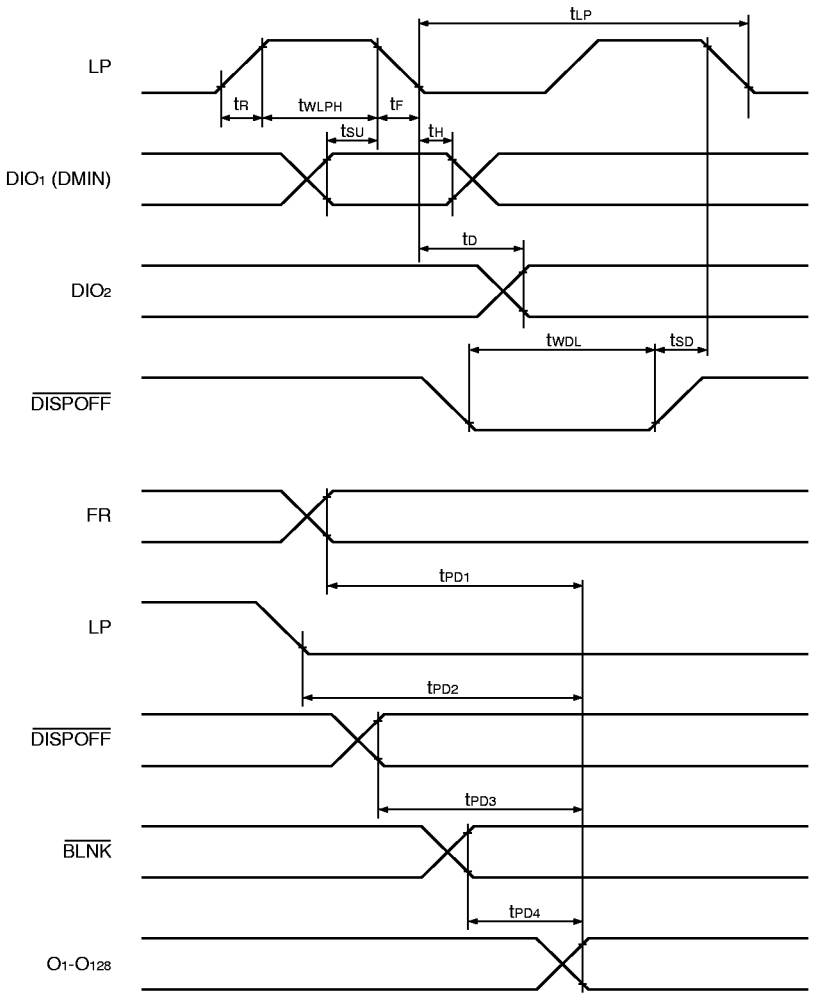
1. V_{CC} = V_{SH} = +32.5 V, V_C = +2.5 V, V_{EE} = V_{SL} = –27.5 V, V_{DD} = +5.0 V.
2. V_{CC} = V_{SH} = +42.5 V, V_C = +2.5 V, V_{EE} = V_{SL} = –37.5 V, V_{DD} = +5.0 V, V_I = V_{SS}.
3. V_{CC} = V_{SH} = +42.5 V, V_C = +2.5 V, V_{EE} = V_{SL} = –37.5 V, V_{DD} = +5.0 V, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_{CC} – V_{EE} = +30.0 to +80.0 V, T_{OPR} = –20 to +85 °C)

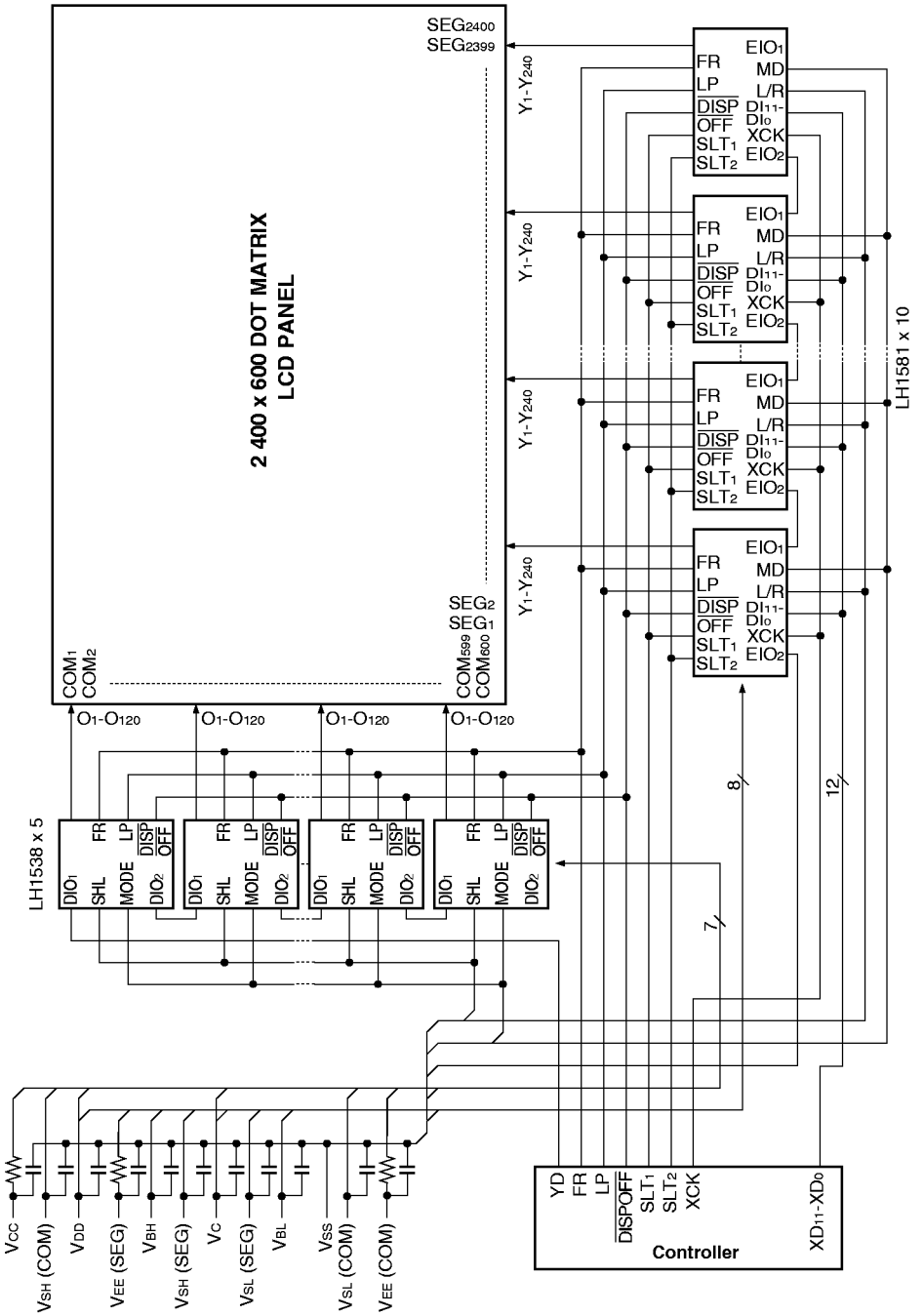
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{LP}	V_{DD} = +5.0±0.5 V	250			ns
		V_{DD} = +2.5 to +4.5 V	330			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0±0.5 V	30			ns
		V_{DD} = +2.5 to +4.5 V	60			ns
Data setup time	t_{SU}		50			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		120			ns
$\overline{\text{DISPOFF}}$ "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_D	C_L = 15 pF V_{DD} = +5.0±0.5 V			170	ns
		C_L = 15 pF V_{DD} = +2.5 to +4.5 V			250	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L = 15 pF V_{DD} = +5.0±0.5 V			0.7	µs
		C_L = 15 pF V_{DD} = +2.7 to +4.5 V			1.2	
		C_L = 15 pF V_{DD} = +2.5 to +2.7 V			2.5	
Output delay time (3)	t_{PD3}	C_L = 15 pF V_{DD} = +5.0±0.5 V			0.7	µs
		C_L = 15 pF V_{DD} = +2.7 to +4.5 V			1.2	
		C_L = 15 pF V_{DD} = +2.5 to +2.7 V			2.5	
Output delay time (4)	t_{PD4}	C_L = 15 pF V_{DD} = +5.0±0.5 V			0.7	µs
		C_L = 15 pF V_{DD} = +2.7 to +4.5 V			1.2	
		C_L = 15 pF V_{DD} = +2.5 to +2.7 V			2.5	

Timing Chart



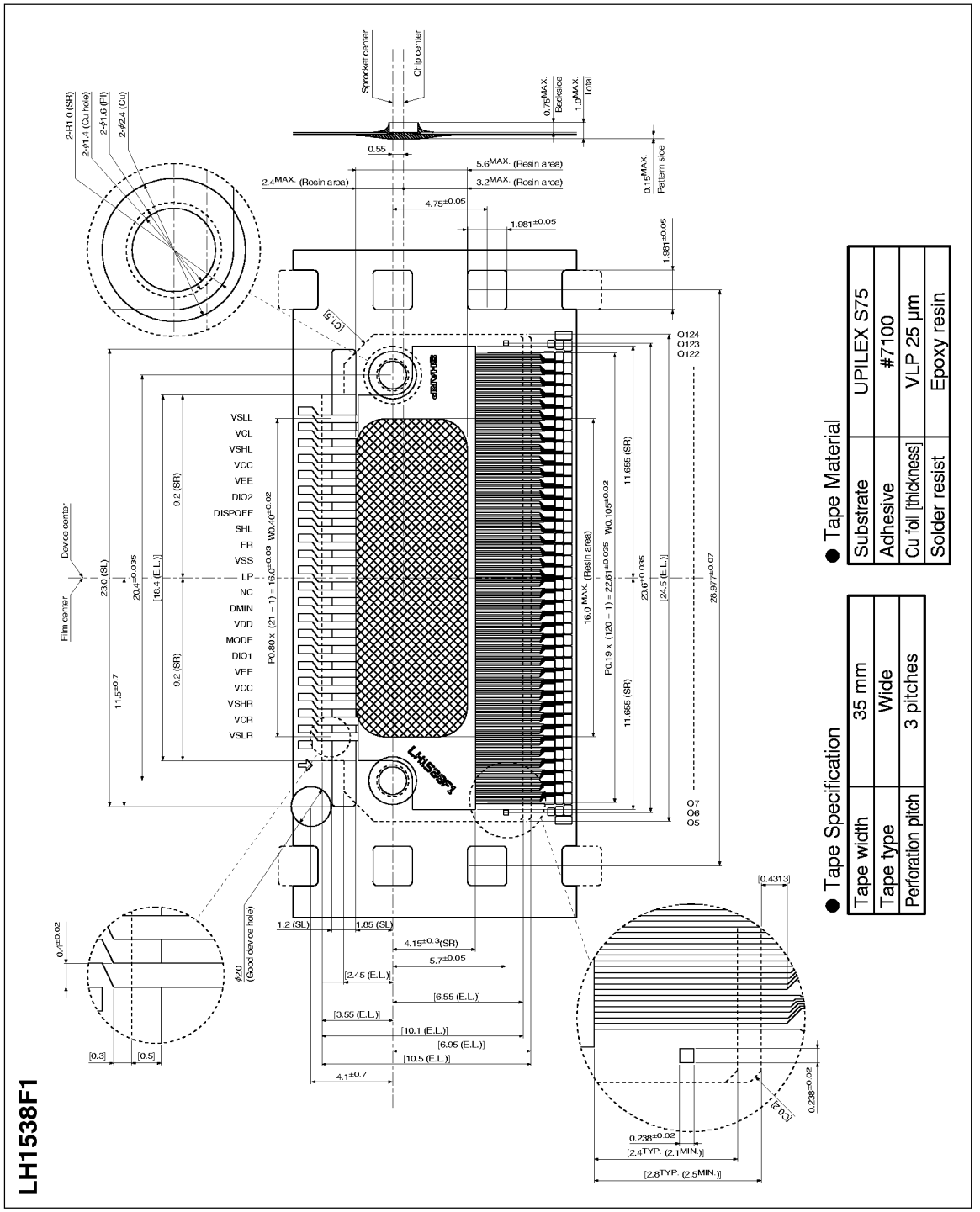
[SHL = "L"]

SYSTEM CONFIGURATION EXAMPLE



PACKAGES

(Unit : mm)



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	VLP 25 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	35 mm
Tape type	Wide
Perforation pitch	3 pitches

LH1538F1

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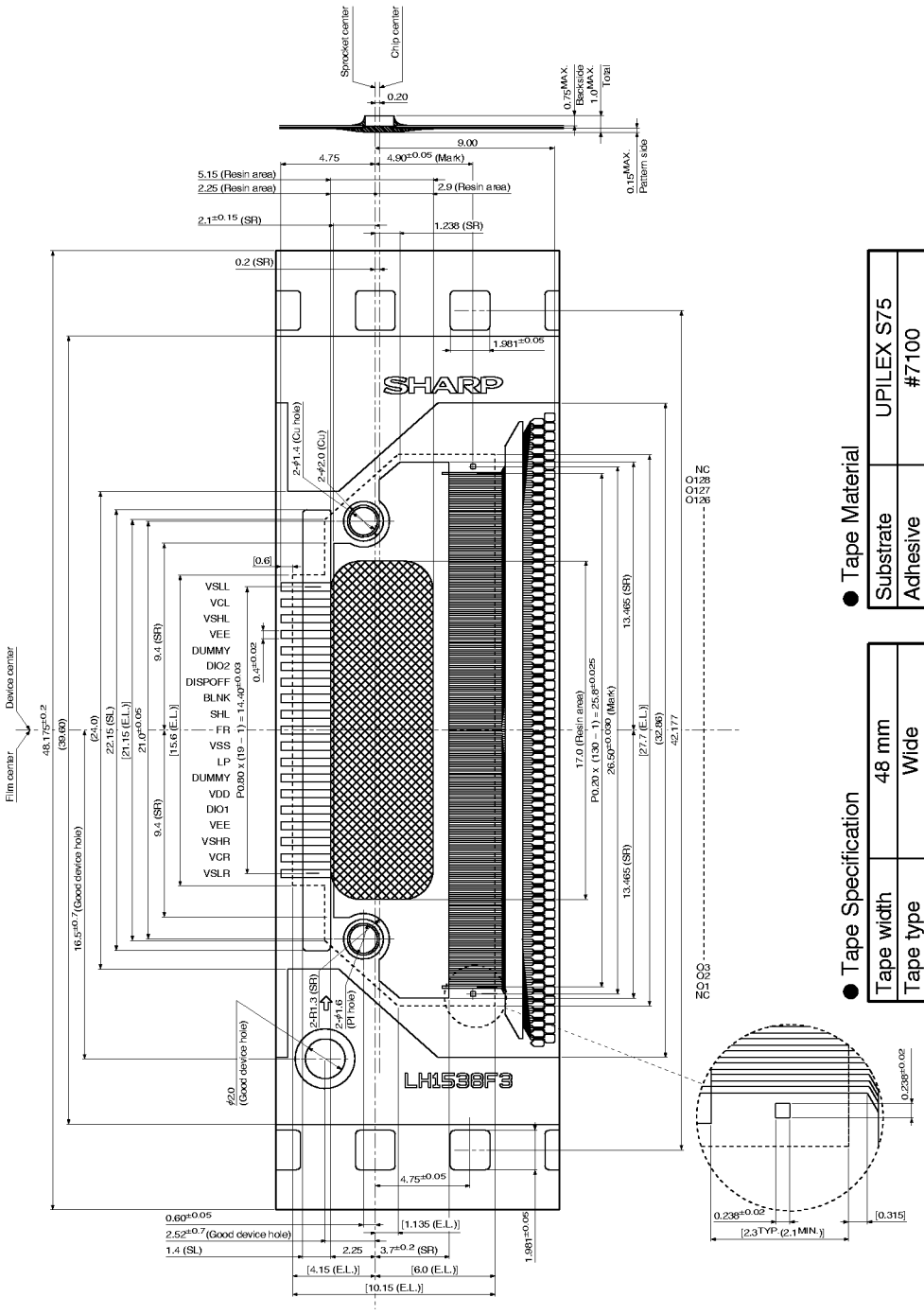
LH1538F3



● Tape Material

Substrate	UPILEX S75
Adhesive	#7100
Cu foil [thickness]	VLP 25 µm
Solder resist	Epoxy resin

● Tape Specification

Tape width	48 mm
Tape type	Wide
Perforation pitch	3 pitches