CYU01M16SFE
MoBL3™

16-Mbit (1M x 16) Pseudo Static RAM

Features

- **Wide voltage range: 1.7V–1.95V**
- **Access Time: 70 ns**
- **Ultra-low active power**
  - **Typical active current: 3 mA @ f = 1 MHz**
  - **Typical active current: 18 mA @ f = f_{max}**
- **Ultra low standby power**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in 48-ball BGA package**
- **Operating Temperature: –40°C to +85°C**

Functional Description[1]

The CYU01M16SFE is a high-performance CMOS Pseudo Static RAM organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. Refer to the truth table for a complete description of read and write modes.
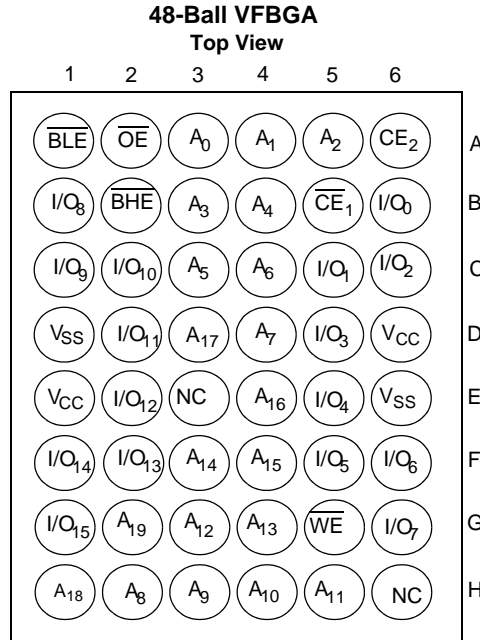
Logic Block Diagram
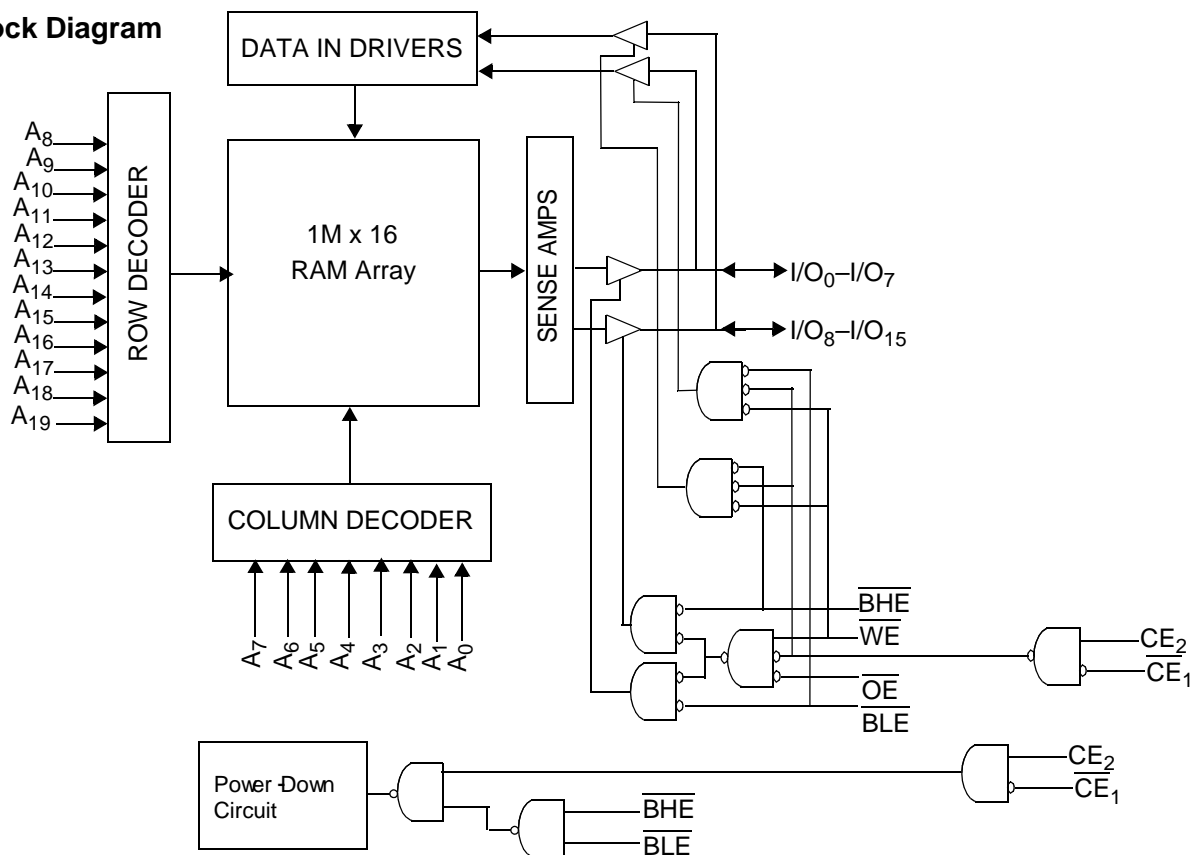
Note:
1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

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Pin Configuration[2, 3]

48-Ball VFBGA
Top View

Product Portfolio[4]

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1MHz		f = f_{max}			
CYU01M16SFE	Min.	Typ.[4]	Max.		Typ.[4]	Max.	Typ.[4]	Max.	Typ.[4]	Max.
	1.7	1.8	1.95	70	3	5	18	20	55	70

Power-up Characteristics

The initialization sequence is shown in the figure below. Chip Select should be $\overline{CE}_1$ HIGH or CE_2 LOW for at least 200 μs after V_{CC} has reached a stable value. No access must be attempted during this period of 200 μs.
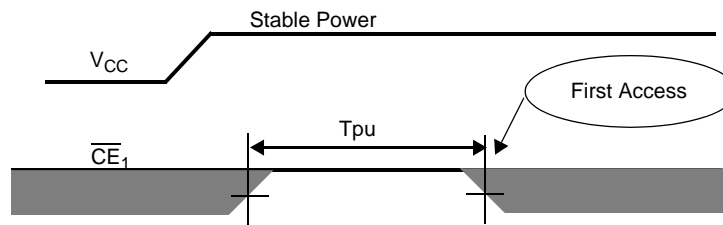
Parameter	Description	Min.	Typ.	Max.	Unit
Tpu	Chip Enable Low After Stable V_{CC}	200			μs

Notes:
2. Ball H6 and E3 can be used to upgrade to a 32-Mbit and a 64-Mbit density, respectively.
3. NC "no connect"-not connected internally to the die.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ (typ) and $T_A = 25°C$. Tested initially and after design changes that may affect the parameters.

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Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....−65°C to +150°C

Ambient Temperature with
Power Applied...−55°C to +125°C

Supply Voltage to Ground Potential .−0.2V to V_{CCMAX} + 0.3V

DC Voltage Applied to Outputs
in High Z State[5, 6, 7]........................−0.2V to V_{CCMAX} + 0.3V

DC Input Voltage[5, 6, 7]....................−0.2V to V_{CCMAX} + 0.3V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... > 200 mA

Device	Range	Operating Temperature (T_A)	V_{CC}
CYU01M16SFE	Industrial	−40°C to +85°C	1.7V to 1.95V

DC Electrical Characteristics (Over the Operating Range) [5, 6, 7]

Parameter	Description	Test Conditions		CYU01M16SFE-70 ns			Unit
				Min.	Typ.[4]	Max.	
V_{CC}	Supply Voltage			1.7	1.8	1.95	V
V_{OH}	Output HIGH Voltage	I_{OH} = −0.1 mA V_{CC}= 1.7V to 1.95V		V_{CC} − 0.2			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA V_{CC}= 1.7V to 1.95V				0.2	V
V_{IH}	Input HIGH Voltage	V_{CC}= 1.7V to 1.95V		0.8 * V_{CC}		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC}= 1.7V to 1.95V		−0.2		0.2 * V_{CC}	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}		−1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC}= V_{CCmax} I_{OUT} = 0 mA CMOS levels		18	20	mA
		f = 1 MHz			3	5	mA
I_{SB1}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} − 0.2V, CE_2 ≤ 0.2V, V_{IN} > V_{CC} − 0.2V, V_{IN} < 0.2V f = f_{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V_{CC} = 3.60V			55	70	µA
I_{SB2}	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} − 0.2V, CE_2 ≤ 0.2V V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = V_{CCMAX}			55	70	µA

Capacitance[8]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance[8]

Parameter	Description	Test Conditions	VFBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedence, per EIA/JESD51.	56	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		11	°C/W

Notes:
5. $V_{IL(MIN)}$ = −0.5V for pulse durations less than 20 ns.
6. $V_{IH(Max)}$ = V_{CC} + 0.5V for pulse durations less than 20 ns.
7. Overshoot and undershoot specifications are characterized and are not 100% tested.
8. Tested initially and after any design or process changes that may affect these parameters.

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AC Test Loads and Waveforms
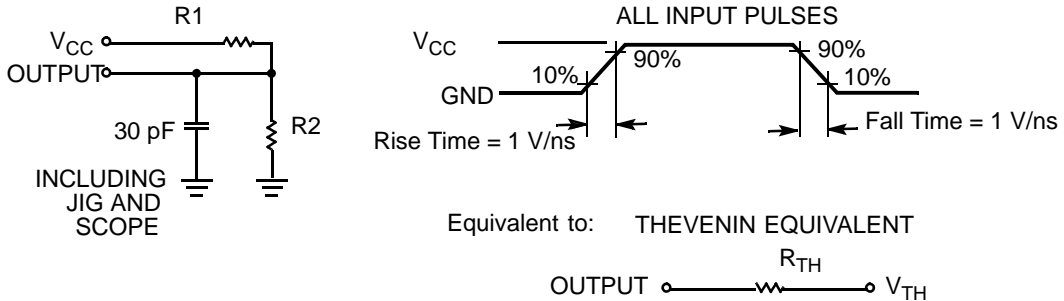
Parameters	1.8V (V_{CC})	Unit
R1	14000	Ω
R2	14000	Ω
R_{TH}	7000	Ω
V_{TH}	0.90	V

Switching Characteristics Over the Operating Range[9, 10, 11, 15, 14]

Parameter	Description	70 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}[13]	Read Cycle Time	70	40000	ns
t_{CD}	Chip Deselect Time $\overline{CE}_1$ = HIGH or CE_2 = LOW, BLE/BHE High Pulse Time	15		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10, 11, 12]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10, 11, 12]		25	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[10, 11, 12]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[10, 11, 12]		25	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[10, 11, 12]	5		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z[10, 11, 12]		25	ns

Notes:
9. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ.)}$/2, input pulse levels of 0V to V_{CC}, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
10. At any given temperature and voltage conditions t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device. All low-Z parameters will be measured with a load capacitance of 30 pF (3V).
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. High-Z and Low-Z parameters are characterized and are not 100% tested.
13. If invalid address signals shorter than min.tRC are continuously repeated for 40 μs, the device needs a normal read timing (t_{RC}) or needs to enter standby state at least once in every 40 μs.
14. In order to achieve 70-ns performance, the read access must be Chip Enable ($\overline{CE}_1$ or CE_2) controlled. That is, the addresses must be stable prior to Chip Enable going active.

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Switching Characteristics Over the Operating Range[9, 10, 11, 15, 14] (continued)

| Parameter	Description	70 ns Min.	70 ns Max.	Unit
Write Cycle[15]				
t_{WC}	Write Cycle Time	70	40000	ns
t_{SCE}	$\overline{CE_1}$ LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{CD}	Chip Deselect Time $\overline{CE_1}$ = HIGH or CE_2 = LOW, $\overline{BLE}/\overline{BHE}$ High Pulse Time	15		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	60		ns
t_{SD}	Data Set-Up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[10, 11, 12]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[10, 11, 12]	10		ns

Note:
15. The internal Write time of the memory is defined by the overlap of $\overline{WE}, \overline{CE_1}$ = V_{IL} or CE_2 = V_{IH}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

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Switching Waveforms
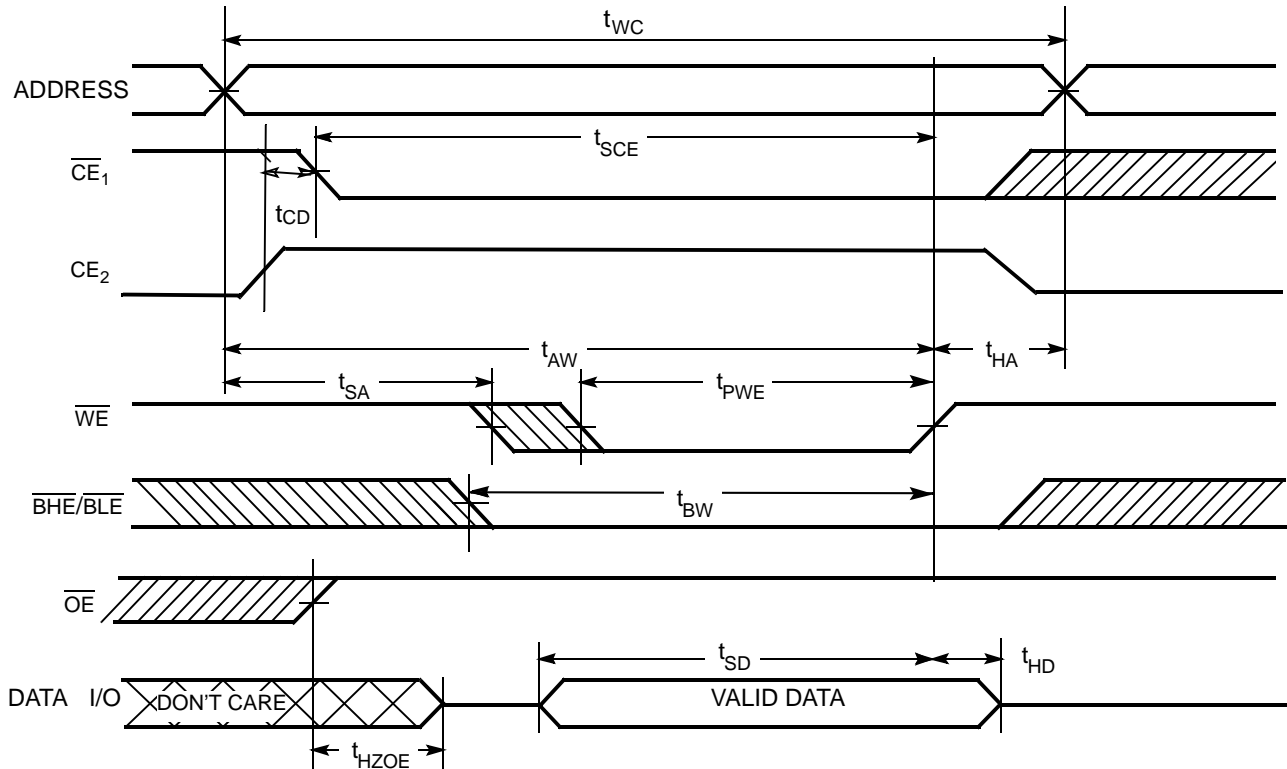
Read Cycle 1 (Address Transition Controlled)[17, 18]
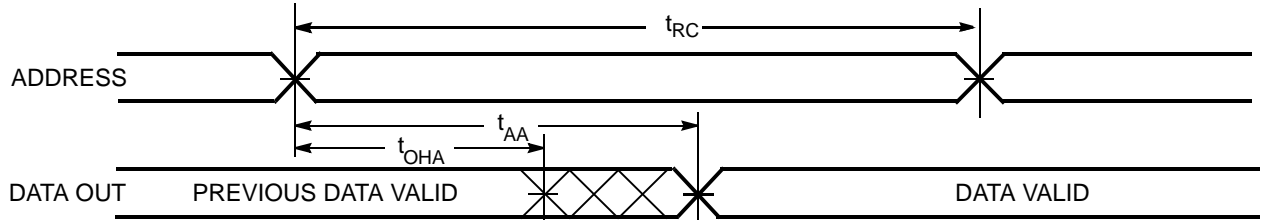
Read Cycle 2 ($\overline{OE}$ Controlled)[16, 18,19]
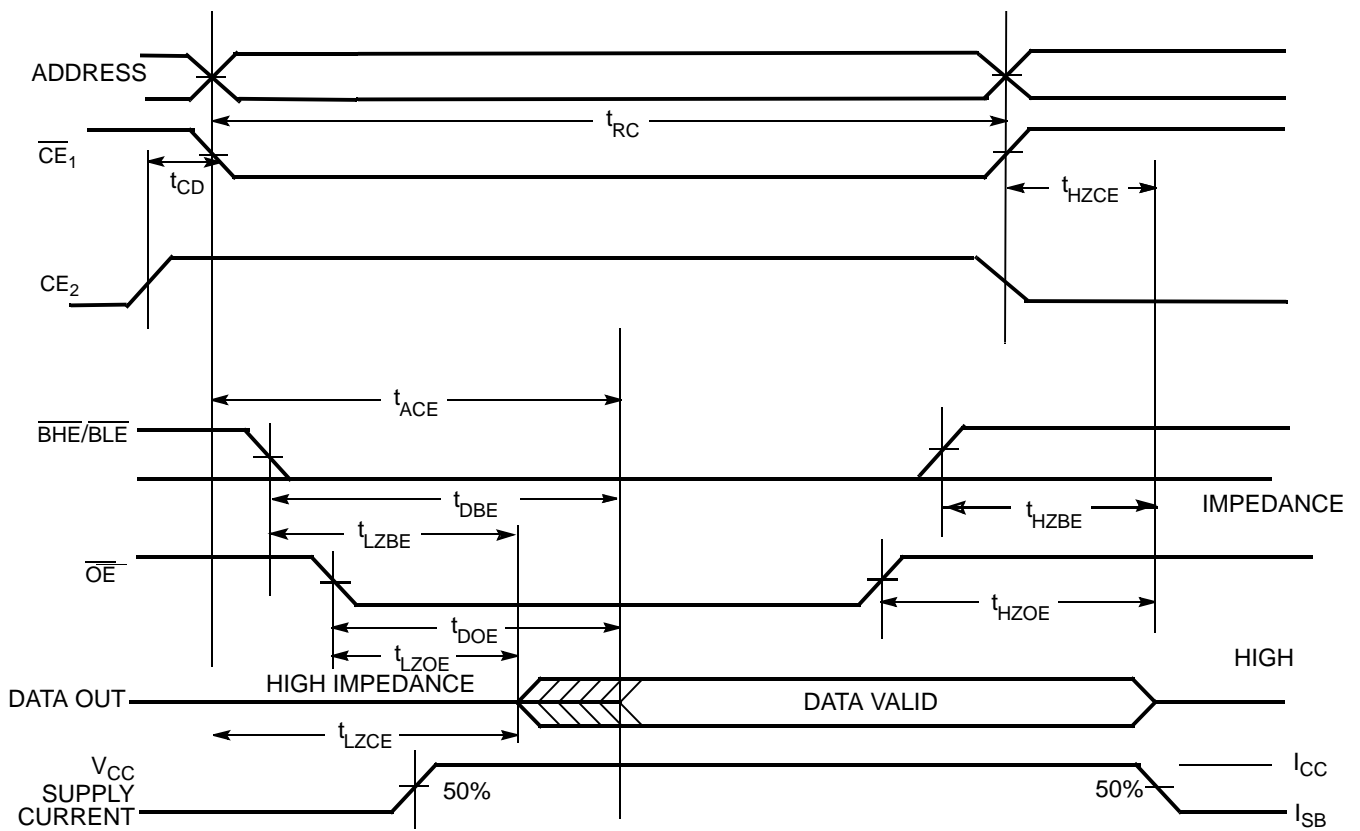
Notes:
16. Whenever $\overline{CE}_1$ = HIGH or CE_2 = LOW, $\overline{BHE}/\overline{BLE}$ are taken inactive, they must remain inactive for a minimum of 5 ns.
17. Device is continuously selected. $\overline{OE} = \overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$.
18. $\overline{WE}$ is HIGH for Read Cycle.
19. $\overline{CE}$ is the Logical AND of $\overline{CE}_1$ and CE_2.
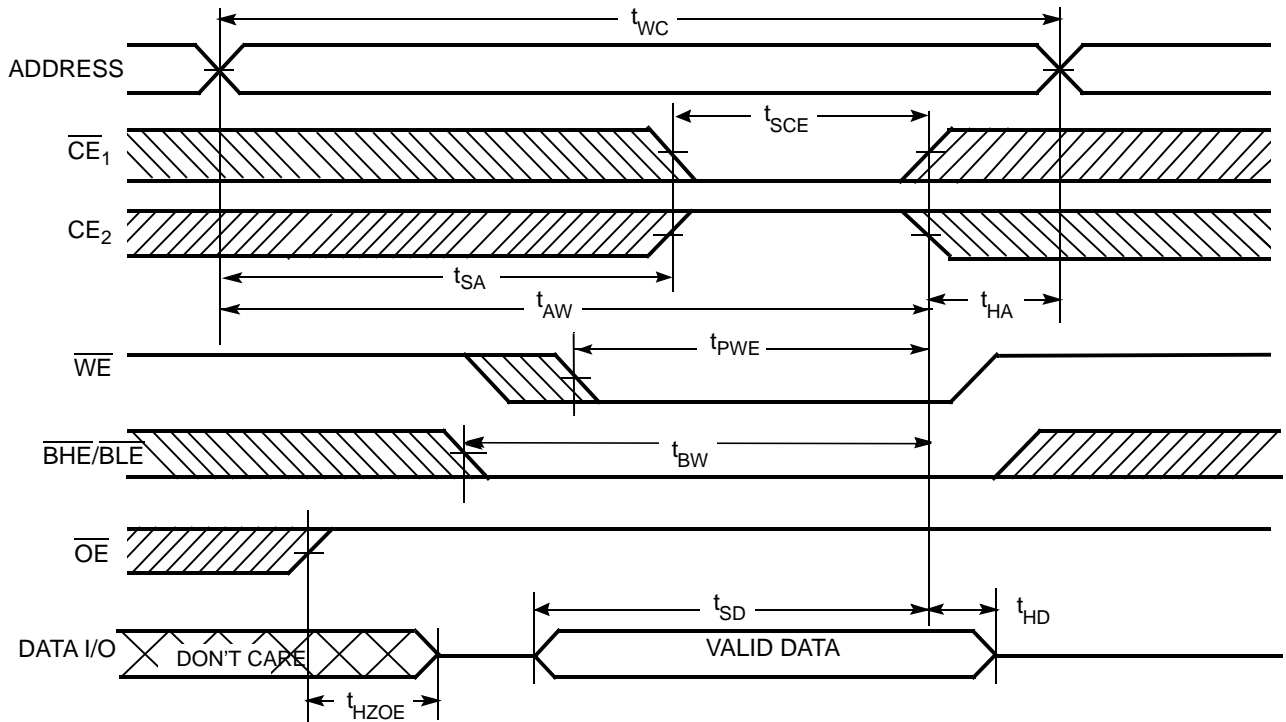
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Switching Waveforms (continued)

Notes:
20. Data I/O is high-impedance if $\overline{OE} \geq V_{IH}$.
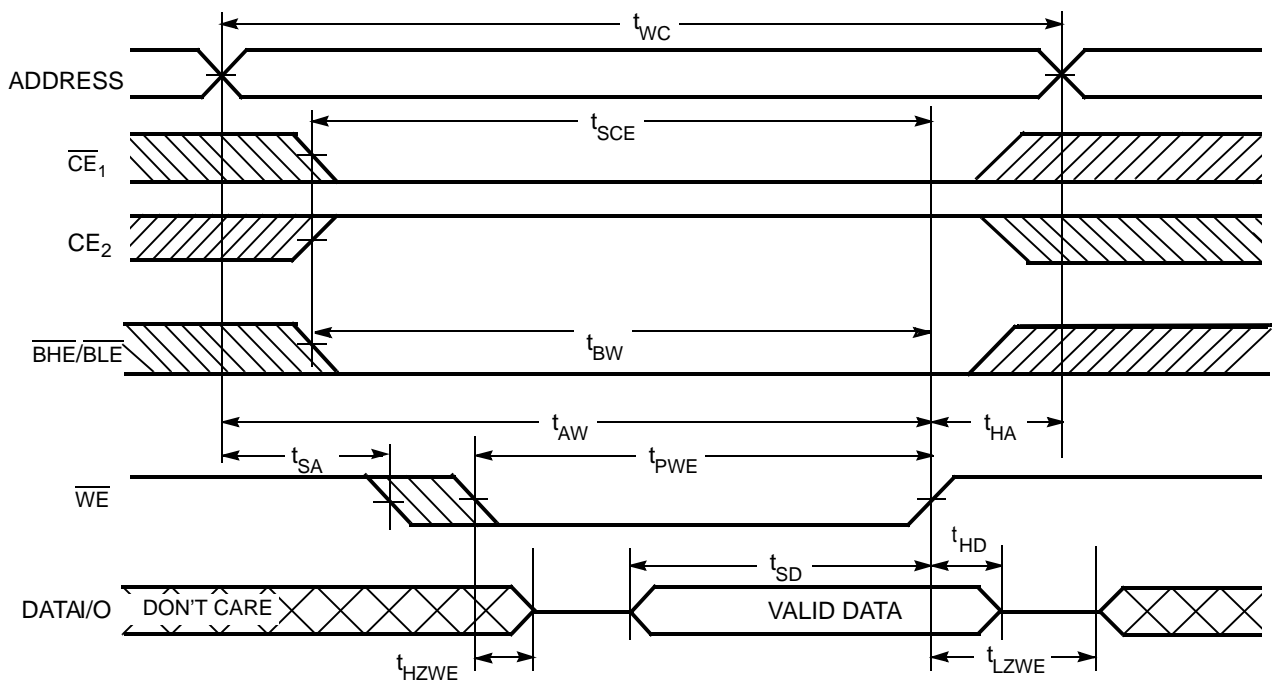21. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

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Switching Waveforms (continued)

Write Cycle 2 ($\overline{CE}_1$ or CE$_2$ Controlled)[15, 12, 16, 20, 21]
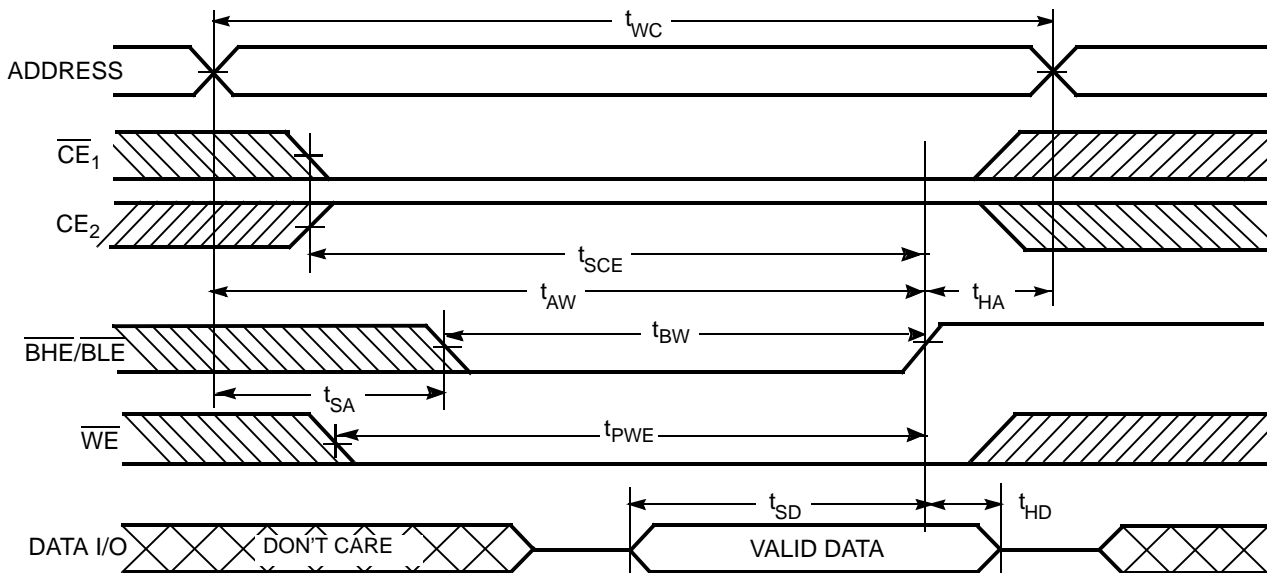

Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16, 21]

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Switching Waveforms (continued)

Write Cycle 4 (BHE/BLE Controlled, OE LOW)[15, 16, 20, 21]

Truth Table[22]

| $\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write (Lower Byte Only)	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write (Upper Byte Only)	Active (I_{CC})

Note:
22. H = Logic HIGH, L = Logic LOW, X = Don't Care.

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Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CYU01M16SFEU-70BVXI	51-85150	48-ball Fine Pitch VBGA (6 mm × 8 mm × 1 mm) (Pb-Free)	Industrial

Package Diagram

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)

51-85150-*D
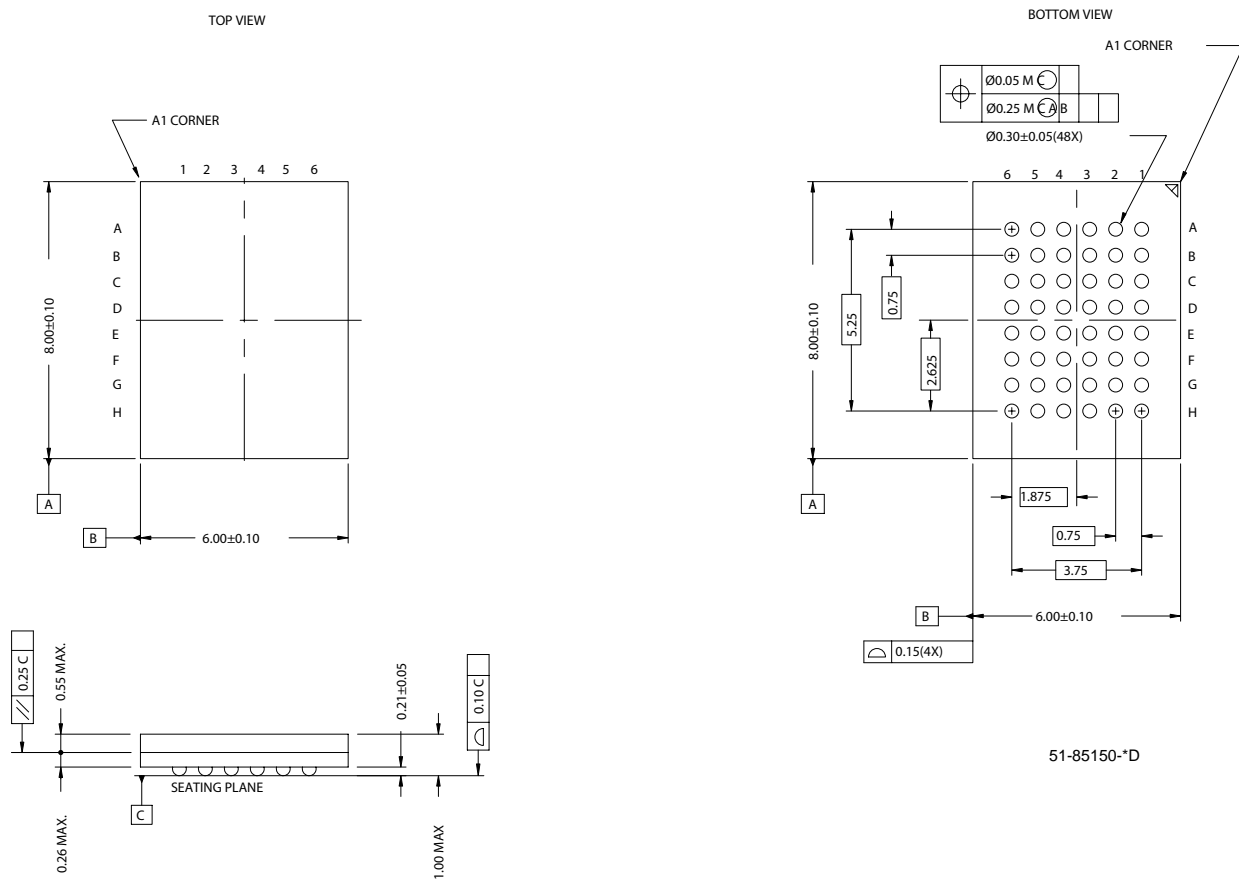
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Document History Page

Document Title: CYU01M16SFE MoBL3™ 16-Mbit (1M x 16) Pseudo Static RAM Document Number: 38-05603				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	342199	See ECN	PCI	New Data sheet
*A	386551	See ECN	PCI	Changed from Advance to Preliminary Replaced TBDs with appropriate values Changed t_{PC} and t_{PA} from 20 to 25 ns Corrected footnote # 16 as $\overline{OE} = \overline{CE}_1 = V_{IL}$ and $CE_{2} = V_{IH}$ Added separate waveforms for $\overline{CE}_1$ and CE_2 in Read #2, Page Read and Write#1 Timing diagram
*B	422623	See ECN	HRT	Removed the 55-ns Speed Bin Changed Isb2 Max value from 60 µA to 70 µA Added Isb1 to the DC parameters Added Chip Enable Access Foot Note to AC Parameters Changed the t_{CD} Min value from 5 ns to 15 ns Changed the Page Mode Values (t_{PC} and t_{PAA}) from 25 ns to 35 ns
*C	462289	See ECN	NXR	Revised MPN from CYU01M16SFCU to CYU01M16SFE Renamed Package Name column with Package Diagram
*D	492939	See ECN	NXR	Removed Page Mode feature
*E	504021	See ECN	NXR	Converted from Preliminary to Final Changede I_{CC}(Max) from 25 mA to 20 mA Changed t_{OHA}(Min) from 5 ns to 10 ns

[+] Feedb