AN932
APPLICATION NOTE

L4955 FAMILY, APPLICATION GUIDE

by Domenico Arrigo

The L4955 ULDO (Ultra Low dropout) linear regulators family is realised in BCDII technology, first and unique example of a multi-Amps regulators making use of an N-channel lateral D-Mos transistor, versus the most common solution of a power bipolar pass element.

Benefits in using such a power device is to have a quiescent current constant and independent from load current situations as well as very fast line and load transients.

The product family includes a full feature device in Heptawatt package, with output adjustable, inhibit, power good, external limiting current, and fixed (or adjustable) versions in TO-220.

The fixed outputs are 3.3V, 5.1V and 12V, the most common standard output voltages.

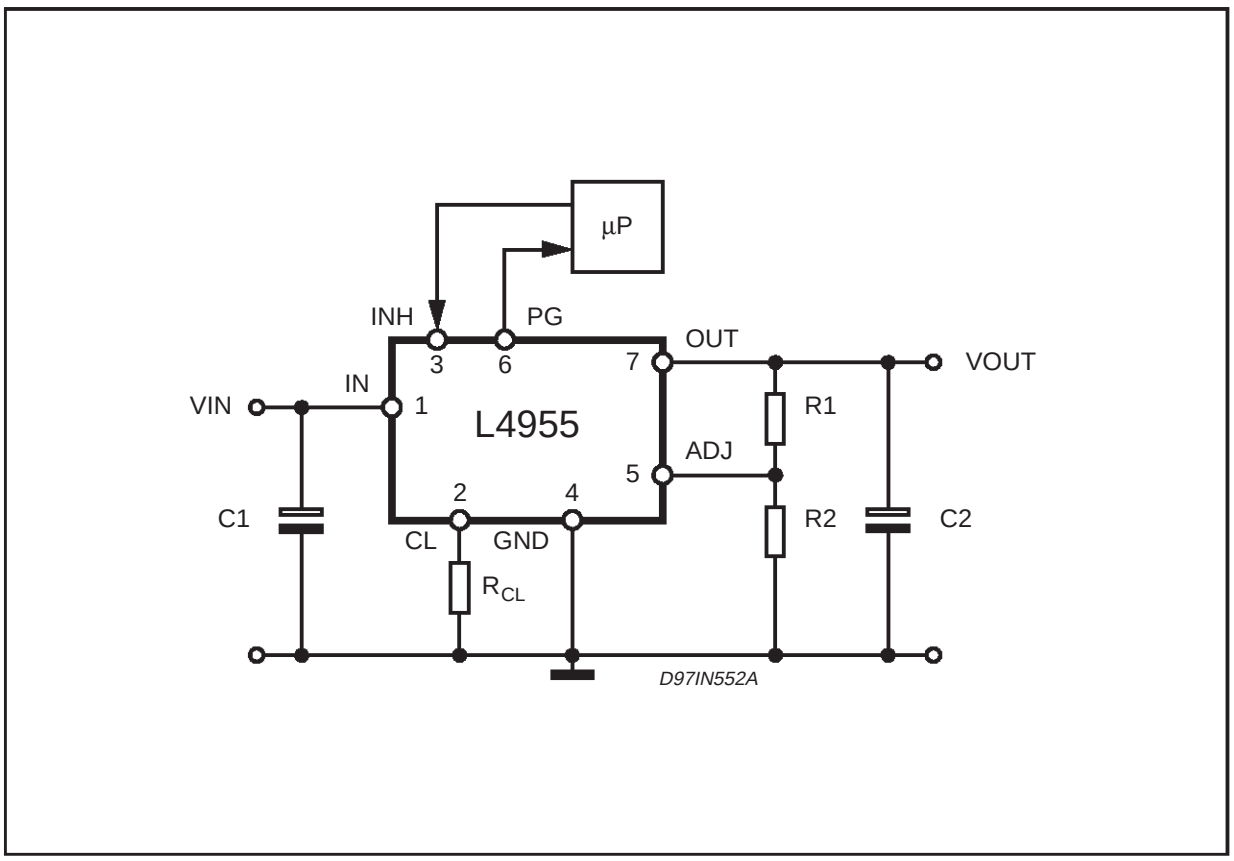
The min. regulated output voltage is 1.26V, while the input voltage is ranging from 4.5V to 22V.

The Heptawatt version, full feature, makes this device useful for systems using improved power management solutions, to supply advanced µ-processors (see fig. 1).

Moreover, due to its ability to regulate the output current it can be used as a post-regulator in many different applications covering up to 5A maximum current.

An electrolytic capacitor of 22µF is requested for output stability, while 10µF min are requested on input supply voltage.

Figure 1. L4955 Typical Application.



WHY LINEAR REGULATORS ?

The operation of a linear regulator is very simple and simple is also the application topology.

The output voltage is determined by the difference between the input voltage and the voltage drop of the pass element, which is modulated by the current flow and input voltage variations.

Benefits of a linear regulator versus the switchers are :

- lower application cost.
- simpler topology.
- less external components (two caps, a voltage divider on adjustable types) versus switchers and discrete solutions.
- easier layout precautions.
- zero output ripple.
- 10-15 times faster load transients response time versus switchers.
- ideal for post-regulation in multioutputs SMPS, comprehensive of limiting current and thermal shutdown.

LINEAR REGULATORS EVOLUTION

Starting from the early 80's, the famous standard linear L78XX series has been developed with a Darlington transistor as the pass linear power element, driven by a pnp transistor (see Fig. 2). It was an innovative solution for that time, in which the output power stage high gain was limiting the operating quiescent current to a few mA, irrespective of the load. The main drawback, discovered some years later, was the min. dropout voltage of a couple of Volt at 1A. It was not anymore acceptable for new emerging automotive applications. Min dropout is: Vbe1 + Vbe2 + Vcesat3.

Able to reduce the dropout to values lower than 2V were the "low dropout" regulators, in the '82 and '83. The power stage was realised with an NPN transistor, driven directly by a PNP type.

Example of this design solution is the L2600 family, automotive oriented because able to regulate 5V output with 7V min. supply voltage coming from car battery.

Fig.3 shows the power stage topology: the dropout is equal to Vcesat1+Vbe1, lower than 1.5V, while the operating quiescent current was kept at reasonable values.

Figure 2. Standard Darlington Regulator.

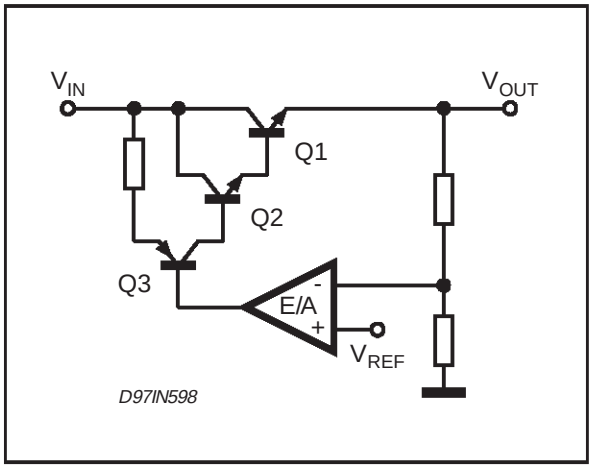
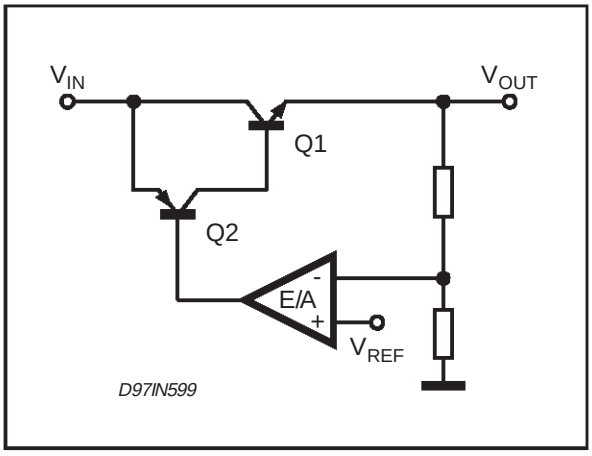
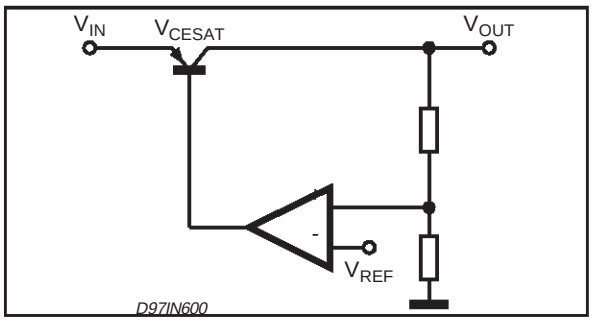


Figure 3. Low drop Regulator with NPN Transistor.



Further requirements, around middle 80's were to have regulation on the 5V output, with about 6V of min. input supply voltage. This generated the need of new "Very Low Drop" regulator families (see Fig. 4), like L4940, L4941 and L48xx family, using a single PNP transistor as the power element lateral first, followed by a vertical solution around '85.

Figure 4. Very low drop regulator with PNP transistor



In this case, the min dropout is one Vcesat only, around 1V at 1A.

The weakness of this solution is the quiescent current, growing proportionally to the output load current, in particular when the input supply is close to the output voltage, i.e., when the power element is close to saturation.

This causes efficiency problems in applications supplied with batteries and so limited autonomy.

On the second half of 80's, MOS transistors, a new way to manage power, opened new horizons in switching frequency and losses.

One employment was a realisation of high current linear post-regulators in discrete forms.

Fig. 5 shows a solution with P-channel, and Fig. 6 with N-channel transistor.

Good solutions from efficiency and performance point of view, they are scarce in reliability. Besides it is expensive to add limiting current and thermal protection.

With such a solution we reached the 90's.

In '96 , the new L4955 family solved these remaining two problems. See Fig. 7.

Figure 5. Discrete P-Channel MOSFET Regulator

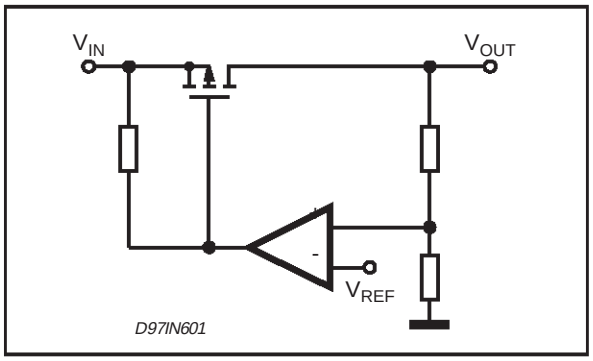


Figure 6. Discrete N-Channel MOSFET Regulator

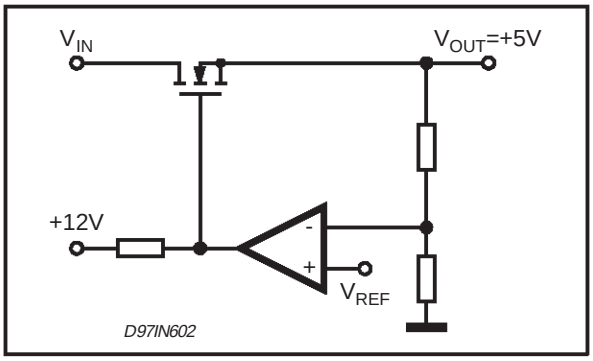
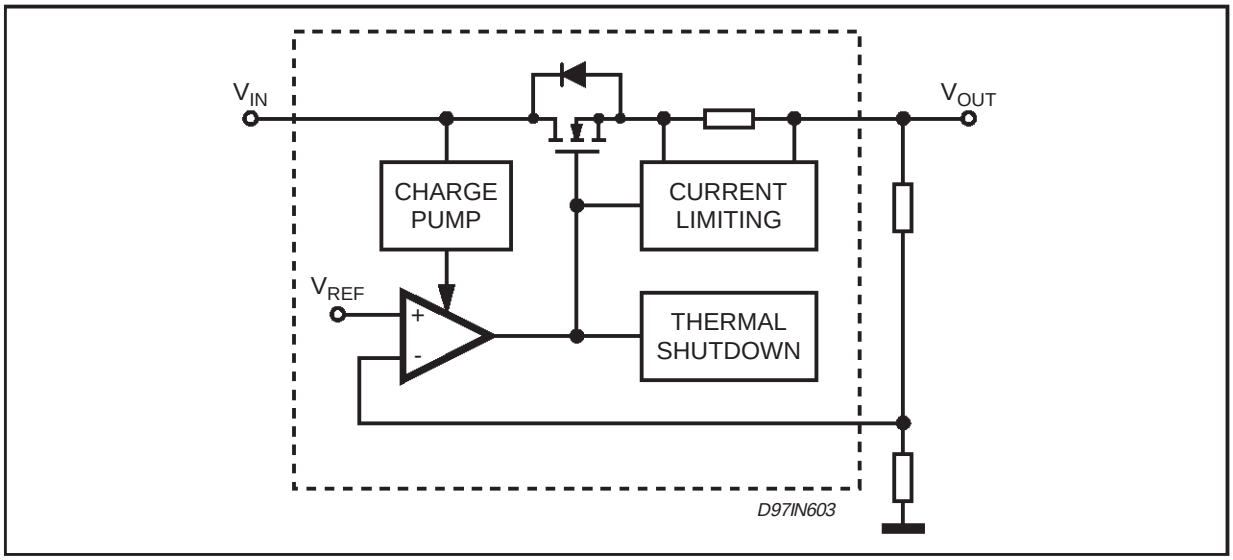


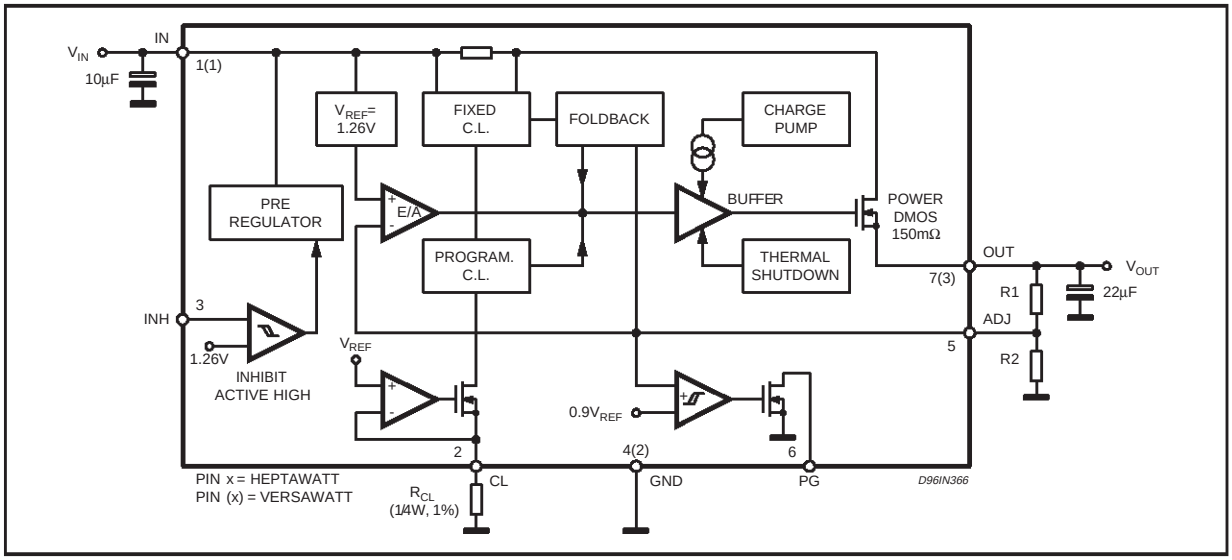
Figure 7. N-Channel MOSFET Integrated Regulator (L4955)



L4955, DEVICE DESCRIPTION

Fig. 8 shows the block diagram.

Figure 8. Block Diagram



PIN DESCRIPTION

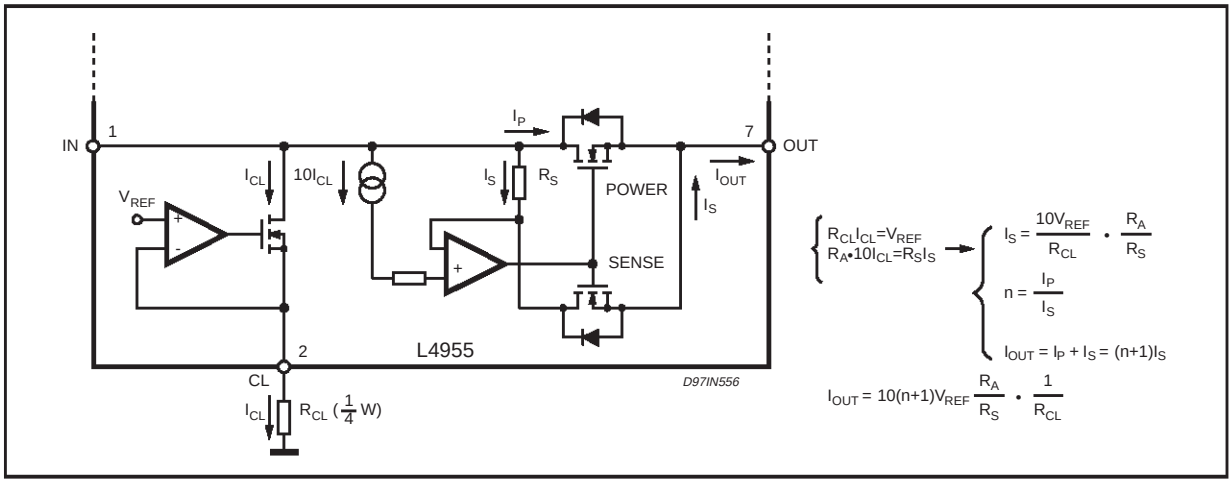
PIN1, IN (INPUT SUPPLY VOLTAGE) .

This is the unregulated input dc voltage. For stability reasons a 10uF min. capacitor value is required.

PIN2, CL (CURRENT LIMITING).

The device is provided with two different current limiting functions, programmable and fixed .

Figure 9. Programmable current limiting circuit.



An external resistor Rcl (+/-1%, 1/4W), connected between pin2 and ground, sets the requested current limiting threshold to a typical value given by :

$$I_{lim} = \frac{39.69}{R_{CL}} \text{ [A]} \quad \text{with} \quad R_{CL} \text{ [k}\Omega\text{]}$$

So we get the following table :

R_{CL} (Ω)	I_{lim} (A)
13k	3
19k	2
40k	1
47k	0.85

The programmable current limiting has a constant current characteristic, without foldback effect.

The programmable current limit is guaranteed only in the range of Rcl between 13kΩ and 47kΩ (see fig 10), with a guaranteed accuracy of about 20%. A difference of about 200mA between the load current and the set current limit is necessary to separate at all the current from the voltage loop maintaning the regulated output voltage at the load current.

It is not recommended to use resistor values out of the above mentioned range.

Figure 10. Programmable Current Limit.

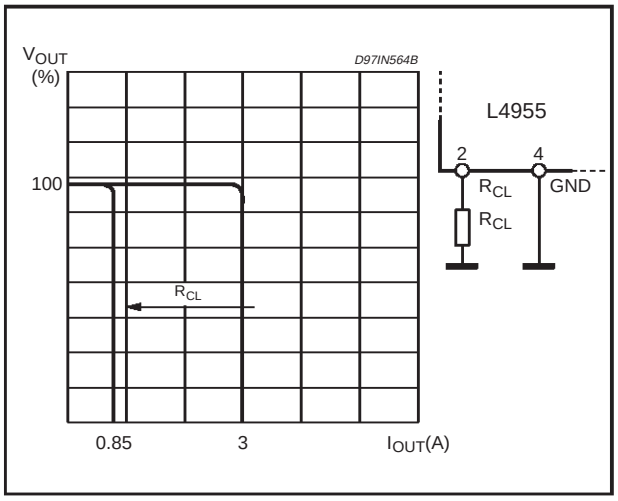
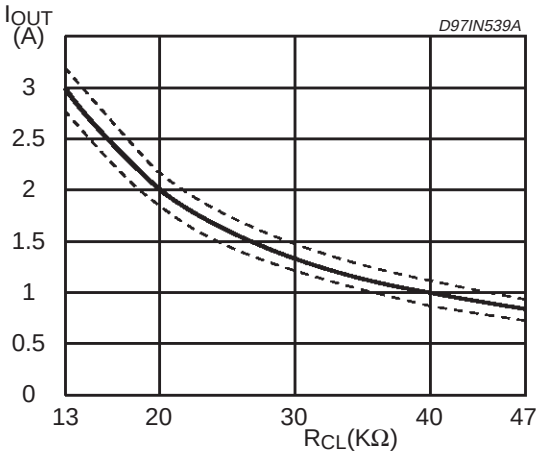


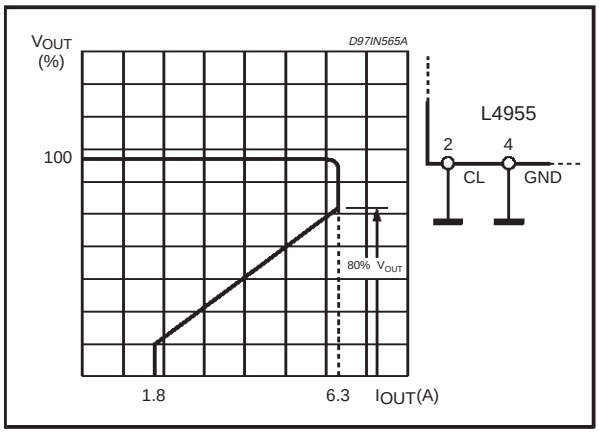
Figure 11. Output Current Available vs Resistor Value.



The pin cannot be left floating; when not used, it has to be connected to GND.

Fig.11 shows the output current available vs. resistor value. In programmable current limiting with R_{CL}=13KΩ the dropout has to be higher than 1.5V, otherwise the current limit is about 6.3A. This minimum drop to enable the programmable current limiting, can be reduced at about 1.1V with R_{CL} = 47KΩ.

Figure 12. Internal current limiting.



By connecting pin 2 to ground the programmable current limiting is overridden by the fixed current limitation (6.3A +/-20%). A foldback function (typ. 1.8A), see figure 12, protects against load short-circuits and limits the power dissipation. The foldback circuit starts to reduce the short-circuit current when the output voltage at the pin7 , falls below 80% of the regulated value.

PIN3, INH (INHIBIT).

This function allows to turn the regulator off , with a consumption of only 120µA.

It can be switched to a frequency up to 5kHz. It is a TTL-CMOS compatible input, active high, disactivating all the blocks except the internal band-gap (see Fig. 13).

Figure 13. Inhibit Circuit.

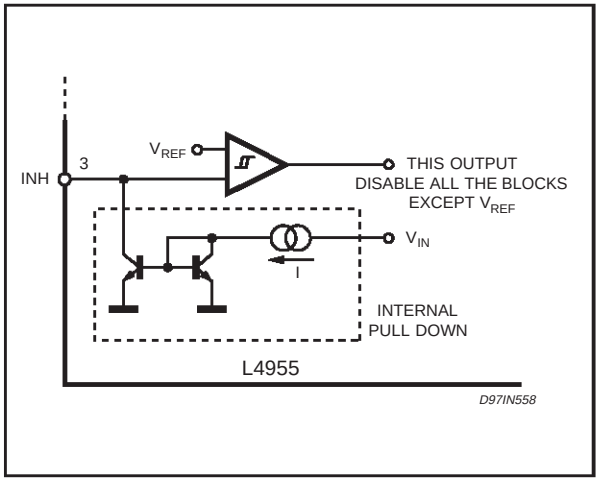
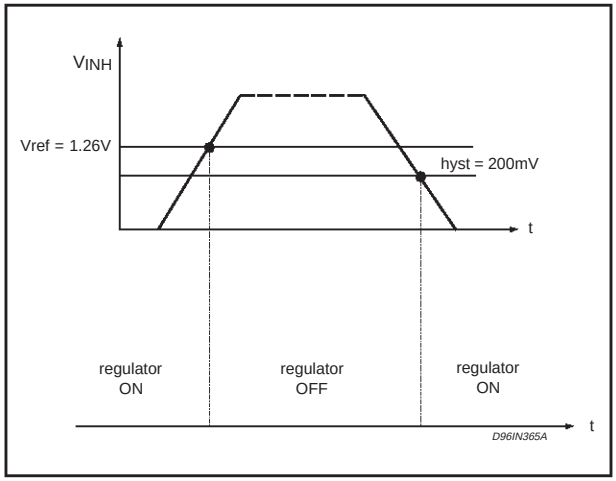


Figure 14. Inhibit Function

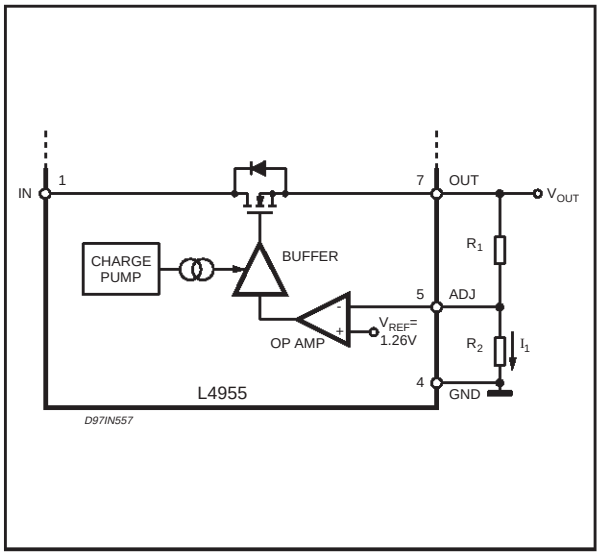


This function, see fig 14, is realised by a comparator with a threshold of 1.2V and 200mV of histeresys. The internal bias sink current is 20uA. The pin can be left open because an internal pull-down insures the correct functionality.

PIN4, (GND).

This is the ground pin of the device. It has to be connected close to the load to improve regulation. The quiescent current flowing from this pin is a couple of mA, irrespective of the load current. When INHIBIT is activated, the current flowing from this pin is about 120µA.

Figure 15.



PIN5, ADJ (ADJUST).

This pin, with the help of a voltage divider, is used to adjust the output voltage.
The output voltage range can go from a min of 1.26V to Vin-Vdrop.

The output regulated voltage can be calculated as follows:

$$V_{out} = (R_1 + R_{2)} \cdot I_1 = \left(\frac{R_1}{R_2} + 1\right) \cdot V_{ref}$$

The R2 value can be determined by fixing the current, I_1, circulating in it (see Fig. 15):

$$R_2 = \frac{V_{ref}}{I_1} = \frac{1260}{I_1} \quad [\Omega] \quad I_1 \ [mA]$$

and so:

$$R_1 = R_2 \cdot \left(\frac{V_{out}}{1.260} - 1\right) \quad [\Omega] \quad V_{out} \ [V]$$

PIN6, PG (POWER GOOD).

This pin is activated (LOW) when the Vadj voltage value is lower than 10% of its nominal value. This means also an output voltage 10% lower than the selected nominal value (see Fig. 16).

This output can also be used as a flag in case of overcurrent conditions.

PG signal can be used to initialise the operation of a µP.

Figure 16. Power Good Function.

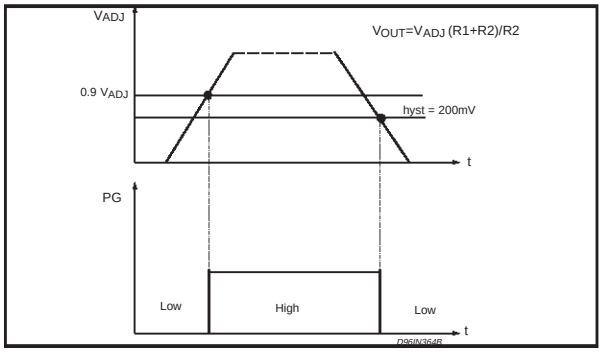
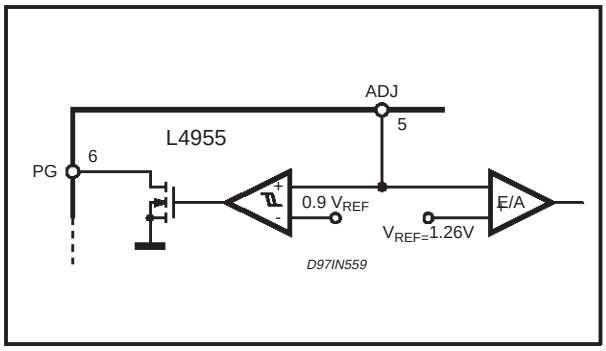


Figure 17. Power Good Circuit.



The circuit, see fig 17, is realised by a comparator with hysteresis of 200mV and an open drain output. The output resistance of the power good is 100Ω max. at T_j =125°C.

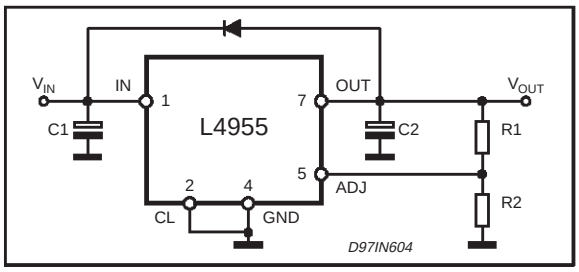
PIN7, OUT.

Regulated output voltage. The minimum electrolytic capacitor required for stability is 22µF .

THERMAL SHUTDOWN

The thermal protection is an internal hysteretic function which turn off the device when the junction temperature exceeds 150°C. Hysteresys is around 20°C.

Figure 18. Protection Diode.



PROTECTION DIODE

In normal operation, the L4955 family does not need any external protection diode between input and output. The internal body diode between input and output can handle current of about 10A for milliseconds. For example, if Vout = 12V, an instantaneous short circuit to the input pin1 with large output capacitor value, such as 880µF, does not damage the device. It needs protection diode (see Fig. 18) only for high value of output capacitors (bigger than 1000µF).

DEMOBOARD L4955 HEPTAWATT

To evaluate the device dynamic behaviours, a demoboard has been designed and optimised for this point of view. The electrical schematic diagram is shown in, Fig.19.

The demo, in any case, can house both SMD or through-hole capacitors, for testing in different conditions, standard and extreme. To obtain excellent performance under very fast load transients, it is mandatory the minimisation of the distributed inductance and of course the resistance too.

Due to these two constrains, a double side pcb has been laid out.

Figure 19. Demo Circuit Schematic.

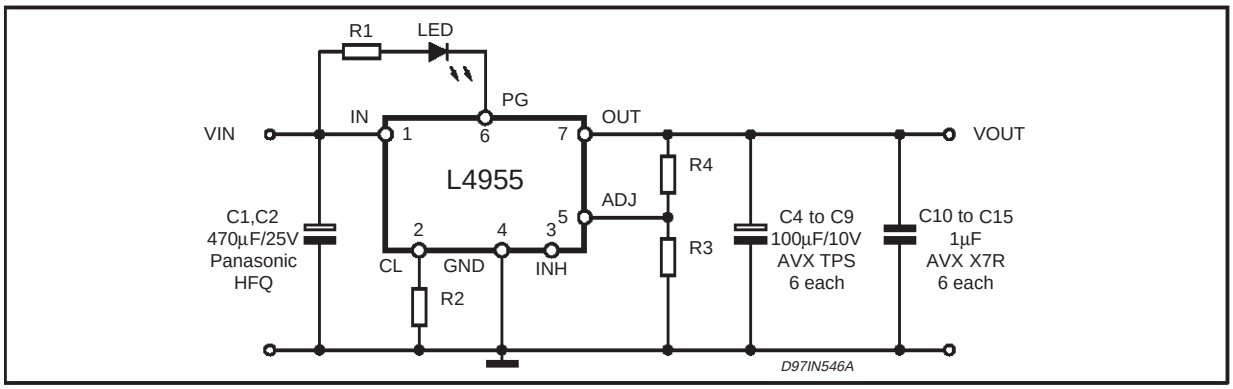
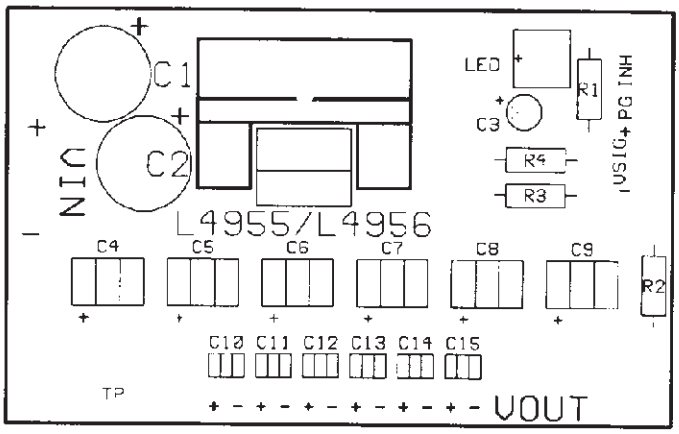
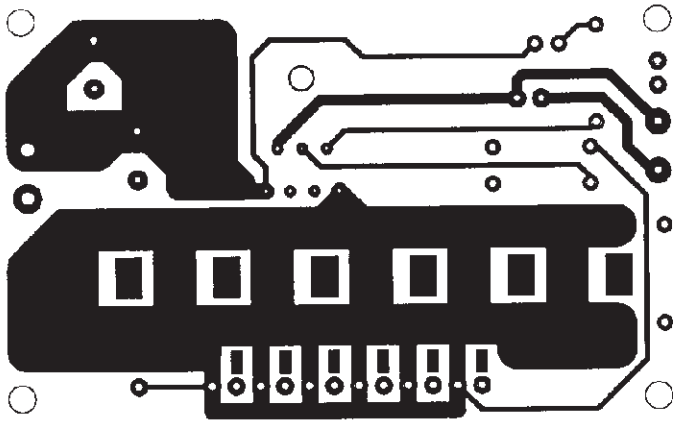


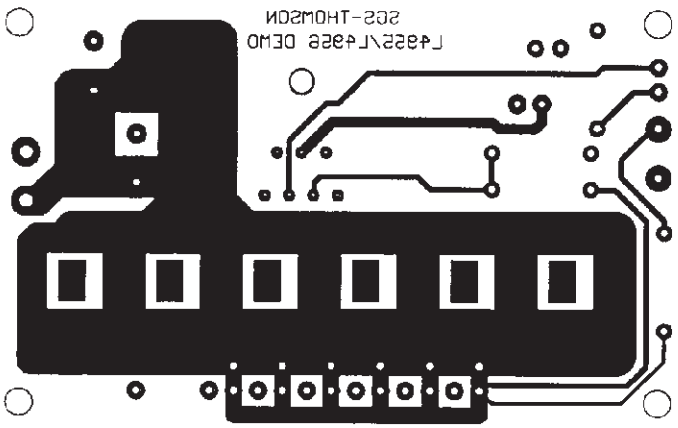
Figure 20. Printed Demo Board (scale 1:1).



COMPONENT SIDE



LAYER 1



LAYER 2

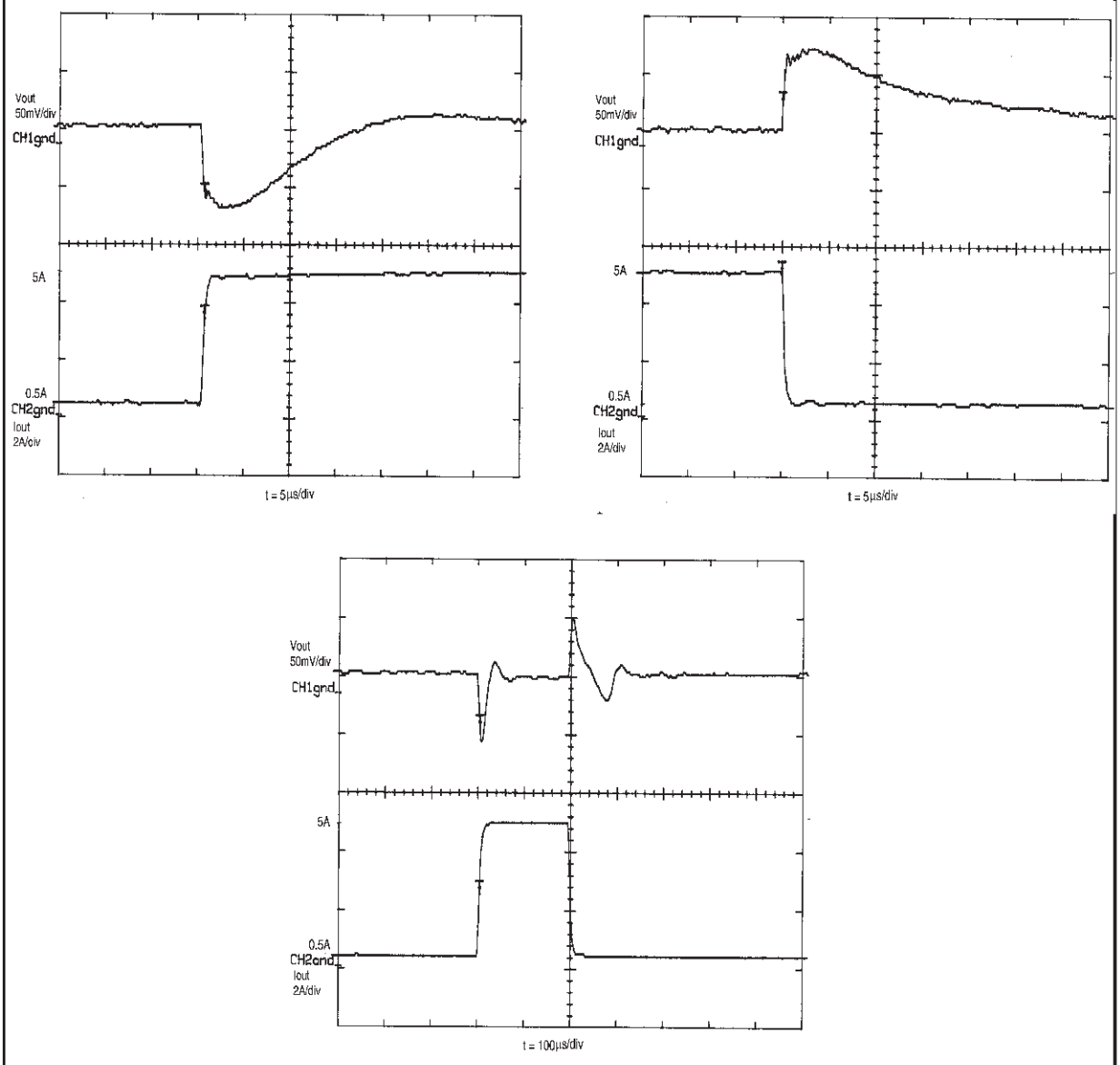
The output capacitors have to be chosen with low ESR, like SMD tantalyum which are a good compromise between low ESR, cost and size. The SMD solution permits to avoid the vias inductances. It is useful to put low ESL capacitors very close to to the output connector. The input capacitors, have to be chosen with low ESR to avoid the drop of the supply voltage during the load transient.

The resistors divider of the voltage feedback, connected directly to the load ground, allows the separation of sensing and forcing avoiding to sense the drop voltage of the power paths.

Here follow some load transient responses obtained with the DEMOBOARD L4955, full populated as in Fig. 19.

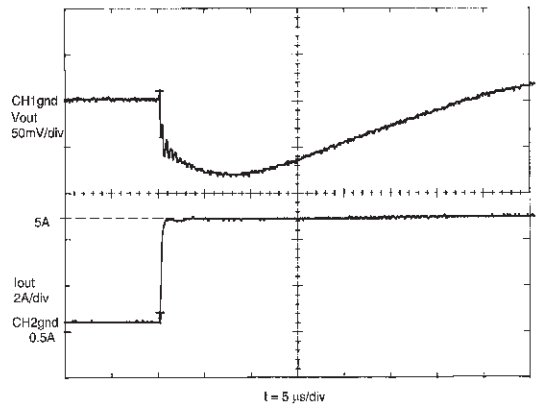
LOAD TRANSIENT RESPONSES

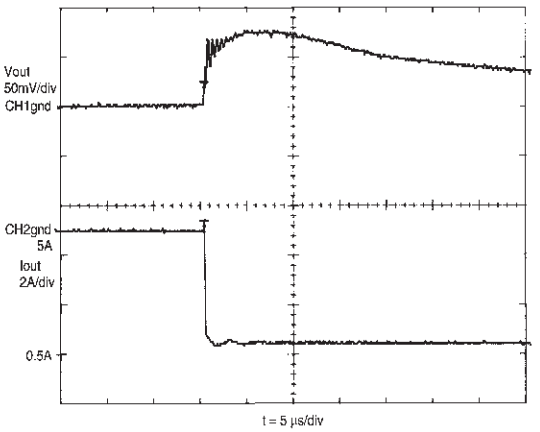
Figure 21.

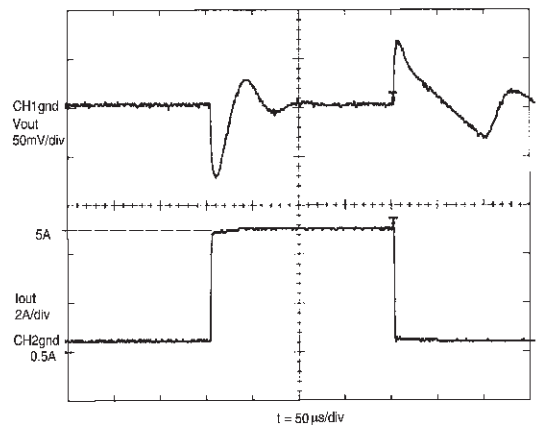


Test condition: V_{IN} = 5V, V_{OUT} = 3.3V; Load Transient from 0.5A to 5A; $\frac{dI_{out}}{dt} = 20A/\mu s$; T_J = 25°C

Figure 22.



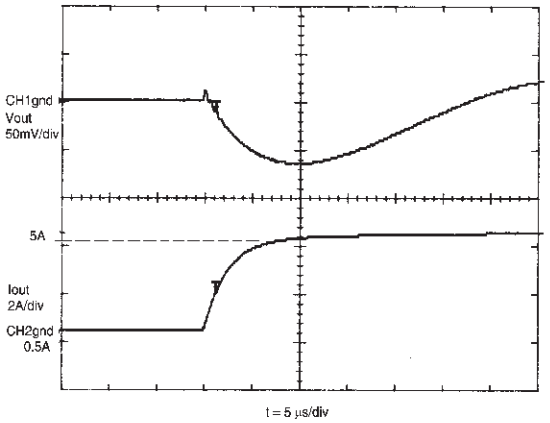


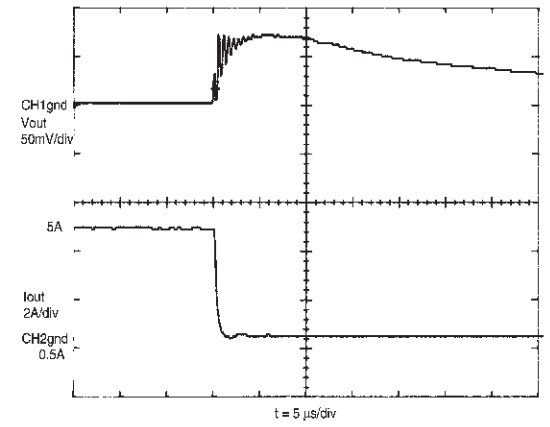


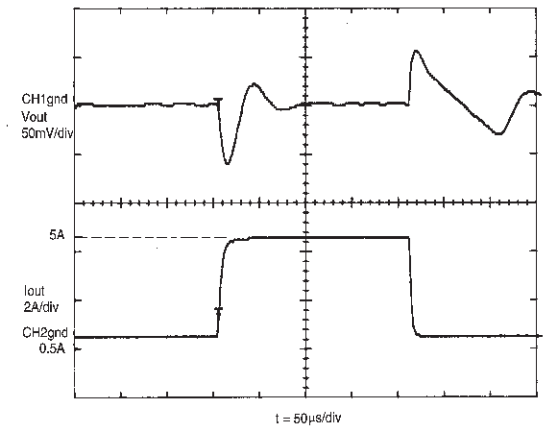
Test condition: V_{IN} =6. 5V, V_{OUT} = 5V;
Load Transient from 0.5A to 5A;

$\frac{dI_{out}}{dt} = 20A/\mu s$; $T_J = 25°C$

Figure 23.







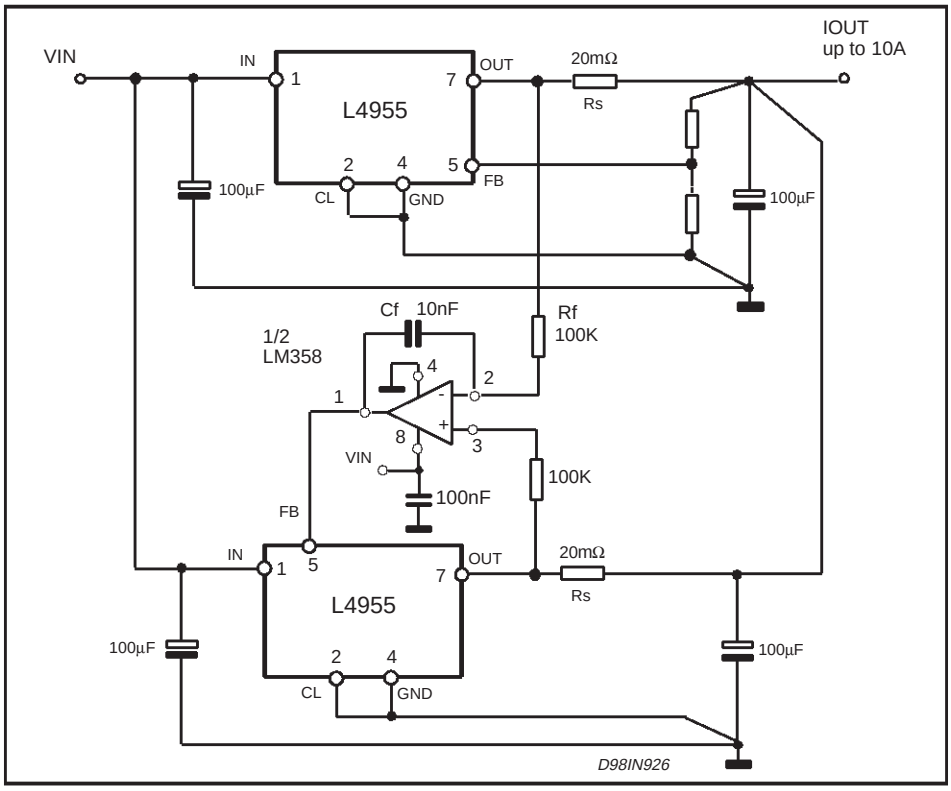
Test condition: V_{IN} =6. 5V, V_{OUT} = 5V;
Load Transient from 0.5A to 5A;

$\frac{dI_{out}}{dt} = 1A/\mu s$; $T_J = 25°C$

APPLICATION IDEAS

PARALLEL REGULATORS

Figure 24. Parallel Regulators.



The L4955 regulators can be paralleled as in the schematic circuit of fig. 24. This application can deliver up to 10A of output current. This solution improves the efficiency and the output current capability and it allows to distribute the power dissipation. For example, assuming V_{IN} = 13.5V, V_{OUT} = 12V, I_{OUT} = 10A, the output power delivered to the load is 120W. The total power dissipation is around 16W and the total efficiency is η = 88%.

SOFT START

Fig. 25 shows a simple solution to obtain a soft-start at regulator turn on.

At start up, the output voltage step up to Vadj + Vd1, then the charging of C1 in parallel with R1 regulates the rising sharp of the output voltage, by the time constant R1C1.

For example, if Vout = 8.4V, C1 = 330nF and R1 = 68kΩ the soft-start time of the output is about 4R1C1≅ 90ms (see fig. 26).

The diode D1 is used to decouple the C1 capacitor from the feedback network after the start up.

The diode D2, in short circuit condition, by-passes R2 and so C1 is fast discharged improving the recovery time. Moreover D2 avoids dangerous negative voltage at pin Vadj during the short circuit current recirculation.

Figure 25.

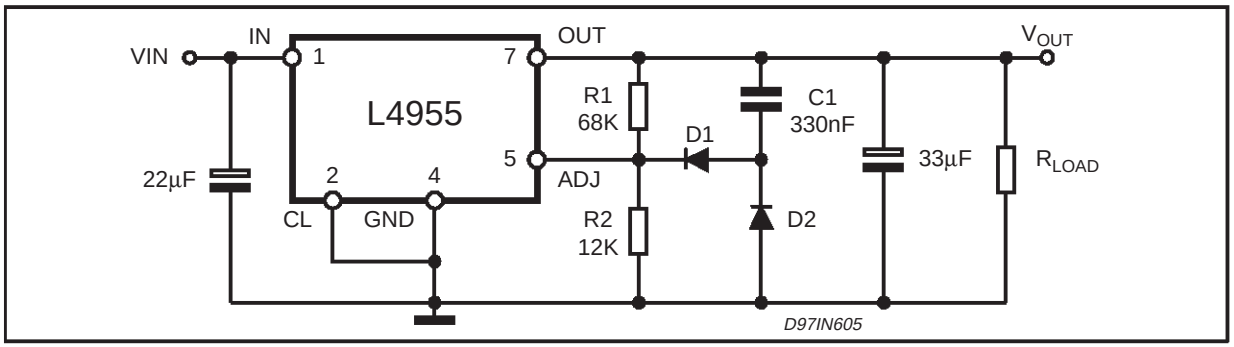


Figure 26.

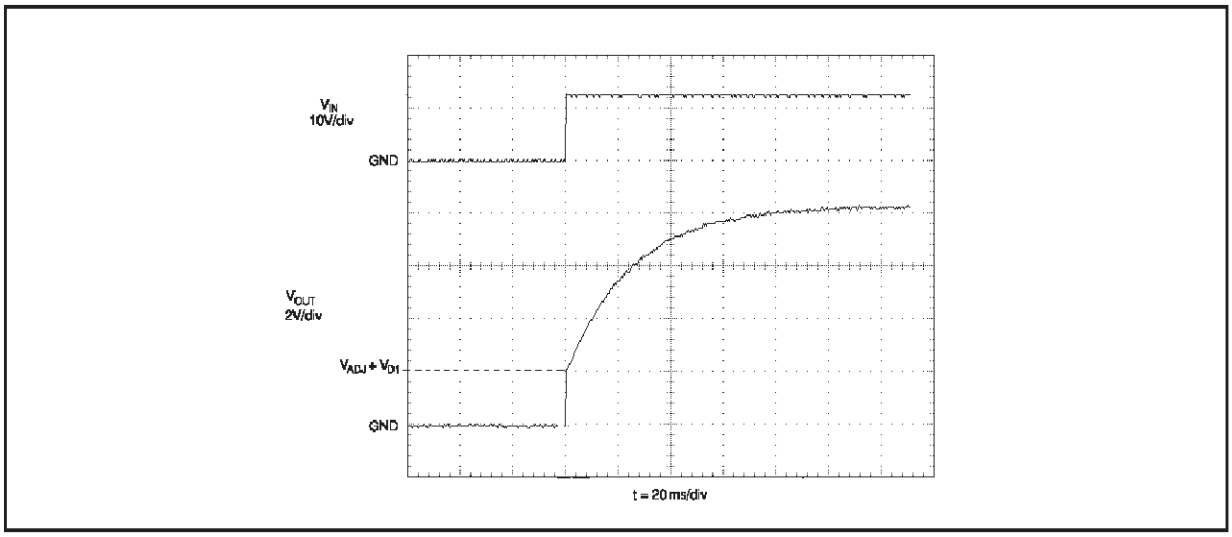
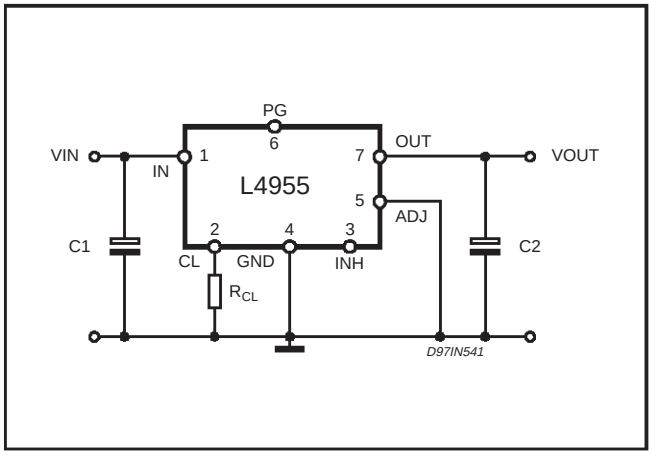


Figure 27.



PROGRAMMABLE CURRENT REGULATOR

By connecting PIN5, ADJ, to ground, the device works as a current regulator (see fig.27).

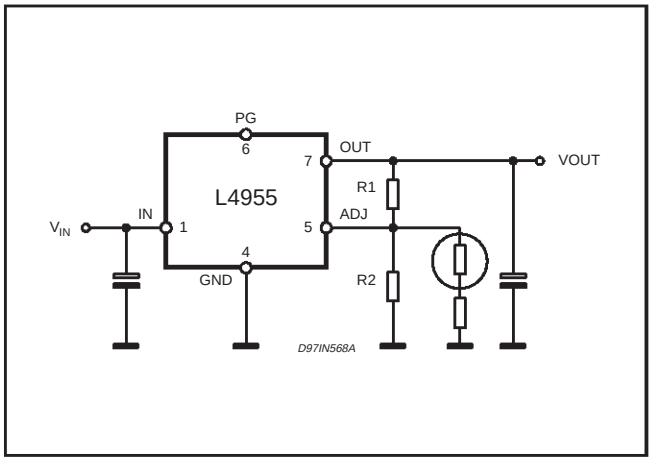
The output current is fixed by Rcl to a typ. value given by :

$$I_{OUT} = \frac{39.69}{R_{CL}} \text{ [A]} \quad \text{with} \quad R_{CL} \text{ [k}\Omega\text{]}$$

If pin2 , Rcl, is grounded the current limit is the foldback value of around 1.8A.

The output voltage can reach a maximum value given by the difference between Vin and the dropout voltage, which depends on Iout.

Figure 28.



LIGHT CONTROLLER

By putting a photo resistor in parallel with R2 (see Fig.28), the output voltage is controlled by the brightness of the surrounding enviroment. In particular in this application the output voltage increases as the brightness increases.

PRECISE CURRENT REGULATOR

Figure 29.

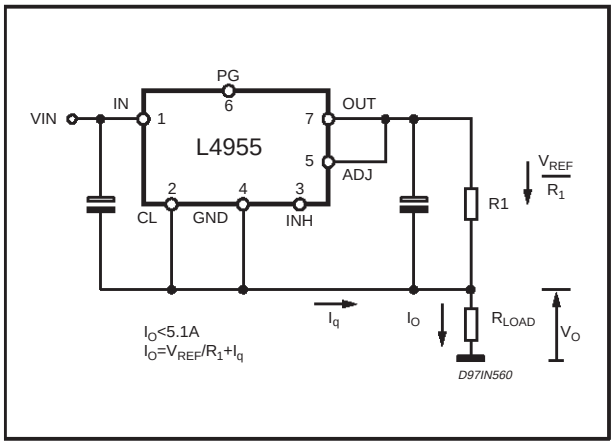
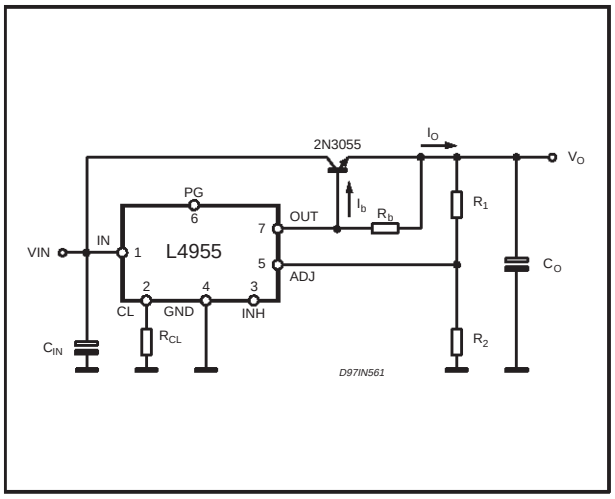


Figure 31.



Example 1.

Electrical spec. Vout = 5V and Iout = 8A

Using L4955 plus 2N3055, the thermal balance is (considering the **L4955** max**Rdson** = 300mOhm @125°C):

PDmax = Vce · Io = 16W (@ B=5) for 2N3055

PDmax = Io^2 · Rdson= 0.8W for L4955

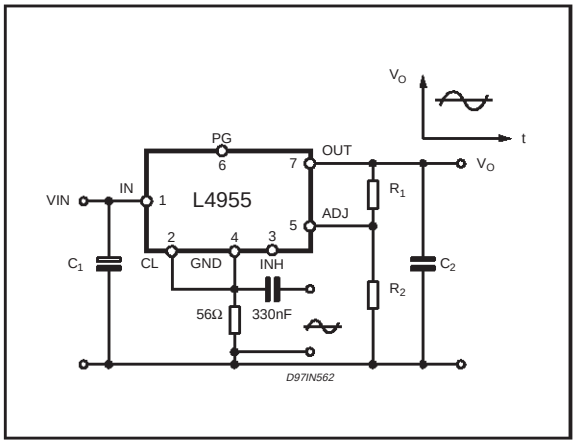
Total power dissipation ≅ 17W

Minimum Input Voltage = 7V

Note: This specification cannot be met by using L4955 stand alone.

POWER AM MODULATOR

Figure 30.



HIGH CURRENT VOLTAGE REGULATOR

In applications in which the required output current can be higher than 5A, or to reduce the power dissipation of the L4955, an efficient solution is shown in Fig 31.

The L4955 drives the base of a npn transistor (2N3055).

This configuration can deliver up to 10A .

This application holds the L4955 functions of current limiting, inhibit and power good.

The current limitation can be obtained with the fixed current limiting, selectable with Rcl, which limits the base current, Ib, and so the output current .

The inhibit function, pin 3, allows to turn off the bipolar transistor.

To fix these concepts let us consider two examples:

Example 2.

Electrical spec. Vout = 5V and Iout = 4A

Using L4955 and 2N3055 :

PDmax = Io^2 · Rdson ≅ 0.5W for L4955

PDmax = Vce · Io = 5.2W for 2N3055

Total power dissipation ≅ 6 W

Minimum Input Voltage = 6.3V

Using L4955 stand alone :

PDmax = Io · Vdropmax = 5 · 1.2 = 6W

Minimum Input Voltage = 6.2V

Note: The total amount power dissipation is similar but it is moved on the external.

DIGITAL OUTPUT VOLTAGE SELECTION

Figure 32.

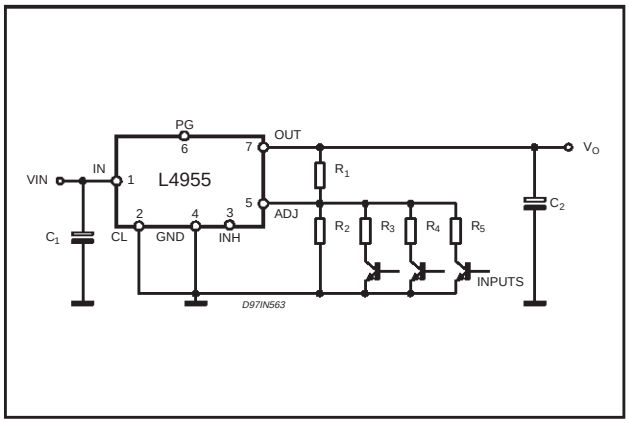
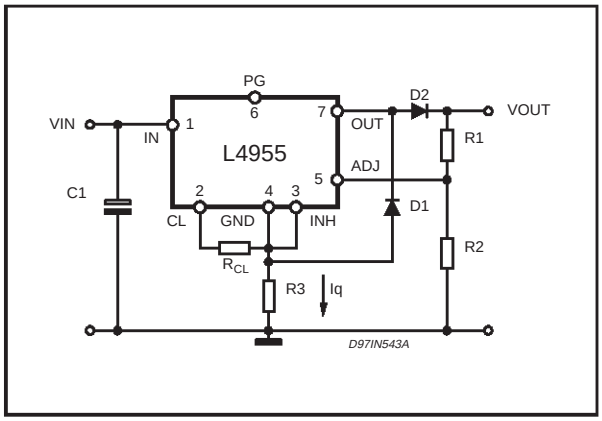


Figure 33.



LOW COST BATTERY CHARGER

In fig. 33 is showed a low-cost battery charger application.

The Rcl sets the charging current and the resistor divider determines the final charging voltage to a value given by:

$$\left(\frac{R_1 + R_2}{R_2}\right) \cdot (V_{ref} + R_3 \cdot I_q)$$

where Iq is the device quiescent current.
The schottky diode, D2, prevents the discharge of the battery through the device when this is off. The diode D1 limits the reverse current through the regulator if the battery is reverse connected.

HIGH INPUT AND OUTPUT VOLTAGE REGULATOR

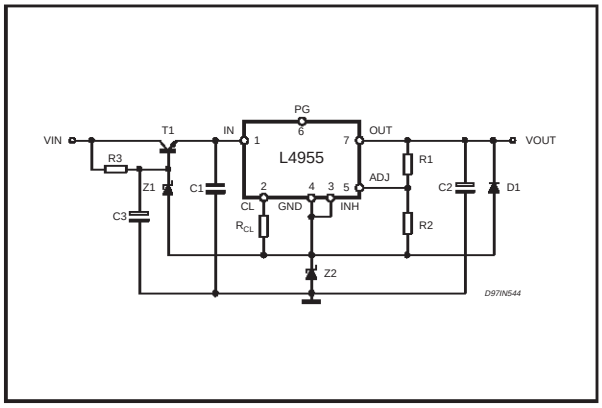
Fig. 34 shows a solution for input supply higher than device max supply voltage.

This schematic combines also higher output voltage.

The input voltage is reduced by the Vceon of a npn power transistor. The current target of the application must take into account the dissipated power of this transistor.

The high output voltage is obtained with the diode Zener Z2. The diode D1 provides output short-circuit protection.

Figure 34.



COMPENSATION OF VOLTAGE DROP ALONG THE WIRES

When it is not possible to use sensing and forcing to compensate load wiring connections, but only two wires are allowed to supply the load, the schematic of Fig. 35. reaches the goal.

If the resistance of the line, Rz, is known, using the resistor Rk (see fig. 34), the output voltage Vout can be expressed as :

$$V_{out} = \frac{R_k \cdot R_1}{R_2}(I_{load} + I_q) + \frac{R_1 + R_2}{R_2} V_{adj}$$

The load voltage, V_L, is:

$$V_L = V_{out} - R_Z \cdot I_{load}$$

Substituting the Vout espression, we get :

$$V_L = \frac{R_k \cdot R_1}{R_2} I_{load} - R_Z \cdot I_{load} + \frac{R_k \cdot R_1}{R_2} I_q + \frac{R_1 + R_2}{R_2} V_{adj}$$

If the voltage V_L has to be constant versus the load current, we have to impose the below condition :

$$\frac{R_k \cdot R_1}{R_2} - R_Z = 0$$

Solving for R_k, we obtain:

$$R_K = \frac{R_2 \cdot R_Z}{R_1}$$

Finally, the regulated load voltage VL is:

$$V_L = R_Z \cdot I_q + \frac{R_1 + R_2}{R_2} V_{adj}$$

Figure 36.

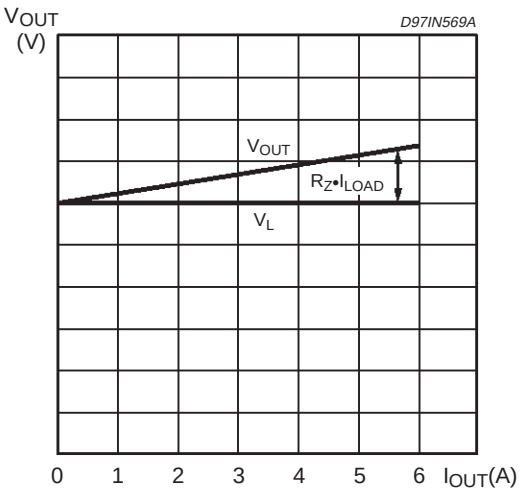
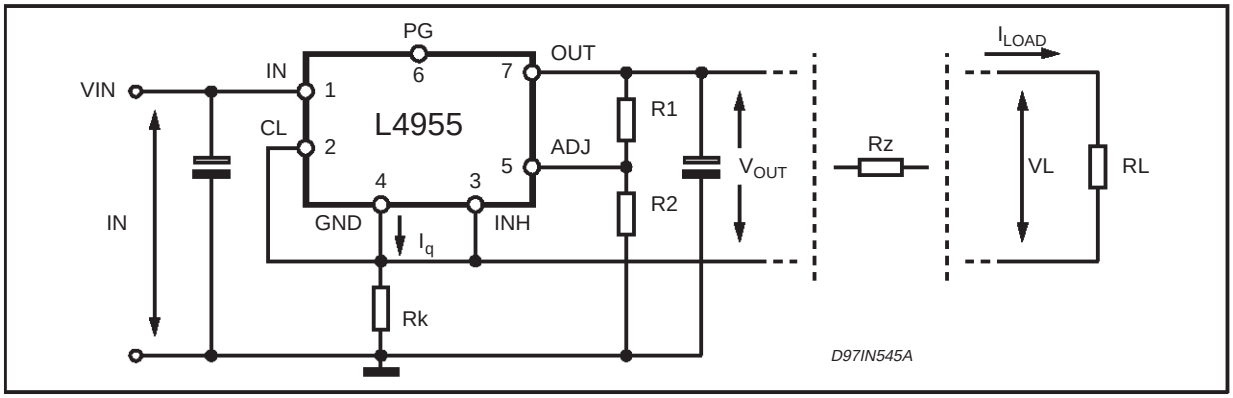


Fig. 36 sh ows V_{out} and V_L versus load current.

Figure 35.



L4955 VERSAWATT

The fixed output voltage versions, (3.3V, 5.1V, 12V) are available in 3-pin versawatt package (see Fig. 37). These versions (L4955Vxxx) are provided with internal fixed current limiting .

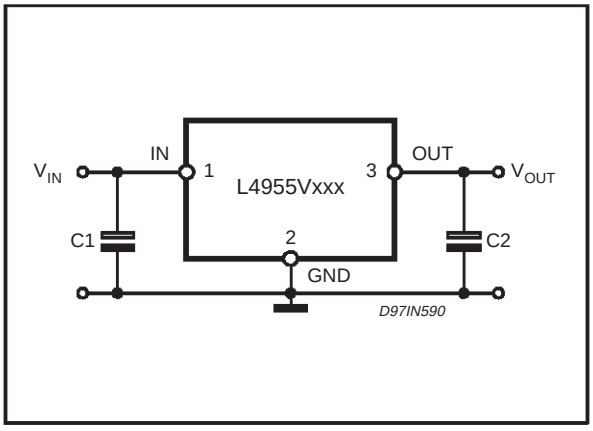
The power stage is totally equivalent to the heptawatt version, i.e., typical Rdson of 150mOhm @ 25°C .

The same dynamic performance and thermal shut-down function are guaranteed too.

The minimum supply voltage is the output voltage plus the max guaranteed dropout voltage, and in any case, min. supply has to be higher than 4.5V.

Fig.37 shows the typical application circuit.

Figure 37.



DEMOBOARD L4955 VERSAWATT

For evaluation purpose, a dedicated demoboard has been realised. The electrical schematic is shown in, Fig.38.

Figure 38.

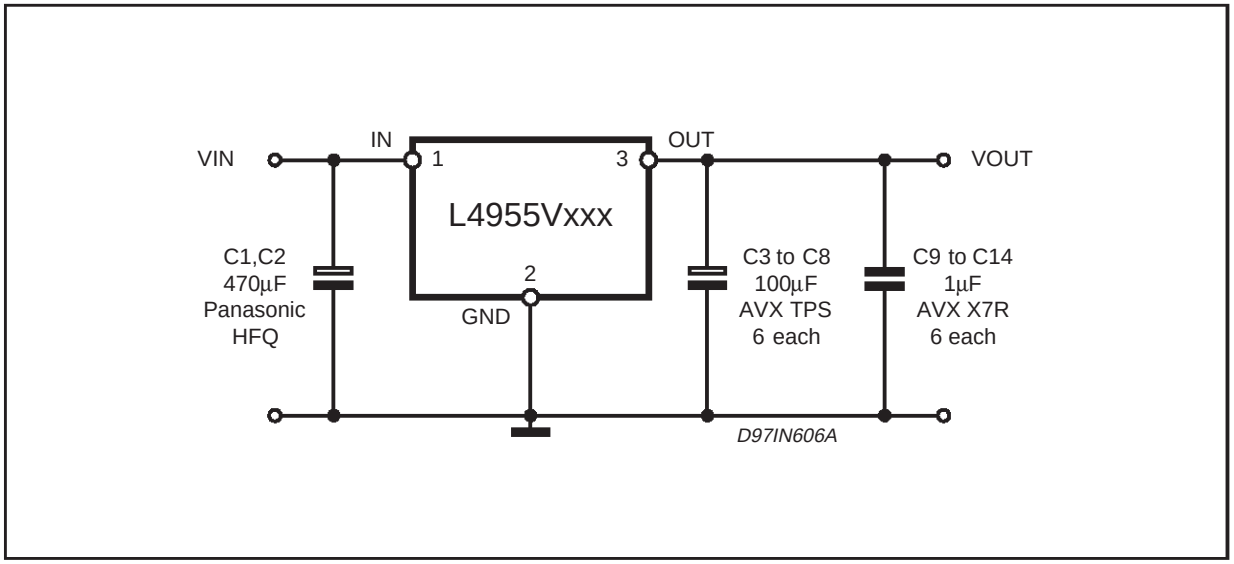
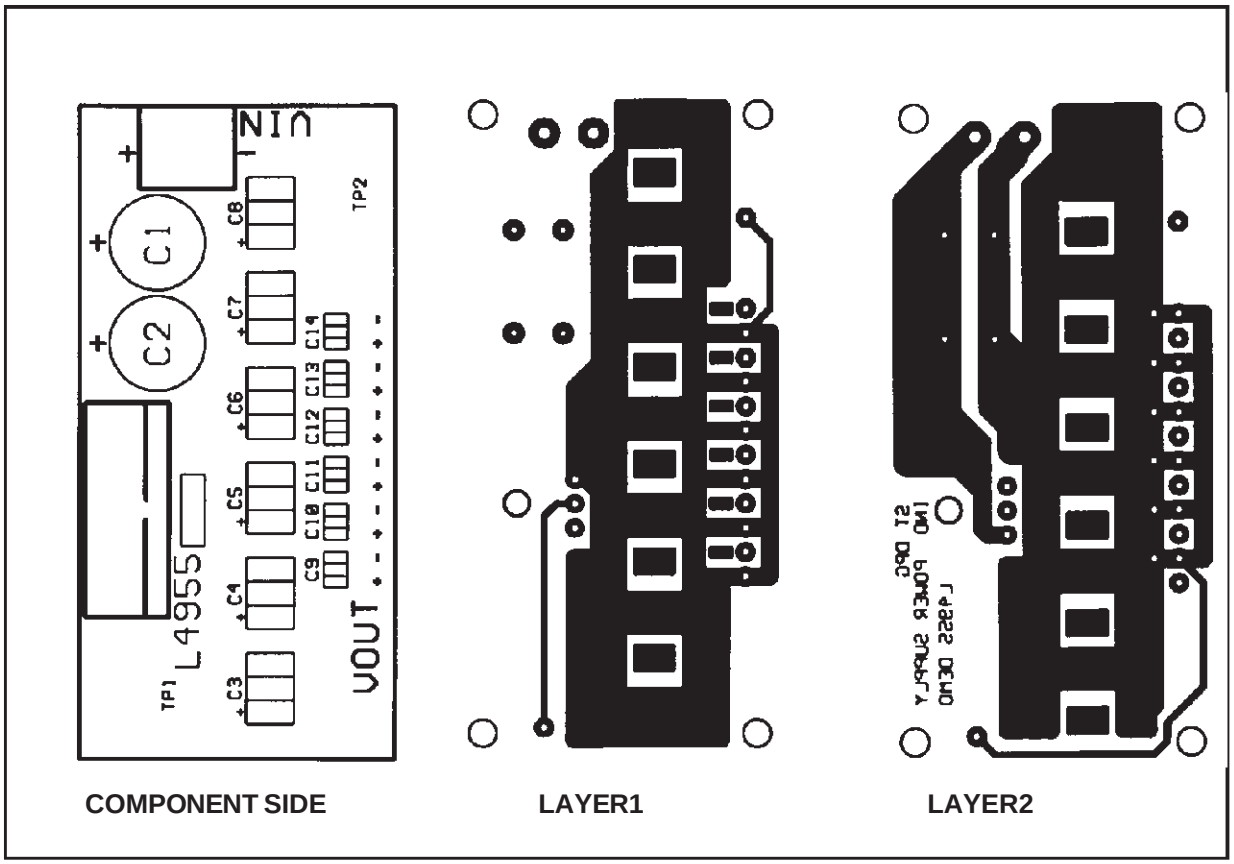


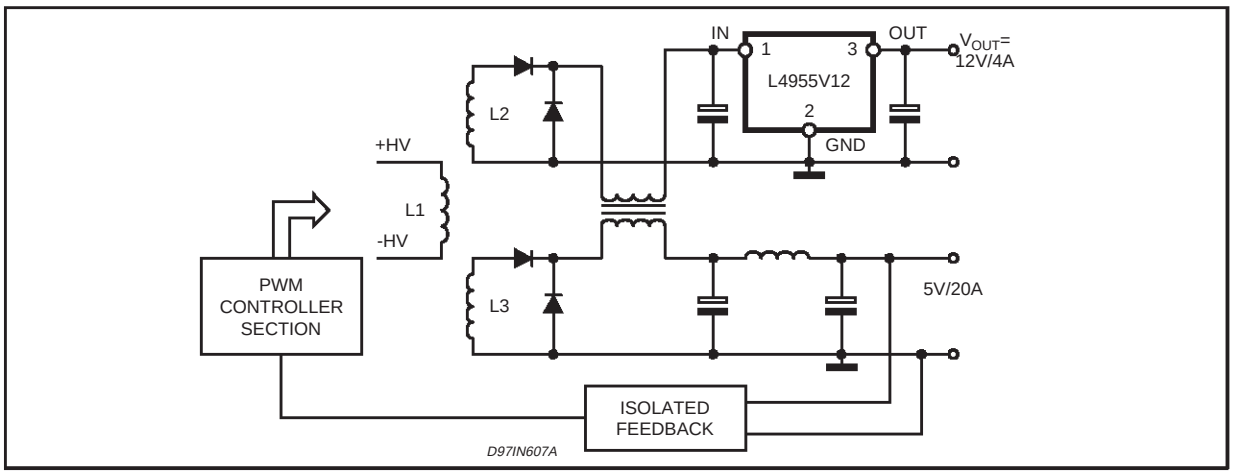
Figure 39. Printed Demo Board (scale 1:1)



APPLICATION IDEAS

COMPUTER POWER SUPPLY

Figure 40.



POWER AM MODULATOR

Figure 41.

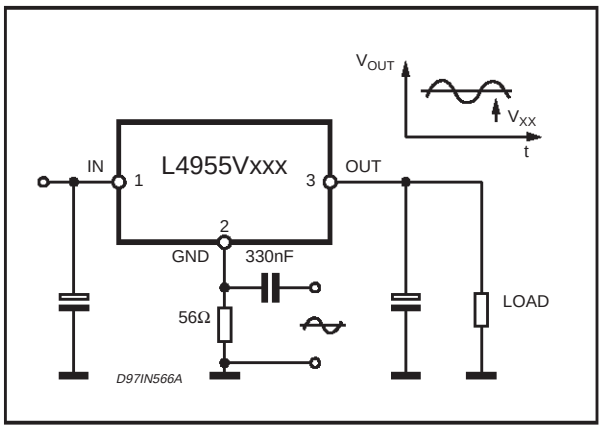
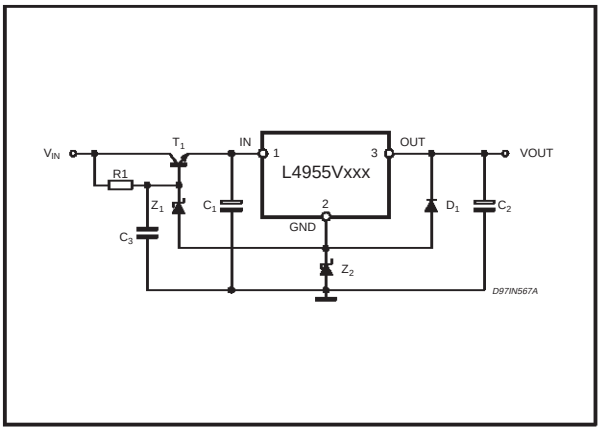


Figure 42.



HIGH INPUT AND OUTPUT VOLTAGE REGULATOR

In Fig. 42 it is shown a solution to applications, which require input and output voltages high than the device allowable ones.

The high input voltage is reduced by the Vceon of a npn power transistor. The current target of the application must take into account the dissipated power of this transistor.

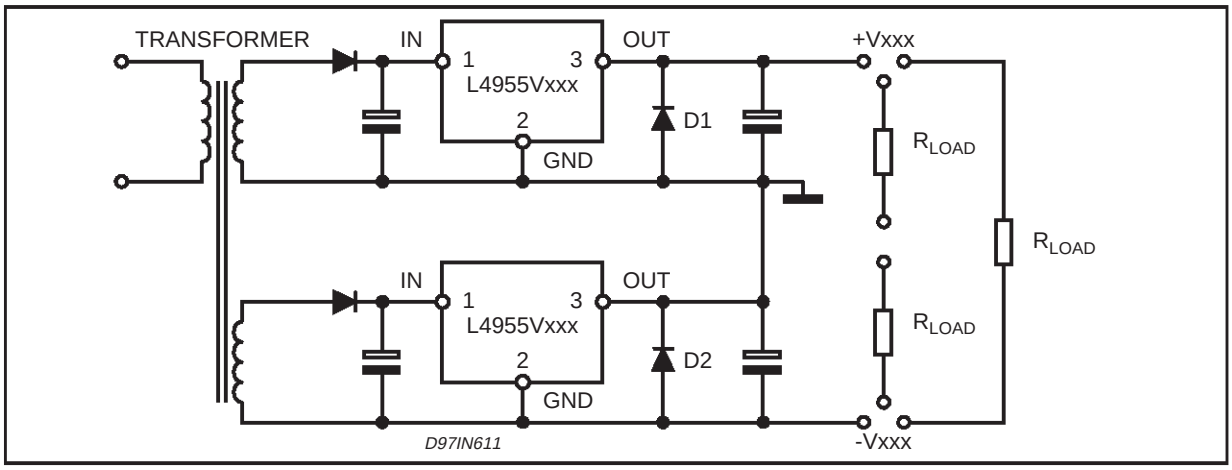
The high output voltage is obtained with the diode zener Z_2, which increases the output voltage of Vz. The diode D1 provides output short-circuit protection.

POSITIVE AND NEGATIVE POWER SUPPLY

Positive and negative power supply can be obtained in the following Fig. 43.

If the Rload is connected between +Vxx and -Vxx, and if one regulators starts ealier than the other one, the output voltage of the slower one becomes negative. The protection diodes D1, D2 are used to reduce the negative voltage avoiding the device latch-up.

Figure 43.



THERMAL DESIGN

The target of this thermal design is to dimension the correct heatsink requirements. The design needs the following parameters of the application:

- Maximum Input Voltage, Vin
- Minimum Output Voltage, Vout
- Maximum Output Current, Iout
- Maximum Ambient Temperature, Tamb

The heatsink thermal resistance has to be chosen so that the junction temperature of the device, in condition of maximum power dissipation expected for the application, is less than 125°C.

The maximum power which can be dissipated in the application, P_d, is given by :

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT}$$

The internal power consumption caused by the quiescent current can be neglected : in the worst case (Vin = 22V and Iq = 3mA) the power dissipation is only 66mW.

In short circuit condition, the fixed current limitation with its foldback characteristic limits the power dissipation but the dissipated power can reach higher values than in the Pd formula.

It happens if :

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} < V_{IN} \cdot I_{FOLDBACK}$$

In this case the thermal shutdown function ensures that the junction temperature will be maintained below 125°C. The power dissipation in overload condition can be higher than in short circuit condition if Vin > (0.8Vout Imax) / (Imax - $I_{FOLDBACK}$).

A simplified thermal model , which does not describe the transients phenomenon is showed in Fig. 44.

So we have:

$$T_J = P_D \cdot (R_{THJ\text{-}C} + R_{THS}) + T_A$$

Where :

$$R_{THS} = R_{THC\text{-}S} + R_{THS\text{-}A}$$

is the heatsink thermal resistance which is composed of the thermal resistance between case and heatsink and between heatsink and ambient.

The, $R_{thj\text{-}c}$, thermal resistance junction-case, is 2.5°C/W.

The heatsink can be dimensioned with the following formula :

$$R_{THS} = \frac{T_J - T_A}{P_D} - R_{THJ-C}$$

For example a typical application for the L4955 is :

Vin = 6.5V
Vout = 5V
Iout = 5A
Tamb = 50°C

If we want to maintain $T_J \cong 100°C$, we can use a heatsink with : $R_{THS} \cong 4°C/W$.

Figure 44.