NEC
NEC Electronics Inc.

μPD431132L
32,768 x 32-Bit CMOS Synchronous Static RAM: With Burst Counter; 3.3-Volt Power

Preliminary Information

August 1994

Description

The μPD431132L is a 32,768-word by 32-bit synchronous static RAM fabricated with advanced CMOS technology. Its unique peripheral circuits and N-channel memory cells make the μPD431132L suitable in low-voltage applications requiring high speed, high density, and wide bit configurations such as cache and buffer memory.

Features

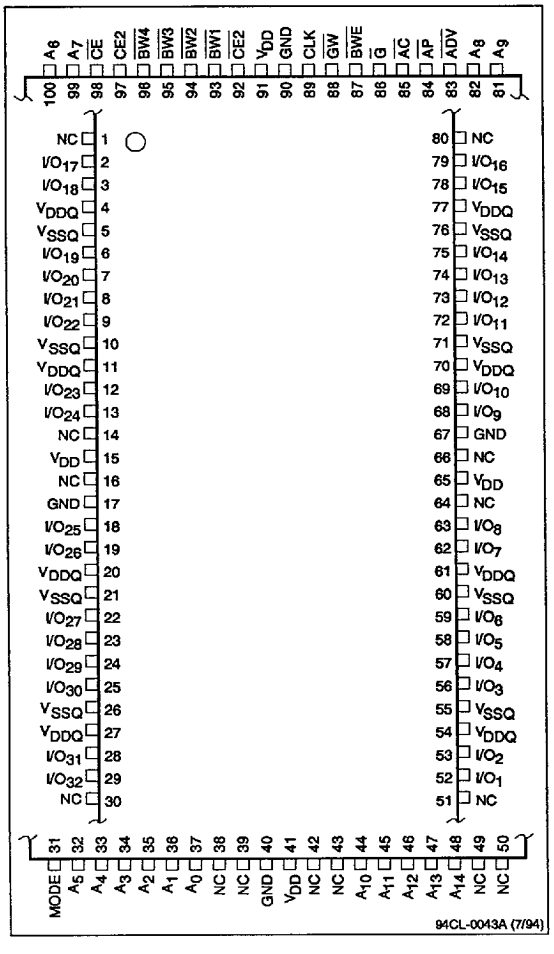
- Single +3.3-volt power supply
- Synchronous operation
- Burst read/write selectable at MODE pin
  - — Pentium™ burst sequence
  - — Linear burst sequence
- Fully registered inputs
- Registers triggered off positive clock edge
- LVTTL-compatible inputs and outputs
- 5-volt tolerant I/O
- Common I/O using three-state outputs
- Three chip enables for easy depth expansion: pins $\overline{CE}$, $\overline{CE2}$, CE2
- Byte write enables: pins $\overline{BW1}$ - $\overline{BW4}$ and $\overline{BWE}$
- Global write enable: pin $\overline{GW}$
- Asynchronous output enable: pin $\overline{G}$
- Fast clock access time
  - — 10 ns at 60 MHz
  - — 12 ns at 50 MHz
  - — 14 ns at 50 MHz
- 100-pin TQFP package

Ordering Information

Part Number	Access Time (max)	Package
μPD431132LGF-10	10 ns	100-pin TQFP
GF-12	12 ns	
GF-14	14 ns	

Pin Configuration

100-Pin TQFP



Pentium is a trademark of Intel Corporation.

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Pin Identification

Symbol	Function
A_0 - A_{14}	Address input
I/O_1 - I/O_{32}	Data input and output
$\overline{ADV}$	Burst address advance
$\overline{AC}$	Controller address status
$\overline{AP}$	Processor address status
$\overline{CE}$, $\overline{CE2}$, CE2	Chip enable
$\overline{BW1}$ - $\overline{BW4}$, $\overline{BWE}$	Byte write enable
$\overline{G}$	Output enable
$\overline{GW}$	Global write
MODE	Mode select
CLK	System clock input
V_{DD}	+3.3-volt power
GND	Ground
V_{DDQ}	Power for outputs
V_{SSQ}	Ground for outputs

Pentium Burst Sequence † *

External address	A_{14} - A_2, A_1, A_0
1st burst address	A_{14} - A_2, A_1, $\overline{A_0}$
2nd burst address	A_{14} - A_2, $\overline{A_1}$, A_0
3rd burst address	A_{14} - A_2, $\overline{A_1}$, $\overline{A_0}$

† MODE pin = NC or V_{DD}

* The burst sequence wraps around to its initial state upon completion.

Linear Burst Sequence † *

External address	A, 0, 0	A, 0, 1	A, 1, 0	A, 1, 1
1st burst address	A, 0, 1	A, 1, 0	A, 1, 1	A, 0, 0
2nd burst address	A, 1, 0	A, 1, 1	A, 0, 0	A, 0, 1
3rd burst address	A, 1, 1	A, 0, 0	A, 0, 1	A, 1, 0

† MODE pin = GND

* The burst sequence wraps around to its initial state upon completion. A = A_{14} - A_2

Synchronous Truth Table

Operation	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	† Write	CLK	Address
Deselected	H	X	X	X	L	X	X	L-H	N/A
	L	X	L	L	X	X	X	L-H	N/A
	L	H	X	L	X	X	X	L-H	N/A
	L	X	L	H	L	X	X	L-H	N/A
	L	H	X	H	L	X	X	L-H	N/A
Read Cycle									
Begin burst	L	L	H	L	X	X	X	L-H	External
Begin burst	L	L	H	H	L	X	H	L-H	External
Continue burst	X	X	X	H	H	L	H	L-H	Next
Continue burst	H	X	X	X	H	L	H	L-H	Next
Suspend burst	X	X	X	H	H	H	H	L-H	Current
Suspend burst	H	X	X	X	H	H	H	L-H	Current
Write Cycle									
Begin burst	L	L	H	H	L	X	L	L-H	External
Continue burst	X	X	X	H	H	L	L	L-H	Next
Continue burst	H	X	X	X	H	L	L	L-H	Next
Suspend burst	X	X	X	H	H	H	L	L-H	Current
Suspend burst	H	X	X	X	H	H	L	L-H	Current

† In the Write column, L means one or more byte write enables ($\overline{BW1}$ - $\overline{BW4}$) and $\overline{BWE}$ are low, or $\overline{GW}$ is low. H means all byte write enables are high.

* X means don't care.

Asynchronous Truth Table

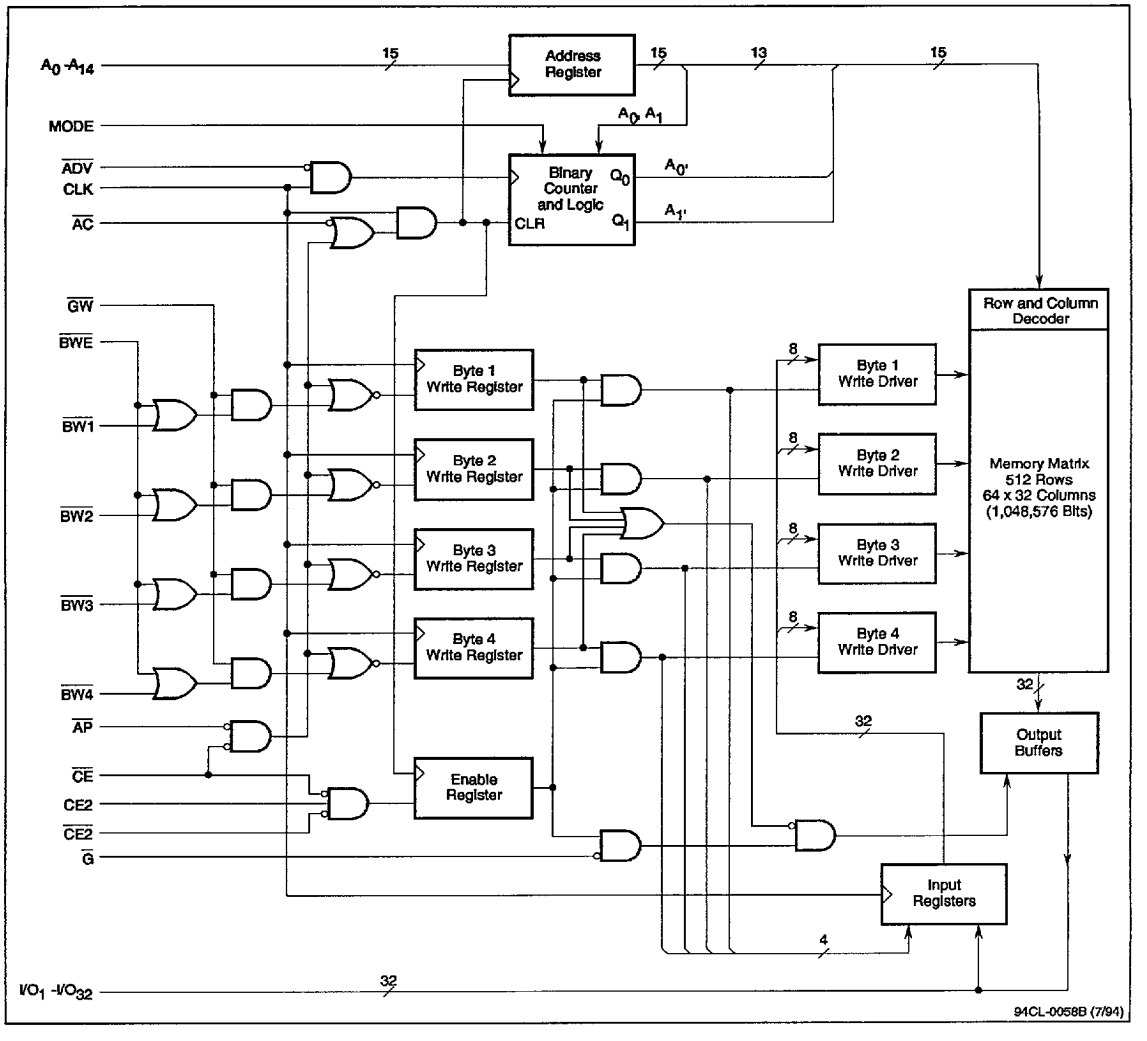
Operation	$\overline{G}$	I/O
Read Cycle	L	D_{OUT}
	H	High-Z
Write Cycle	X	D_{IN}, High-Z
Deselected	X	High-Z

X means don't care

Partial Truth Table for Write Enables

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read Cycle	H	H	X	X	X	X
	H	L	H	H	H	H
Write Cycle						
Byte 1 only	H	L	L	H	H	H
All bytes	H	L	L	L	L	L
All bytes	L	X	X	X	X	X

Block Diagram



Absolute Maximum Ratings

*Supply voltage, V_{DD}	−0.5 to +4.6 V
*Input voltage, V_{IN}	−0.5 to +6.0 V
*Input/Output voltage, $V_{I/O}$	−0.5 to +6.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

* − 2.5 V minimum (pulse width = 3 ns)

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDQ}	3.1	3.3	3.5	V
*Input voltage, low	V_{IL}	− 0.5		0.8	V
Input voltage, high	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		70	°C

*− 2.0 V minimum (pulse width = 2 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and $V_{I/O}$ = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		4	pF
Input/output capacitance	$C_{I/O}$		7	pF

Note: Capacitance is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{DD} = +3.3 V ± 0.2 V; minimum transverse air flow = 2.5 meters/second

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{DD}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{DD}; output disabled
Operating supply current	I_{DD}			210	mA	Device selected; f = 60 MHz; $I_{I/O}$ = 0; (Note 1)
	I_{DD1}			45	mA	Suspend read cycle; f = 60 MHz; $I_{I/O}$ = 0; (Notes 1, 2)
Standby supply current	I_{SB}			20	mA	Device deselected; all inputs static; f = 0 MHz; (Note 1)
	I_{SB1}			2	mA	Device deselected; all inputs static; f = 0 MHz, (Note 3)
	I_{SB2}			50	mA	Device deselected; f = 60 MHz; (Note 1)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4 mA

Notes:

(1) $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$

(2) $\overline{AC}$, $\overline{AP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BWs} \geq V_{IH}$

(3) $V_{IN} \leq 0.2$ V or $\geq V_{DD} - 0.2$ V

AC Characteristics, Read and Write Cycle

T_A = 0 to +70°C; V_{DD} = +3.3 V ±0.2 V

Parameter	Symbol		-10 (60 MHz)		-12 (50 MHz)		-14 (50 MHz)		Unit
	Standard	Alternate	Min	Max	Min	Max	Min	Max	
Cycle time	t_{KHKH}	t_{CYC}	16.7	—	20	—	20	—	ns
Clock access time	t_{KHQV0}	t_{CD0}	—	10	—	12	—	14	ns
	t_{KHQV}	t_{CD}	—	11	—	13	—	15	ns
Output enable to output valid	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns
Clock high to output active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	ns
Clock high to output change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns
Output enable to output active	t_{GLQX}	t_{OLZ}	2	—	2	—	2	—	ns
Output disable to output high-Z	t_{GHQZ}	t_{OHZ}	—	5	—	6	—	7	ns
Clock high to output high-Z	t_{KHQZ}	t_{CZ}	—	5	—	6	—	7	ns
Clock high pulse width	t_{KHKL}	t_{CH}	4	—	4	—	4	—	ns
Clock low pulse width	t_{KLKH}	t_{CL}	4	—	4	—	4	—	ns
Setup time									
Address	t_{AVKH}	t_{AS}	3	—	3	—	3	—	ns
Address status	t_{ADSVKH}	t_{SS}							
Data in	t_{DVKH}	t_{DS}							
Write enable	t_{WVKH}	t_{WS}							
Address advance	t_{ADVVKH}								
Chip enable	t_{EVKH}								
Hold time									
Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	ns
Address status	t_{KHADSX}	t_{SH}							
Data in	t_{KHDX}	t_{DH}							
Write enable	t_{KHWX}	t_{WH}							
Address advance	t_{KHADVX}								
Chip enable	t_{KHEX}								

Test Conditions:

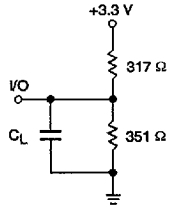
(1) Input pulse: GND to 3 V with rise/fall times 1.5 ns.

(2) Timing reference level: 1.5 V.

(3) Output load: figure 1.

(4) Minimum transverse air flow: 2.5 meters/second.

Figure 1. Output Load



Parameter (t_{XX})	Output Load
DC1, DC2, OLZ, OHZ, CZ	C_L = 5 pF (including scope and jig)
CD0	No output load; values are simulated
Others	C_L = 30 pF (including scope and jig)

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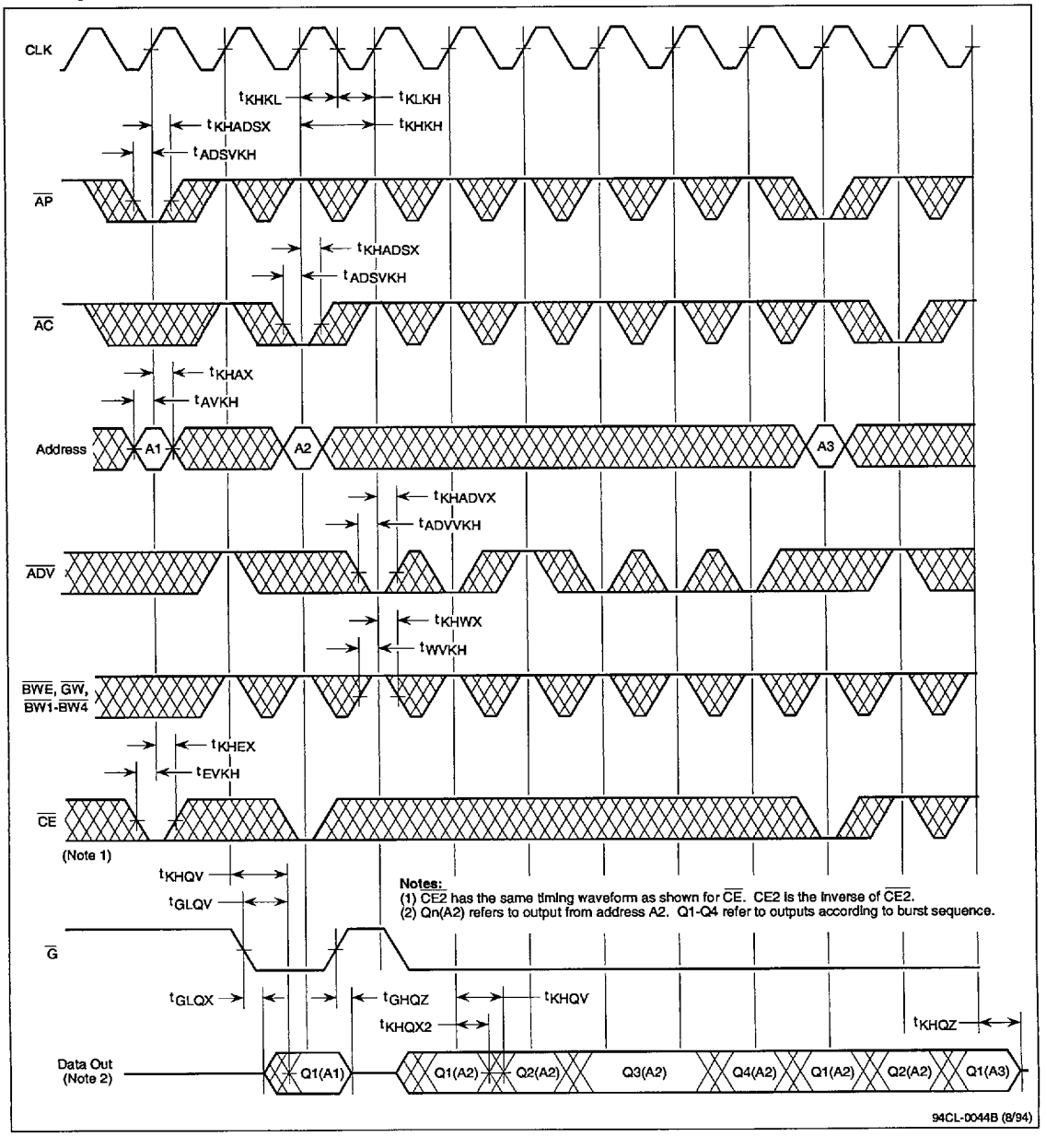
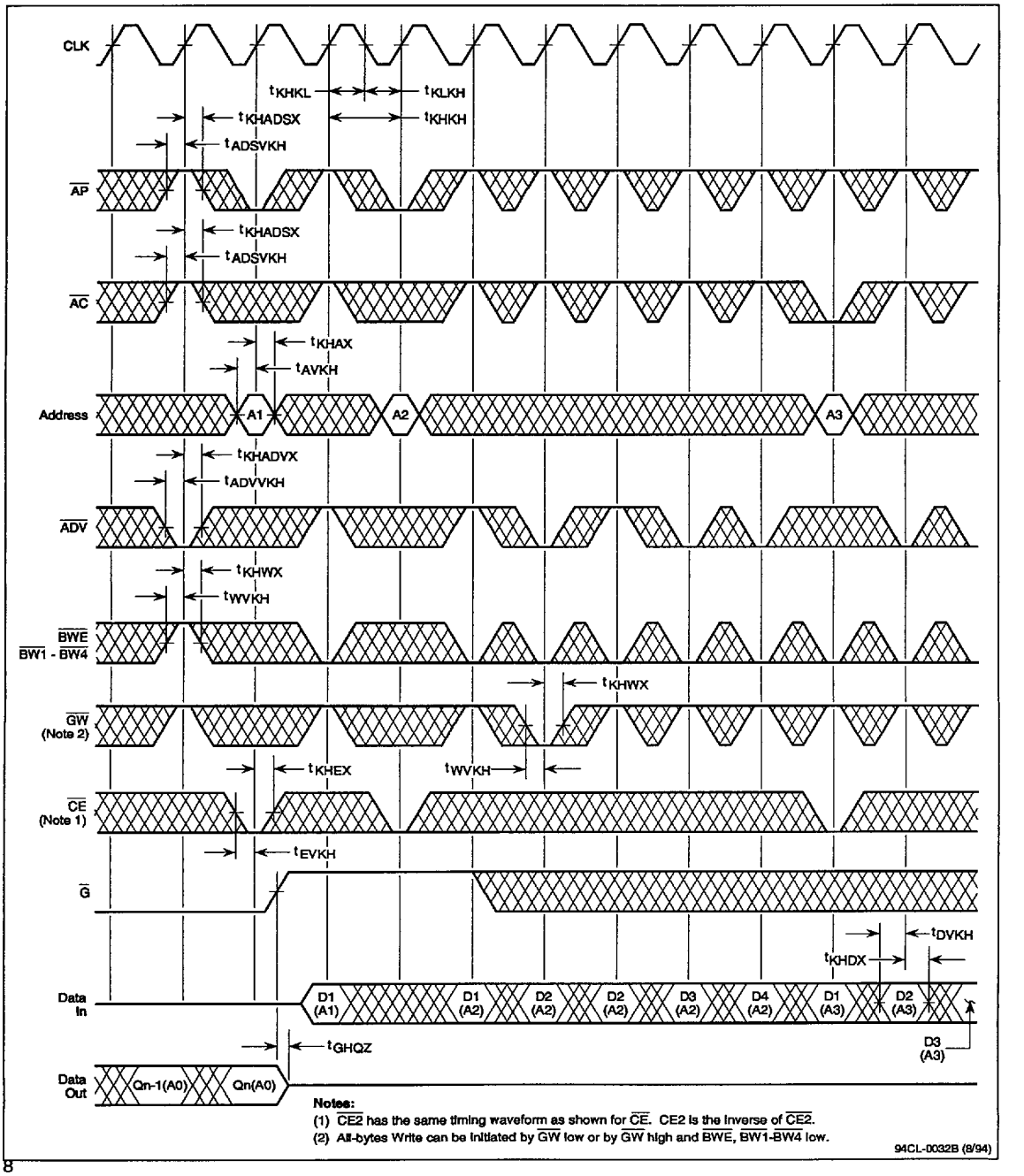
Timing Waveforms

Read Cycle



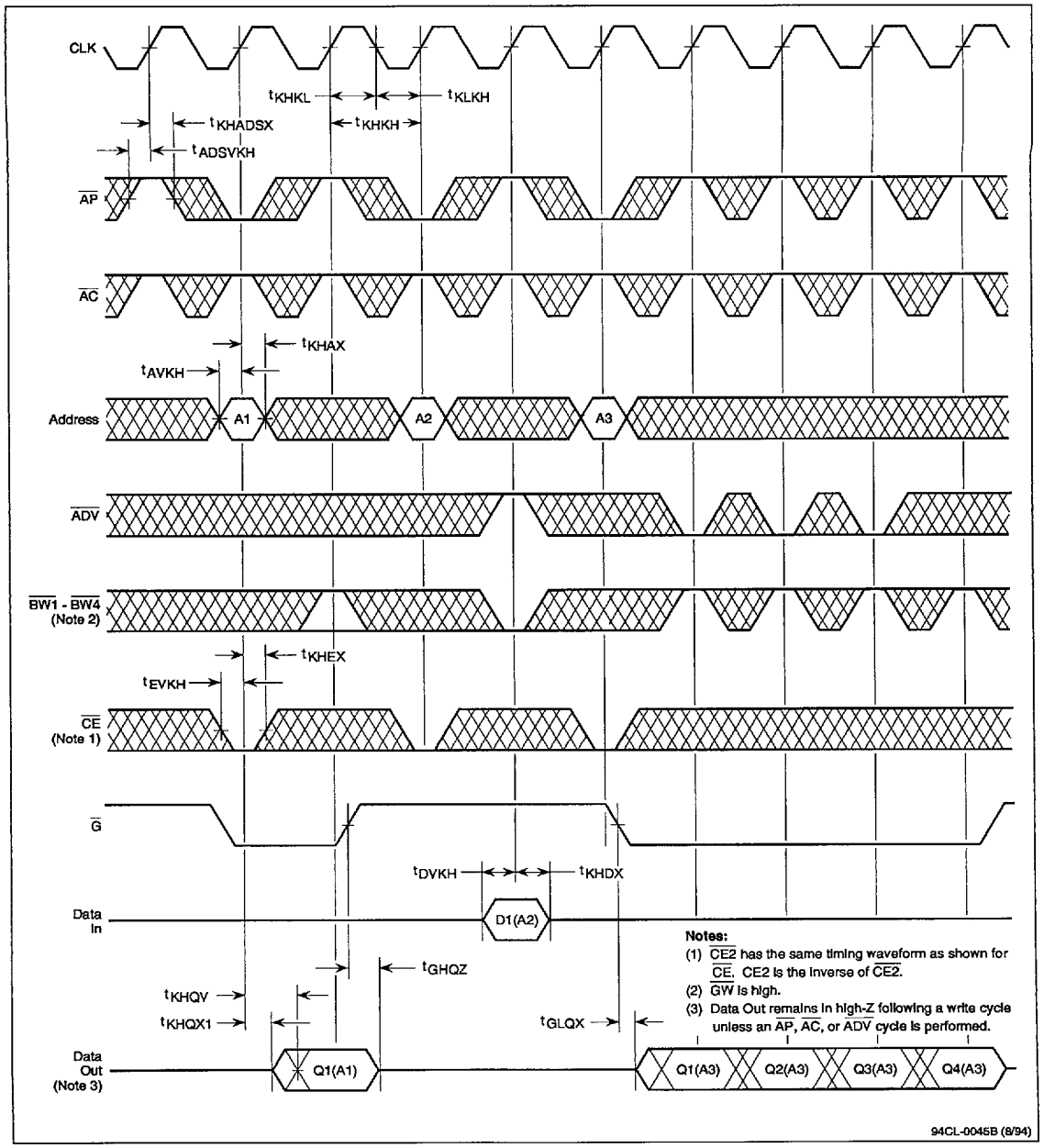
Timing Waveforms (cont)

Write Cycle



Timing Waveforms (cont)

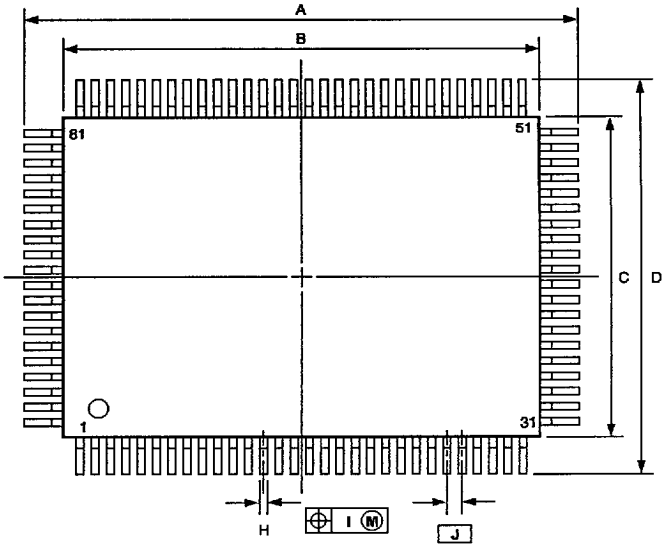
Read/Write Cycle

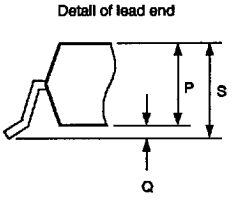


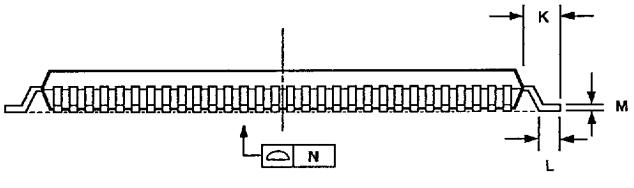
Package Drawing

100-Pin TQFP

Item	Millimeters	Inches
A	22.0 ±0.3	.866 ±.012
B	20.0 ±0.2	.787 $^{+.009}_{-.008}$
C	14.0 ±0.2	.551 $^{+.009}_{-.008}$
D	17.6 ±0.4	.693 ±.016
H	0.32 $^{+0.08}_{-0.07}$	.013 $^{+.003}_{-.003}$
I	0.13	.005
J	0.65 (TP)	.026 (TP)
K	1.0 ±0.2	.039 ±.008
L	0.5 ±0.2	.020 $^{+.009}_{-.008}$
M	0.145 typ	.006 typ
N	0.1 typ	.004 typ
P	1.4 typ	.055 typ
Q	0.1 ±0.05	.004 ±.002
S	1.7 max	.067 max







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