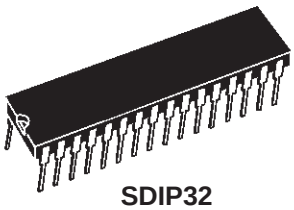
ST72260G, ST72262G, ST72264G

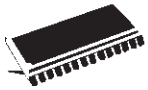
8-BIT MCU WITH FLASH OR ROM MEMORY, ADC, TWO 16-BIT TIMERS, I^2C, SPI, SCI INTERFACES

DATA BRIEFING

- **Memories**
  - 4 K or 8 Kbytes Program memory: ROM or Single voltage extended Flash (XFlash) with read-out protection write protection and In-Circuit Programming and In-Application Programming (ICP and IAP)
  - 256 bytes RAM
- **Clock, Reset and Supply Management**
  - Enhanced reset system
  - Enhanced low voltage supply supervisor (LVD) with 3 programmable levels and auxiliary voltage detector (AVD) with interrupt capability for implementing safe power-down procedures
  - Clock sources: crystal/ceramic resonator oscillators, internal or external RC oscillator, clock security system and bypass for external clock
  - PLL for 2x frequency multiplication
  - Clock-out capability
  - 4 Power Saving Modes: Halt, Active Halt,Wait and Slow
- **Interrupt Management**
  - Nested interrupt controller
  - 10 interrupt vectors plus TRAP and RESET
  - 22 external interrupt lines (on 2 vectors)
- **22 I/O Ports**
  - 22 multifunctional bidirectional I/O lines
  - 20 alternate function lines
  - 8 high sink outputs
- **3 Timers**
  - Configurable watchdog timer
  - Two 16-bit timers with: 2 input captures, 2 output compares, external clock input on one timer, PWM and Pulse generator modes



SDIP32



SO28

- **3 Communications Interfaces**
  - SPI synchronous serial interface
  - I^2C multimaster interface
  - SCI asynchronous serial interface (LIN compatible)
- **1 Analog peripheral**
  - 10-bit ADC with 6 input channels
- **Instruction Set**
  - 8-bit data manipulation
  - 63 basic instructions
  - 17 main addressing modes
  - 8 x 8 unsigned multiply instruction
  - True bit manipulation
- **Development Tools**
  - Full hardware/software development package

Device Summary

Features	ST72260G1	ST72262G1	ST72262G2	ST72264G1
Program memory - bytes	4K	4K	8K	8K
RAM (stack) - bytes	256 (128)			
Peripherals	Watchdog timer, Two16-bit timers, SPI	Watchdog timer, Two 16-bit timers, SPI, ADC	Watchdog timer, Two 16-bit timers, SPI, ADC	Watchdog timer, Two 16-bit timers, SPI, SCI, I^2C, ADC
Operating Supply	2.4 V to 5.5 V			
CPU Frequency	Up to 8 MHz (with oscillator up to 16 MHz) PLL 4/8 Mhz			
Operating Temperature	-40° C to +85° C			
Packages	SO28 / SDIP32			

Rev. 1.4

This is preliminary information on a new product now in development. Details are subject to change without notice.

1 INTRODUCTION

The ST72260G, ST72262G and ST72264G devices are members of the ST7 microcontroller family. They can be grouped as follows :

– ST72264G devices are designed for mid-range applications with ADC, I^2C and SCI interface capabilities.

– ST72262G devices target the same range of applications but without I^2C interface or SCI.

– ST72260G devices are for applications that do not need ADC, I^2C peripherals or SCI.

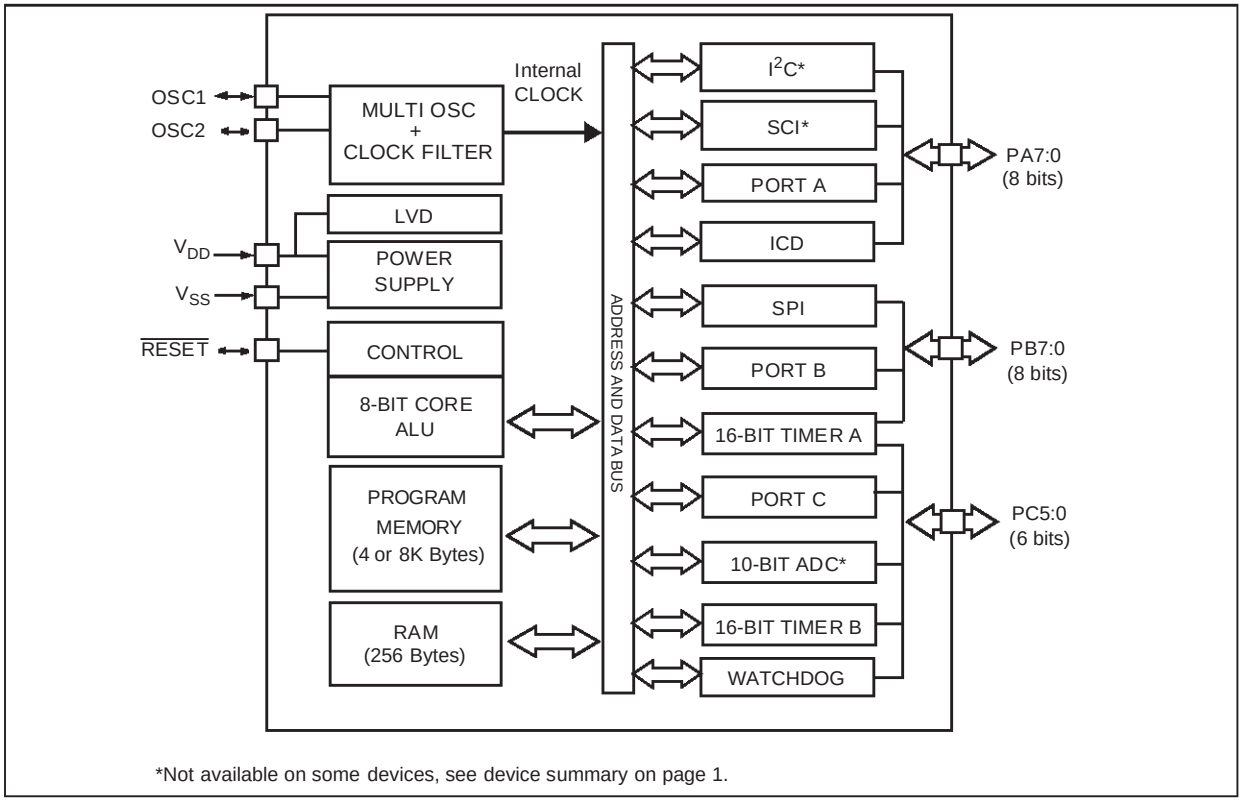
All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

The ST72F260G, ST72F262G, and ST72F264G versions feature single-voltage FLASH memory with byte-by-byte In-Circuit Programming (ICP) capabilities.

Under software control, all devices can be placed in WAIT, SLOW, Active-HALT or HALT mode, reducing power consumption when the application is in idle or stand-by state.

The enhanced instruction set and addressing modes of the ST7 offer both power and flexibility to software developers, enabling the design of highly efficient and compact application code. In addition to standard 8-bit data management, all ST7 microcontrollers feature true bit manipulation, 8x8 unsigned multiplication and indirect addressing modes.

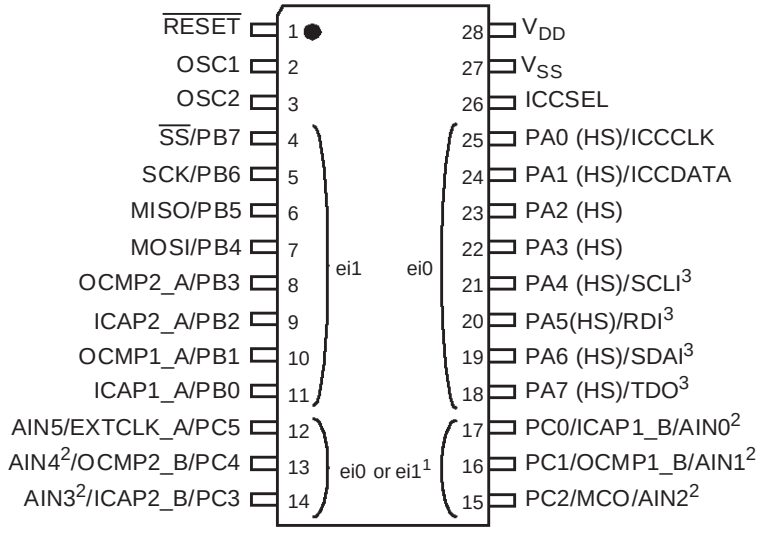
Figure 1. General Block Diagram



*Not available on some devices, see device summary on page 1.

2 PIN DESCRIPTION

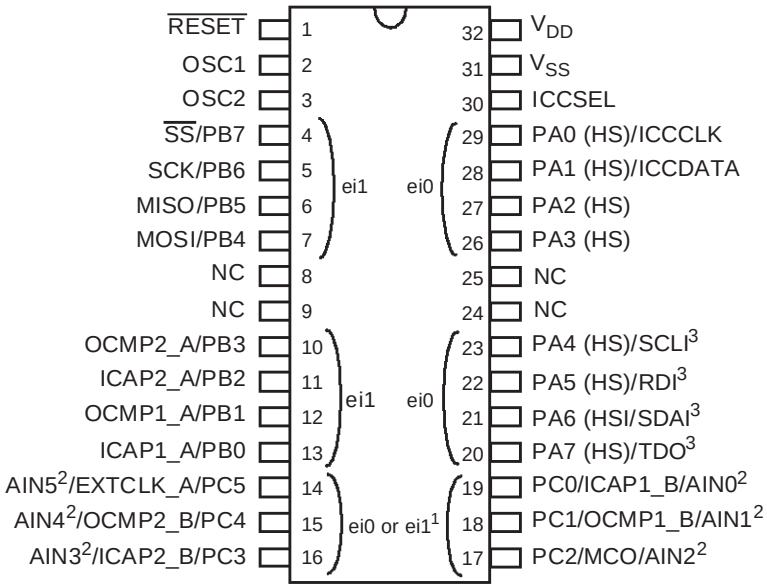
Figure 2. 28-Pin SO Package Pinout



1 Configurable by option byte
2 Alternate function not available on ST72260
3 Alternate function not available on ST72260 and ST72262

(HS) 20mA high sink capability
eiX associated external interrupt vector

Figure 3. 32-Pin SDIP Package Pinout



1 Configurable by option byte
2 Alternate function not available on ST72260
3 Alternate function not available on ST72260 and ST72262

(HS) 20mA high sink capability
eiX associated external interrupt vector

PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for Table 1**:**

Type: I = input, O = output, S = supply

Input level: A = Dedicated analog input

In/Output level: C_T= CMOS 0.3 V_{DD}/0.7 V_{DD} with input trigger

Output level: HS = 20 mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt [1], ana = analog

– Output: OD = open drain [2], PP = push-pull

The RESET configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin n°		Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
						Input				Output			
SDIP32	SO28			Input	Output	float	wpu	int	ana	OD	PP		
1	1	$\overline{\text{RESET}}$	I/O	C_T			X			X		Top priority non maskable interrupt (active low)	
2	2	OSC1 [3]	I									External clock input or Resonator oscillator inverter input or resistor input for RC oscillator	
3	3	OSC2 [3]	O									Resonator oscillator inverter output or capacitor input for RC oscillator	
4	4	PB7/$\overline{\text{SS}}$	I/O	C_T		**X**	ei1			X	X	**Port B7**	SPI Slave Select (active low)
5	5	PB6/SCK	I/O	C_T		**X**	ei1			X	X	**Port B6**	SPI Serial Clock
6	6	PB5/MISO	I/O	C_T		**X**	ei1			X	X	**Port B5**	SPI Master In/ Slave Out Data
7	7	PB4/MOSI	I/O	C_T		**X**	ei1			X	X	**Port B4**	SPI Master Out / Slave In Data
8		NC	Not Connected										
9		NC											
10	8	PB3/OCMP2_A	I/O	C_T		**X**	ei1			X	X	**Port B3**	Timer A Output Compare 2
11	9	PB2/ICAP2_A	I/O	C_T		**X**	ei1			X	X	**Port B2**	Timer A Input Capture 2
12	10	PB1 /OCMP1_A	I/O	C_T		**X**	ei1			X	X	**Port B1**	Timer A Output Compare 1
13	11	PB0 /ICAP1_A	I/O	C_T		**X**	ei1			X	X	**Port B0**	Timer A Input Capture 1
14	12	PC5/EXTCLK_A/AIN5	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C5**	Timer A Input Clock or ADC Analog Input 5
15	13	PC4/OCMP2_B/AIN4	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C4**	Timer B Output Compare 2 or ADC Analog Input 4
16	14	PC3/ ICAP2_B/AIN3	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C3**	Timer B Input Capture 2 or ADC Analog Input 3
17	15	PC2/MCO/AIN2	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C2**	Main clock output (f_{CPU}) or ADC Analog Input 2
18	16	PC1/OCMP1_B/AIN1	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C1**	Timer B Output Compare 1 or ADC Analog Input 1
19	17	PC0/ICAP1_B/AIN0	I/O	C_T		**X**	ei0/ei1	X		X	X	**Port C0**	Timer B Input Capture 1 or ADC Analog Input 0

Pin n°		Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
						Input				Output			
SDIP32	SO28			Input	Output	float	wpu	int	ana	OD	PP		
20	18	PA7/TDO	I/O	C_T	HS	**X**	ei0			X	X	**Port A7**	SCI output
21	19	PA6/SDAI	I/O	C_T	HS	**X**		ei0		T		**Port A6**	I^2C DATA
22	20	PA5 /RDI	I/O	C_T	HS	**X**	ei0			X	X	**Port A5**	SCI input
23	21	PA4/SCLI	I/O	C_T	HS	**X**		ei0		T		**Port A4**	I^2C CLOCK
24		NC	Not Connected										
25		NC											
26	22	PA3	I/O	C_T	HS	**X**	ei0			X	X	**Port A3**	
27	23	PA2	I/O	C_T	HS	**X**	ei0			X	X	**Port A2**	
28	24	PA1/ICCDATA	I/O	C_T	HS	**X**	ei0			X	X	**Port A1**	In Circuit Communication Data
29	25	PA0/ICCCLK	I/O	C_T	HS	**X**	ei0			X	X	**Port A0**	In Circuit Communication Clock
30	26	ICCSEL	I	C_T		**X**						ICC mode pin, must be tied low	
31	27	V_{SS}	S									Ground	
32	28	V_{DD}	S									Main power supply	

Notes:

1. In the interrupt input column, “eiX” defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is a pull-up interrupt input, otherwise the configuration is a floating interrupt input. Port C is mapped to ei0 or ei1 by option byte.

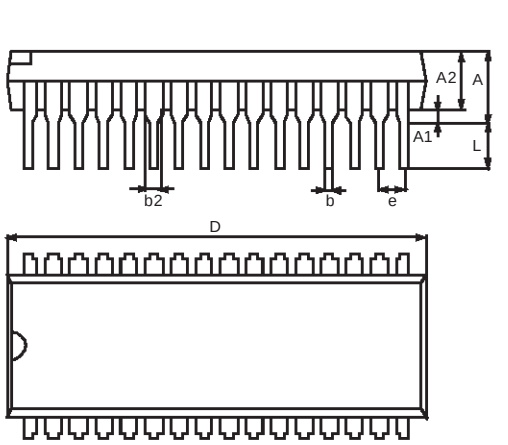
2. In the open drain output column, “T” defines a true open drain I/O (P-Buffer and protection diode to V_{DD} are not implemented).

3. OSC1 and OSC2 pins connect a crystal or ceramic resonator, an external RC, or an external source to the on-chip oscillator.

3 PACKAGE CHARACTERISTICS

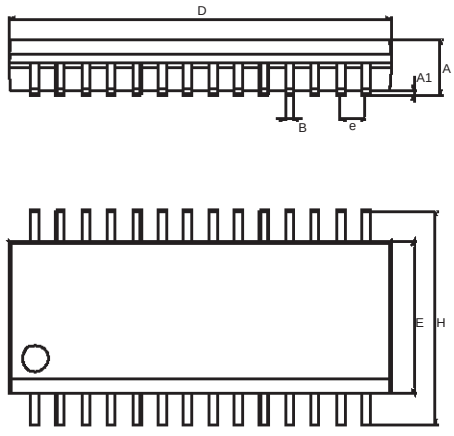
3.1 PACKAGE MECHANICAL DATA

Figure 4. 32-Pin Plastic Dual In-Line Package, Shrink 400-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.56	3.76	5.08	0.140	0.148	0.200
A1	0.51			0.020		
A2	3.05	3.56	4.57	0.120	0.140	0.180
b	0.36	0.46	0.58	0.014	0.018	0.023
b1	0.76	1.02	1.40	0.030	0.040	0.055
C	0.20	0.25	0.36	0.008	0.010	0.014
D	27.43		28.45	1.080	1.100	1.120
E	9.91	10.41	11.05	0.390	0.410	0.435
E1	7.62	8.89	9.40	0.300	0.350	0.370
e		1.78			0.070	
eA		10.16			0.400	
eB			12.70			0.500
eC			1.40			0.055
L	2.54	3.05	3.81	0.100	0.120	0.150
	Number of Pins					
N	32					

Figure 5. 28-Pin Plastic Small Outline Package, 300-mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	17.70		18.10	0.697		0.713
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
α	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of Pins					
N	28					

Notes:

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