MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX828

CTCSS/DCS/SelCall Processor

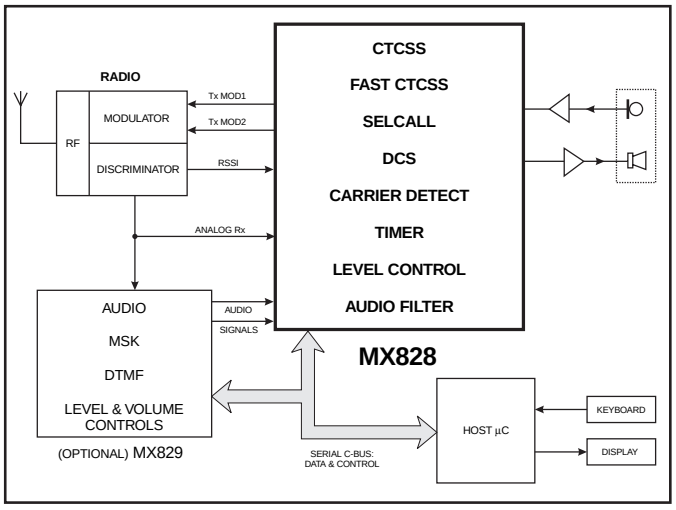
PRELIMINARY INFORMATION

Features

- **Fast CTCSS Detection**
- **Full Duplex CTCSS and SelCall**
- **Full 23/24 Bit DCS Codec**
- **SelCall Codec**
- **Non Predictive Tone Detection**
- **Low Power 3.3V/5.0V Operation**
- **Variable Gain Audio Filter**
- **Programmable:**
  - **Tone Decoder**
  - **Tone Encoder**
  - **Modulator Drivers**
  - **Comparator for RSSI**
- **Pin compatible with reduced function MX818**
- **Full control via 4-Wire Serial Interface**

Applications

- **Radio Systems Requiring Sub-Audible Signaling**
  - **Trunking Control**
  - **Selective Calling**
  - **Group Calling**
- **Increased Efficiency**
  - **Scanning Systems**
  - **Trunking Systems**



The MX828 is a low power SelCall, CTCSS, and DCS signal processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling, and Group Calling applications. The MX828 is full duplex and offers many advanced features to assist in the design of new Sub-Audible and in-band based systems. These include: a programmable tone decoder which may be set to respond to between 1 and 15 CTCSS or SelCall tones with minimum software intervention, a Fast/Predictive CTCSS detector that can respond to a single programmed tone in less than 60ms or provide an output if CTCSS tone is present at the detector input, two high resolution tone encoders that accurately generate CTCSS or SelCall tones, and a full 23/24 bit DCS encoder and decoder. The MX828 also provides a general purpose timer, a comparator with a programmable threshold, and a summing amplifier with two adjustable gain blocks to facilitate design integration and reduce part count.

The MX828 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP (MX828DS), 24-pin SOIC (MX828DW), and 24-pin PDIP (MX828P).

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1. Block Diagram

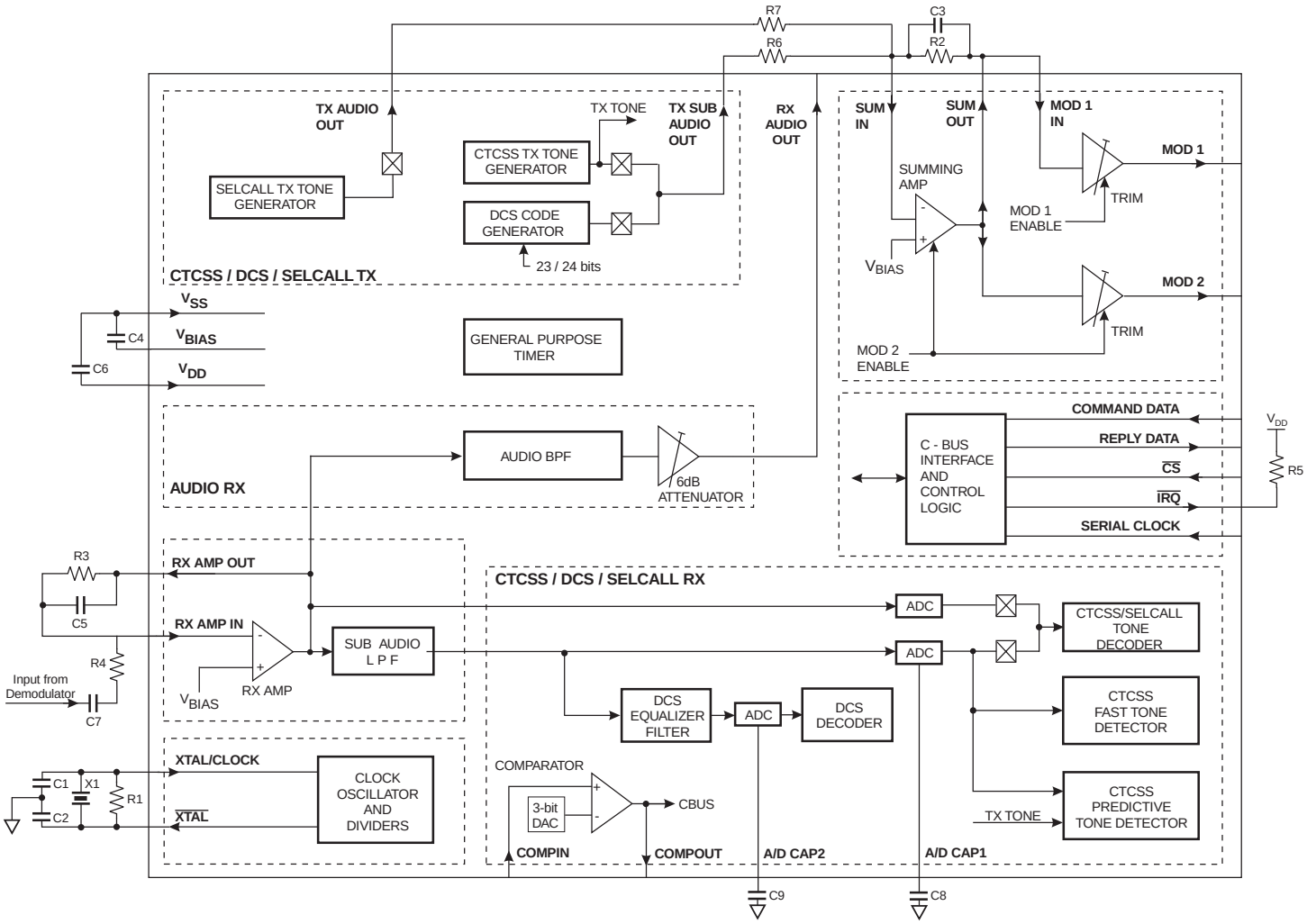


Figure 1: Block Diagram

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The “C-BUS” serial clock input. This clock, produced by the µC, is used for timing transfer of commands and data to and from the device. (Figure 4).
4	COMMAND DATA	input	The “C-BUS” serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. (Figure 4).
5	REPLY DATA	output	The “C-BUS” serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This 3-state output is held at high impedance when not sending data to the µC. (Figure 4).
6	$\overline{\text{CS}}$	input	The “C-BUS” data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal (Figure 4).
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	COMPOUT	output	The output of the comparator.
9	COMPIN	input	The input to the comparator.
10	A/D CAP 1	output	An internal reference voltage for the CTCSS A/D. Bypassed to V_{SS} with an external capacitor.
11	A/D CAP 2	output	An internal reference voltage for the DCS A/D. Bypassed to V_{SS} with an external capacitor.
12	V_{SS}	Power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	Output of the Rx input amplifier
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	TX AUDIO OUT	output	Output of the SelCall tone generator.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier.
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS or DCS Tx tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

Table 1: Signal List

3. External Components

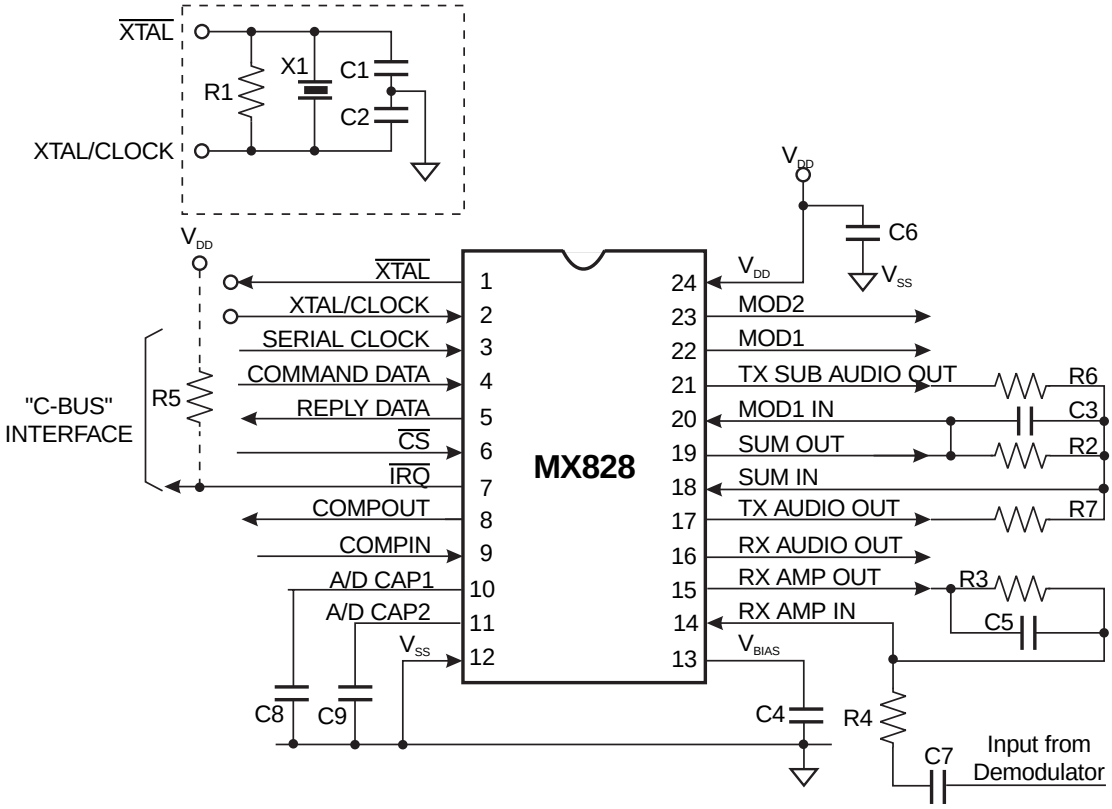


Figure 2: Recommended External Components

R1		1MΩ	±5%
R2		100kΩ	±10%
R3		100kΩ	±10%
R4	Note 2		±10%
R5		22kΩ	±10%
R6	Note 1		±10%
R7	Note 1		±10%
C1		22pF	±20%
C2		22pF	±20%

C3		100pF	±20%
C4		0.1µF	±20%
C5		100pF	±20%
C6		0.1µF	±20%
C7	Note 2		±20%
C8		0.1µF	±20%
C9		1.0µF to 3.3µF	±20%
X1	Note 3	4.032MHz	±100ppm

Table 2: External Components

External Components Notes:

1. R2, R6, R7 and C3 form the gain components for the Summing Amplifier. R6 and R7 should be chosen as required from the system specification, using the following formula:

   $$\text{Tx Sub Audio Gain} = -\frac{R2}{R6} \qquad \text{Tx Audio Gain} = -\frac{R2}{R7}$$

2. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

   $$\text{Gain} = -\frac{R3}{R4}$$

   C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX828 is a signaling encoder/decoder for use in land mobile radio equipment, see Figure 1. The transmitter section of the MX828 has independently controllable tone generators for sub-audio (CTCSS) and inband (SelCall) signaling. Also featured is a DCS code generator, which may be used in place of the CTCSS tone generator.

The receiver section of the MX828 has a fast/predictive CTCSS tone detector which operates in parallel with a DCS decoder and a CTCSS/SelCall tone decoder. The latter is switchable to perform either CTCSS or SelCall tone decoding of a user-programmable set of up to 15 tones. In the CTCSS mode it performs a more accurate (but slower) analysis of the tones detected by the fast/predictive CTCSS tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

Both the DCS transmit and receive bit rates are fixed at 134.4bps.

Other functions on the MX828 are a comparator with programmable threshold level, a general purpose timer and a summing amplifier with two adjustable gain blocks, which may be used for two point modulation, for example. All MX828 functions are controlled by an external µC over the “C-BUS” interface, a serial interface designed to reduce interference levels in radio equipment.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

				DATA BYTE(S)	
REGISTER NAME	**SECTION**	**HEX ADDRESS COMMAND**	**READ / WRITE**	**BYTE 1**	**BYTE 2**
General Reset	4.4.1	$01	W	none	none
Sub-Audio Control	4.4.2	$80	W	Refer to Bit Description	none
SelCall Sub-Audio Status	4.5 4.6.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.4.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.4.10	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
RX Tone Program	4.4.11	$84	W	1 of 15 possible Registers Select & Decode Frequencies	
DCS Code	4.4.4	$85	W	Byte 3 of 3	none
DCS Code	4.4.5	$86	W	Byte 2 of 3	none
DCS Code	4.4.6	$87	W	Byte 1 of 3	none
General Control	4.4.7	$88	W	Refer to Bit Description	none
Audio Control	4.4.12	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.4.8	$8B	W	Refer to Bit Description	none
SelCall TX	4.4.13 4.4.2 4.4.3	$8D	W	Specify TX SelCall Frequencies	
IRQ Mask	4.4.9	$8E	W	Refer to Bit Description	none
IRQ Flag	4.5 4.6.2	$8F	R	Refer to Bit Description	none

Table 3: Command Summary

4.1.2 Address/Commands

Instructions and data are transferred, via “C-BUS”, in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the MX828 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or

(ii) a status or Rx data reply (1 byte)

4.2 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SIGNALLING CONTROL	SUBAUDIO TX ENABLE	TONE DECODER ENABLE	FAST DETECT ENABLE	0	0	SELCALL TX ENABLE	0	DCS RX ENABLE
$82	SIGNALLING SET-UP	TONE DECODER BANDWIDTH MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	FAST CTCSS MODE DETECT/ PREDICTIVE	TONE DECODER MODE	SUBAUDIO TX MODE	DCS 23/24
$85	DCS BYTE 3	DCS BYTE 3 OPTIONAL MSB BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
$86	DCS BYTE 2	DCS BYTE 2 BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$87	DCS BYTE 1	DCS BYTE 1 BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$88	GENERAL CONTROL	BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD	MSB DAC BIT 2	DAC BIT 1	LSB DAC BIT 0	GP TIMER ENABLE	GP TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GP TIMER IRQ MASK	COMP 0 to 1 IRQ MASK	COMP 1 to 0 IRQ MASK	TONE IRQ MASK	CTCSS FAST IRQ MASK	0	DCS IRQ MASK
$9C	*Reserved for later use*								

Table 4: 8-bit Write Only Registers

4.3 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
	CTCSS TX/				CTCSS TX/FAST RX FREQUENCY				
$83	FAST RX	CTCSS (TX)	0	0	MSB				
	FREQUENCY (1)	NOTONE			BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/	CTCSS TX/FAST RX FREQUENCY							
	FAST RX								LSB
	FREQUENCY (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RX TONE	TONE ADDRESS				TONE FREQUENCY			
$84	PROGRAM	MSB			LSB	MSB			
	(1)	BIT 3	BIT 2	BIT 1	BIT 0	BIT 11	BIT 10	BIT 9	BIT 8
	RX TONE	TONE FREQUENCY							
	PROGRAM								LSB
	(2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	AUDIO				MOD 1				
$8A	CONTROL	0	0	MOD 1	MSB				LSB
	(1)			ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	AUDIO				MOD 2				
	CONTROL	0	0	MOD 2	MSB				LSB
	(2)			ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
					SELCALL TX TONE				
$8D	SELCALL TX	SELCALL	0	0	MSB				
	(1)	NOTONE			BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		SELCALL TX TONE							
	SELCALL TX								LSB
	(2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Table 5: 16-bit Write Only Registers

4.4 Write Only Register Description

4.4.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
SIGNALING CONTROL	$80	0	0	0	0	0	0	0	0
SELCALL & SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SIGNALING SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (2)		0	0	0	0	0	0	0	0
RX TONE PROGRAM (1)	$84	0	0	0	0	0	0	0	0
RX TONE PROGRAM (2)		0	0	0	0	0	0	0	0
DCS BYTE 3	$85	0	0	0	0	0	0	0	0
DCS BYTE 2	$86	0	0	0	0	0	0	0	0
DCS BYTE 1	$87	0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
SELCALL TX (1)	$8D	0	0	0	0	0	0	0	0
SELCALL TX (2)		0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

Table 6: GENERAL RESET (Hex address $01)

4.4.2 SIGNALING CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

SUBAUDIO TX ENABLE (Bit 7)	Bit 7 should be set to “1” to enable the CTCSS/DCS subaudio transmitter. The subaudio Tx type will depend on the state of the SUBAUDIO TX MODE (Bit 1 SIGNALING SET-UP Register $82).
TONE DECODER ENABLE (Bit 6)	Bit 6 should be set to “1” to enable the CTCSS/SelCall tone decoder or the DCS decoder. Note: See Bit 0 for DCS decoder operation. Bits 7 and 6 should not both be set to “1” when Bit 0 is set to “1” because the DCS function is half-duplex only.
CTCSS FAST DETECT ENABLE (Bit 5)	When this bit is "1", the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SIGNALING SET-UP Register, $82). When this bit is "0", both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled.
SELCALL TX ENABLE (Bit 2)	When this bit is "1" the SelCall transmitter is enabled. When this bit is "0" the SelCall transmitter is disabled and powersaved.

DCS RX ENABLE (Bit 0)	When this bit is "1", the DCS decoder is enabled. When this bit is "0" the DCS decoder is disabled. The DCS decoder and the subaudio (CTCSS or DCS) transmitter should not be enabled at the same time.
(Bits 4, 3, and 1)	Reserved for future use. These bits should be set to "0".

Table 7: SIGNALING CONTROL Register (Hex address $80)

4.4.3 SIGNALING SET-UP Register (Hex address $82)

This register is used to define the signaling parameters, as described below:

TONE DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS/SelCall tone decoder according to the table below:
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SIGNALING CONTROL Register, $80) is "1", this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to the table below: If the CTCSS FAST DETECT ENABLE bit is "0" then both modes are deselected.
TONE DECODER MODE (Bit 2)	When this bit is "1" the CTCSS/SelCall tone decoder is set to detect inband (SelCall) tones. When this bit is "0" the tone decoder is set to detect subaudio (CTCSS) tones.
SUBAUDIO TX MODE (Bit 1)	When this bit is "1" the subaudio transmitter will be set to transmit DCS signals, if enabled. When this bit is "0" the subaudio transmitter will be set to transmit CTCSS signals, if enabled.
DCS 23/24 (Bit 0)	When this bit is "1" the DCS transmitter and decoder are configured for a 23-bit code. When this bit is "0" they are configured for a 24-bit code.

Table 8: SIGNALING SET-UP Register (Hex address $82)

					BANDWIDTH	
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Will Decode**	**Will Not Decode**
Recommended for CTCSS	1	0	0	0	±1.1%	±2.4%
Recommended for CCIR	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%
	1	1	0	0	±2.0%	±3.5%
	1	1	0	1	±2.2%	±3.7%
Recommended for ZVEI	1	1	1	0	±2.5%	±4.0%
	1	1	1	1	±2.7%	±4.2%

Table 9: TONE DECODER BANDWIDTH

DETECT/PREDICTIVE Bit 3	**Function**
0	DETECT mode
1	PREDICTIVE mode

Table 10: FAST CTCSS MODE

4.4.4 DCS BYTE 3 Register (Hex address $85)

4.4.5 DCS BYTE 2 Register (Hex address $86)

4.4.6 DCS BYTE 1 Register (Hex address $87)

These three bytes set the code that is transmitted or received in the DCS mode. The LSB bit "0" of the DCS BYTE 1 is transmitted first and the last bit is the MSB bit 23 of DCS BYTE 3 in the 24-bit mode or bit 22 in the 23-bit mode. See Table 22 or refer to the latest version of ANSI/TIA/EIA - 603 specification and programming documentation for DCS standard 23-bit codes.

4.4.7 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below:

BPF ENABLE (Bit 7)	When this bit is "1" the audio band-pass filter is enabled. When this bit is "0" the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is "1" the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is "0" the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is "1" a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is "0" the output of the audio band-pass filter is not attenuated.
DAC (Bits 4, 3 and 2)	These three bits set the level of the digital to analogue converter that feeds the negative input of the comparator. The DAC can be set to one of eight levels equally spaced between V_{SS} and V_{BIAS}, not including V_{SS}, but including V_{BIAS}, i.e. with a 5V supply, the lowest level would be 312.5mV set by "000" in bits 2, 3 and 4 and the highest level would be 2.5V set by "111" in bits 2, 3 and 4.
TIMER ENABLE (Bit 1)	When this bit goes to a "1" the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is "0" the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is "1" the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is "0" the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from "1" to "0" while the timer is enabled then the timer will complete the present count before stopping.

Table 11: GENERAL CONTROL Register (Hex address $88)

4.4.8 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (1ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to "1". An interrupt is generated on the $\overline{IRQ}$ pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is "1" otherwise the GPT IRQ FLAG remains set to "1" and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is "1" then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is "0" then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with "0" will cause the timer circuitry to be disabled (i.e. powersaved).

4.4.9 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7 and 1)	Reserved for future use. These should be set to "0".
GPT IRQ MASK (Bit 6)	When this bit is set to "1" it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 5)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "0" to "1". When this bit is set to "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 4)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "1" to "0". When this bit is set to "0" the interrupt is masked.
TONE IRQ MASK (Bit 3)	When this bit is set to "1" it enables an interrupt that occurs when the TONE IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to "1" it enables an interrupt that occurs when the CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
DCS IRQ MASK (Bit 0)	When this bit is set to "1" it enables an interrupt that occurs when the DCS DECODE/NO DECODE FLAG (Bit 7, SELCALL & SUB-AUDIO STATUS Register $81) changes state. When this bit is set to "0" the interrupt is masked.

Table 12: IRQ MASK Register (Hex address $8E)

4.4.10 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, the bits 0 to 12 define the receive frequency which the fast predictive detector is looking for according to the formula below:

$$A = \frac{f_{XTAL}\,(Hz)}{16 \times f_{TONE}\,(Hz)}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, the bits 0 to 12 control the frequency of the transmitted CTCSS tones according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above. (i.e. Tx Tone = predictive tone).

When Bit 7 in byte (1) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT.

4.4.11 RX TONE PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. The two bytes are used to program the center frequencies of up to 15 tones in either the audio or sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<---------- N ---------->				<---------- R ---------->							
0	0	0	1												
0	0	1	0	N is the binary representation of the				R is the nearest 6-bit binary							
0	0	1	1	following decimal number (n):				representation of (r), where:							
0	1	0	0												
0	1	0	1												
0	1	1	0												
0	1	1	1	SUBAUDIO (CTCSS)				SUBAUDIO (CTCSS)							
1	0	0	0	$n = INT (948982 \times f_{TONE} / f_{XTAL})$				$r = ((237245/f_{XTAL}) - (n/(4 \times f_{TONE}))) \times 8400$							
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0	INBAND (SELCALL)				INBAND (SELCALL)							
1	1	0	1	$n = INT (83036 \times f_{TONE} / f_{XTAL})$				$r = ((20759/f_{XTAL}) - (n/(4 \times f_{TONE}))) \times 96000$							
1	1	1	0												

Table 13: RX TONE PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal in SUBAUDIO (CTCSS) mode.

n = INT (948982 x 100 / 4.032 x 10^6)
= INT (23.536) = 23
N = 010111 (binary)

$r = ((237245 / 4.032 \times 10^6) - (23 / (4 \times 100))) \times 8400$
= 11.26

R = 11 (rounding up if exactly halfway)
= 001011 (binary)

Thus the 12-bit code is 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SELCALL and SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

4.4.12 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and bits 0 - 5 of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to Table 14.

BYTE 1								BYTE 2						
5	4	3	2	1	0	Mod. 1 Attenuation		5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})		0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB		1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB		1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	11.6dB		1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	11.2dB		1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	10.8dB		1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	10.4dB		1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	10.0dB		1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	9.6dB		1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	9.2dB		1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	8.8dB		1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	8.4dB		1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	8.0dB		1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	7.6dB		1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	7.2dB		1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	6.8dB		1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	6.4dB		1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	6.0dB		1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	5.6dB		1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	5.2dB		1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	4.8dB		1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	4.4dB		1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	4.0dB		1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	3.6dB		1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	3.2dB		1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	2.8dB		1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	2.4dB		1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	2.0dB		1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	1.6dB		1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	1.2dB		1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.8dB		1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.4dB		1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB		1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is "1" the MOD2 attenuator and the SUMMING AMP are enabled. When this bit is "0" they are both disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to "0".

Table 14: AUDIO CONTROL Register (Hex address $8A)

4.4.13 SELCALL TX Register (Hex address $8D)

This is a 16-bit register. Byte (1) is sent first.

When the SELCALL transmitter is enabled, bits 0 to 12 control the frequency of the transmitted SELCALL tones according to the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming bits 0 through 12 to "0" places the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL Tx.

4.5 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
	SELCALL &	DCS	CTCSS			RX TONE			
$81	SUB-AUDIO	DECODE/	FAST	0	TONE	MSB			LSB
	STATUS	NO DECODE	TONE		DECODE	BIT 3	BIT 2	BIT 1	BIT 0
			GP TIMER	COMP	COMP	TONE	CTCSS FAST		DCS
$8F	IRQ FLAG	0	IRQ	0 to 1	1 to 0	IRQ	IRQ	0	IRQ
			FLAG	IRQ FLAG	IRQ FLAG	FLAG	FLAG		FLAG

Table 15: 8-bit Read Only Registers

4.6 Read Only Register Description

4.6.1 SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

DCS DECODE/ NO DECODE (Bit 7)	When the DCS decoder is enabled this bit is continuously updated with the result. A "1" indicates a successful decode (with 3 or less errors). A "0" indicates a failure to decode.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SIGNALING CONTROL Register and Bit 3 in the SIGNALING SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to "1" if a periodic tone is detected. If no periodic tone is detected this bit will be "0".
	When bits 5 and 3 are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to "1" if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX FREQUENCY Register is detected. If no match is found this bit will be "0". When Bit 5 in the SIGNALING CONTROL Register is set to "0" this bit will be "0".
(Bit 5)	Reserved for future use. This will be set to "0" but should be ignored by the user's software.

TONE DECODE (Bit 4)	This bit indicates the status of the tone decoder. A "1" indicates a tone has been detected (TONE DECODE) and a "0" indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SIGNALING SET-UP Register bits 7, 6, 5 and 4) and the RX TONE number (See SELCALL and SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SIGNALING CONTROL Register is set to "0" the TONE DECODE bit 4 will be set to "0". Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of "1111" in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone, will cause the NOTONE timer to be started. If loss of tone continues for the duration of the timeout period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the tone decoded according to the tones programmed in the RX TONE PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SIGNALING SET-UP Register, $82) and FREQUENCY (Bits 11 - 0, RX TONE PROGRAM Register, $84).

Table 16: SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

4.6.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as below:

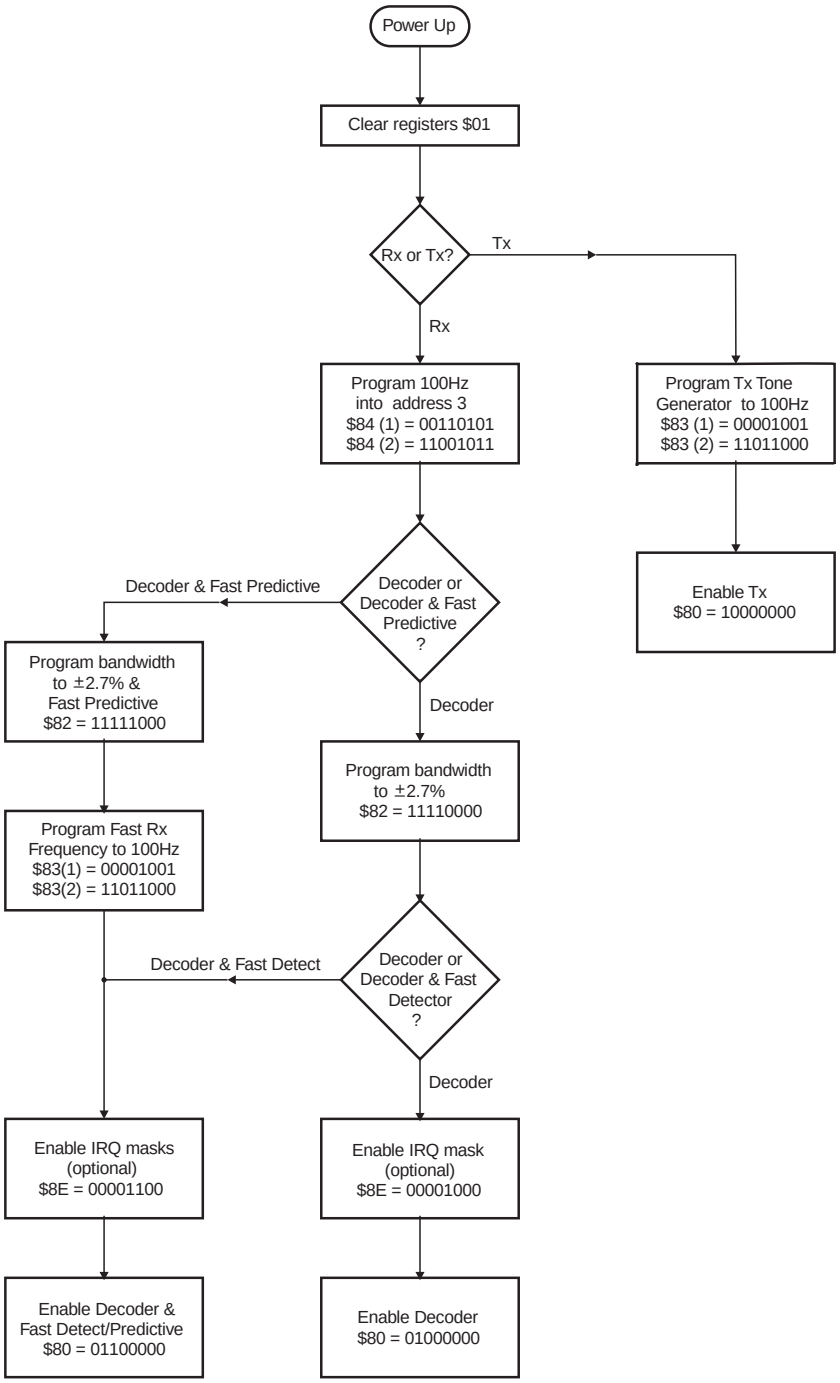
(Bits 7 and 1)	Reserved for future use. These will be set to "0" but should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to "1" to indicate the timeout has expired. This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
COMP 0 to 1 IRQ FLAG (Bit 5)	When the comparator output goes from "0" to "1" (i.e. when the input voltage is above the DAC output voltage) this bit will be set to "1" and an interrupt generated (if bit 5 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
COMP 1 to 0 IRQ FLAG (Bit 4)	When the comparator output goes from "1" to "0" this bit will be set to "1" and an interrupt generated (if bit 4 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
TONE IRQ FLAG (Bit 3)	When RX TONE DECODE (Bit 4, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
DCS IRQ FLAG (Bit 0)	When DCS DECODE/NO DECODE (Bit 7 SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

Table 17: IRQ FLAG Register (Hex address $8F)

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

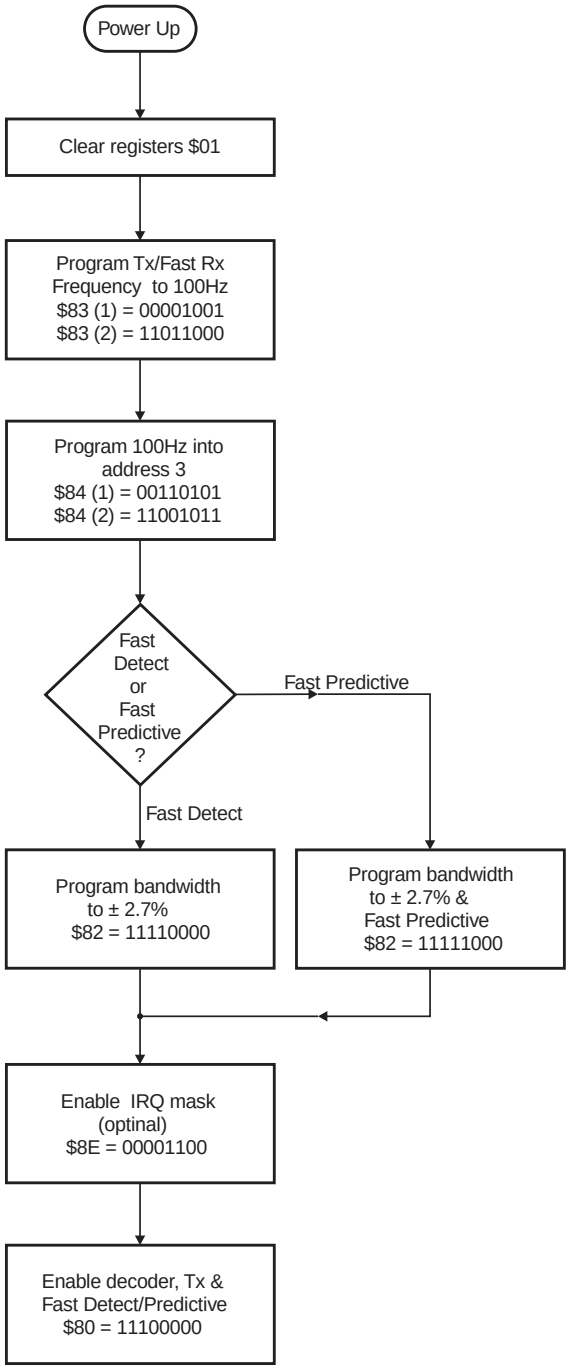
Note: $8X is the Hex address/command.



The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.



5. Application

5.1 General

The MX828 is intended for use in radio systems where signaling is required for functions such as trunking, control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permit certainty and signal to noise performance to be traded when congestion or range limits the system performance.

5.2 Transmitters

5.2.1 CTCSS

The CTCSS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX FREQUENCY Register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT (Bits 7 and 5 in the SIGNALING CONTROL Register $80).

5.2.2 The SelCall transmitter

The SelCall transmitter is enabled with Bit 2 in the SIGNALING CONTROL Register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the SELCALL TX Register ($8D) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the SelCall Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL TX ENABLE (Bit 2 in the SIGNALING CONTROL Register $80).

5.2.3 DCS Transmitter

The DCS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx data is set in the DCS BYTE 3, DCS BYTE 2 and DCS BYTE 1 Registers ($85, $86 and $87).

Note: The DCS transmitter produces an inverted output. When the signal is fed through the summing amp, in an inverted configuration, the correct polarity of the DCS signal will be restored (The MOD1 and MOD2 amplifier blocks do not invert).

5.3 Receiver (CTCSS/SelCall Decoder)

The CTCSS/SelCall decoder should first be set up according to the desired characteristics. This entails setting the TONE DECODER MODE Bit 2 of the SIGNALING SET UP Register ($82), and setting the TONE decoder bandwidth in the SIGNALING SET-UP Register ($82), also programming the center frequencies of the desired tones in the RX TONE PROGRAM Register ($84). (It can hold up to 15 different tones). Any tone can be in any location. When the device is decoding, the tones are scanned in the sequence of their location, i.e. $0 first and $E last. Once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The TONE IRQ MASK in the IRQ MASK Register ($8E) should also be set as required.

The TONE DECODER ENABLE in the SIGNALING CONTROL Register ($80) should then be set to "1". While in the CTCSS/SelCall decoder mode the fast/predictive detector may be enabled (see below). (Bit 5 in the SIGNALING CONTROL Register $80).

When the CTCSS/SelCall decoder detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG Register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SELCALL and SUB-AUDIO STATUS Register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (CTCSS Fast/Predictive Detector)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SIGNALING CONTROL Register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK Register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SIGNALING SET-UP Register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX FREQUENCY Register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG Register ($8F), and the CTCSS FAST TONE Bit 6 in the SELCALL and SUB-AUDIO STATUS Register ($81).

5.5 Receiver (DCS Decoder)

The incoming signal is matched with the DCS code programmed into the DCS BYTE 1/2/3 Registers. When the DCS decoder is enabled, the DCS DECODE/NO DECODE FLAG in Bit 7 of the SELCALL and SUB-AUDIO STATUS Register ($81) will be set if the decode is successful (3 or fewer errors). A "0" flag indicates a failure to decode. This flag is updated for every bit of the incoming signal.

In order to detect the DCS turn-off code (134Hz) the CTCSS tone decoder should also be enabled and programmed with this value. Once detected, this will cause a CTCSS tone decoder interrupt, the receiver audio output should then be muted.

5.6 General Purpose Timer (GPT)

This may be used in conjunction with the CTCSS/SelCall decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value in the GENERAL PURPOSE TIMER Register ($8B) set in units of 1msec, an IRQ FLAG in Bit 6 of the IRQ FLAG Register ($8F) and an IRQ MASK in Bit 6 of the IRQ MASK Register ($8E).

5.7 Full Duplex Modes

Although the device is specified as half duplex, the only functions that must operate as such are:

DCS Tx	or	DCS Rx
DCS Tx	or	CTCSS Tx
CTCSS decode	or	SELCALL decode

All other functions are totally independent and therefore a full duplex CTCSS or full duplex SELCALL along with many other combinations are possible.

5.7.1 Tx / Fast Rx Tone Table : CTCSS

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 18: Tx/Fast Rx Tone Table CTCSS

www.mxcom.com Tele: 800 638-5577 336 744-5050 Fax: 336 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

5.7.2 Rx Tone Program Tables : CTCSS

The following table lists the commonly used CTCSS tones together with the values for programming the “RX TONE PROGRAM” register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 19: Rx Tone Program Tables : CTCSS

5.7.3 Tx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'SELCALL TX' register ($8D).

EEA			CCIR			ZVEI 1			ZVEI 2		
Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
1981	01	FD	1981	01	FD	2400	01	A4	2400	01	A4
1124	03	81	1124	03	81	1060	03	B7	1060	03	B7
1197	03	4A	1197	03	4A	1160	03	65	1160	03	65
1275	03	17	1275	03	17	1270	03	1A	1270	03	1A
1358	02	E6	1358	02	E6	1400	02	D0	1400	02	D0
1446	02	B9	1446	02	B9	1530	02	93	1530	02	93
1540	02	8F	1540	02	8F	1670	02	5C	1670	02	5C
1640	02	67	1640	02	67	1830	02	27	1830	02	27
1747	02	41	1747	02	41	2000	01	F8	2000	01	F8
1860	02	1E	1860	02	1E	2200	01	CA	2200	01	CA
1055	03	BB	2400	01	A4	2800	01	68	885	04	73
930	04	3C	930	04	3C	810	04	DC	810	04	DC
2247	01	C1	2247	01	C1	970	04	0F	740	04	0F
991	03	F9	991	03	F9	885	04	73	680	05	CA
2110	01	DE	2110	01	DE	2600	01	84	970	04	0F

Table 20: Tx Tone Program Table : SelCall

5.7.4 Rx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'RX TONE PROGRAM' register ($84) in each Tone Address location as shown.

	EEA			CCIR			ZVEI 1			ZVEI 2		
Tone Address	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq (Hz)	Byte 1 (hex)	Byte 2 (hex)
0	1981	A	A	1981	A	A	2400	C	44	2400	C	44
1	1124	15	C3	1124	15	C3	1060	15	53	1060	15	53
2	1197	26	D	1197	26	D	1160	25	D2	1160	25	D2
3	1275	36	85	1275	36	85	1270	36	83	1270	36	83
4	1358	46	D1	1358	46	D1	1400	47	E	1400	47	E
5	1446	57	4D	1446	57	4D	1530	57	C8	1530	57	C8
6	1540	67	CB	1540	67	CB	1670	68	86	1670	68	86
7	1640	78	4B	1640	78	4B	1830	79	49	1830	79	49
8	1747	88	CD	1747	88	CD	2000	8A	42	2000	8A	42
9	1860	99	84	1860	99	84	2200	9B	43	2200	9B	43
10	1055	A5	51	2400	AC	44	2800	AE	46	885	A4	86
11	930	B4	C4	930	B4	C4	810	B4	14	810	B4	14
12	2247	CB	83	2247	CB	83	970	C4	D8	740	C3	C8
13	991	D5	A	991	D5	A	885	D4	86	680	D3	80
14	2110	EA	C5	2110	EA	C5	2600	ED	45	970	E4	D8

Table 21: Rx Tone Program Table : SelCall

5.7.5 DCS Code Table

The following table gives a list of DCS codes together with the corresponding values (in Hex) which should be programmed into the DCS BYTE registers for a 23-bit DCS sequence.

DCS Code	DCS Byte 3 ($85)	DCS Byte 2 ($86)	DCS Byte 1 ($87)
023	76	38	13
025	6B	78	15
026	65	D8	16
031	51	F8	19
032	5F	58	1A
043	5B	68	23
047	0F	D8	27
051	7C	A8	29
054	6F	48	2C
065	5D	18	35
071	67	98	39
072	69	38	3A
073	2E	68	3B
074	74	78	3C
114	35	E8	4C
115	72	B8	4D
116	7C	18	4E
125	07	B8	55
131	3D	38	59
132	33	98	5A
134	2E	D8	5C
143	37	A8	63
152	1E	C8	6A
155	44	D8	6D
156	4A	78	6E
162	6B	C8	72
165	31	D8	75
172	05	F8	7A
174	18	B8	7C
205	6E	98	85
223	68	E8	93
226	7B	08	96
243	45	B8	A3
244	1F	A8	A4
245	58	F8	A5
251	62	78	A9
261	17	78	B1
263	5E	88	B3
265	43	C8	B5
271	79	48	B9
306	0C	F8	C6
311	38	D8	C9
315	6C	68	CD
331	23	E8	D9
343	29	78	E3
346	3A	98	E6
351	0E	B8	E9
364	68	58	F4
365	2F	08	F5
371	15	88	F9
411	77	69	09
412	79	C9	0A
413	3E	99	0B
423	4B	99	13
431	6C	59	19
432	62	F9	1A
445	7B	89	25
464	27	E9	34
465	60	B9	35
466	6E	19	36
503	3C	69	43
506	2F	89	46
516	41	B9	4E
532	0E	39	5A
546	19	E9	66
565	0C	79	75
606	5D	99	86
612	67	19	8A
624	0F	59	94
627	01	F9	97
631	72	89	99
632	7C	29	9A
654	4C	39	AC
662	24	79	B2
664	39	39	B4
703	22	B9	C3
712	0B	D9	CA
723	39	89	D3
731	1E	49	D9
732	10	E9	DA
734	0D	A9	DC
743	14	D9	E3
754	20	F9	EC

Table 22: DCS Code Table

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308 mV_{RMS} at 1kHz
V_{DD} = 3.3V to 5.0V, T_{AMB}= 25°C, T_{OP} = -40°C to 85°C
Composite Signal = 308 mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31 mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
V_{DD} = 3.3V						
I_{DD}						
All Powersaved		2		0.5	1.0	mA
FAST DETECT Enabled		2		1.7	2.5	mA
Rx Operating						
DCS, FAST DETECT and CTCSS or SelCall		2		3.0	4.5	mA
Tx Operating						
DCS or SelCall or SUB AUDIO		2		1.5	3.0	mA
DCS and SelCall		2		2.5	4.0	mA
V_{DD} = 5.0V						
I_{DD}						
All Powersaved		1, 2		1.0	1.5	mA
FAST DETECT Enabled		1, 2		3.0	4.5	mA
Rx Operating						
DCS, FAST DETECT and CTCSS or SelCall		1, 2		5.5	7.5	mA
Tx Operating						
DCS or SelCall or SUB AUDIO		1, 2		4.5	6.0	mA
DCS and SelCall		1, 2		5.0	6.5	mA
"C-BUS" Interface						
Input Logic "1"			70%			V_{DD}
Input Logic "0"					30%	V_{DD}
Input Leakage Current	Logic "1" or "0"		-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic "1"	I_{OH} = 120µA		90%			V_{DD}
Output Logic "0"	I_{OL} = 360µA				10%	V_{DD}
"Off" State Leakage Current	$V_{OUT} = V_{DD}$	6			10	µA
AC Parameters						
TONE Decoder						
Sensitivity	Pure Tone	5		-26.0		dB
CTCSS						
Response Time	Composite Signal			140		ms
De-response Time	Composite Signal			145		ms
Frequency Range			60		253	Hz
SelCall						
Response Time	Good Signal			14		ms
De-response Time	Good Signal			22		ms
Frequency Range			625		3000	Hz

DCS Decoder						
Bit-Rate Sync Time				2		edges
Sensitivity		1	58		116	mV_{P-P}
CTCSS Detector - Fast Detect						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal			56.0		ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Predictive						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal	7		37.0		ms
Frequency Range			60		253	Hz
Decode Bandwidth				40		Hz
CTCSS Encoder						
Frequency Range			60.0		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	+1.0	dB
Total Harmonic Distortion		9		2.0		%
SELCALL Encoder						
Frequency Range			208		3000	Hz
Tone Frequency Resolution					0.2	%
Tone Amplitude Tolerance		1	-1.0		+1.0	dB
Total Harmonic Distortion		9		2.0		%
DCS Encoder						
Bit Rate				134.4		bps
Amplitude Tolerance		1	-1.0		+1.0	dB
Amplitude		1		871		mV_{P-P}
Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain (at 1.0kHz)		8		0		dB
Passband Ripple	wrt gain at 1.0kHz	8	-2		+0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz
Output Impedance						
TX AUDIO OUT, TX SUB AUDIO OUT and RX AUDIO OUT						
Enabled		10		2.0		kΩ
Disabled				500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	input = 1mV at 100Hz			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	at 100Hz		10			MΩ
Output Impedance	Open Loop			6.0		kΩ

Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation	at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error	wrt attenuation at 0dB		-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	at 100Hz			15.0		kΩ
Mod.2 Attenuator						
Attenuation	at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error	wrt attenuation at 0dB		-0.6		0.6	dB
Output Impedance		3		600		Ω
General Purpose Timer						
Timing Period Range			1		255	ms
Count Interval				1		ms
Xtal/Clock Input						
Pulse Width	('High' or 'Low'	4	40.0			ns
Input Impedance	(at 100Hz)		10.0			MΩ
Gain	input = $1mV_{RMS}$ at 100Hz		20.0			dB
D/A						
Range		1	312.5		2500	mV
Step Size		1		312.5		mV
Step Accuracy		1	-30		30	mV
Input Impedance	COMPIN			10		MΩ
Output Impedance	COMPOUT			1		kΩ

Table 23: Operating Characteristics

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance, at V_{DD} = 5.0V and T_{AMB} = 25°C.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{IRQ}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD 1 or MOD 2 output.
10. SUBAUDIO, SELCALL and DCS.

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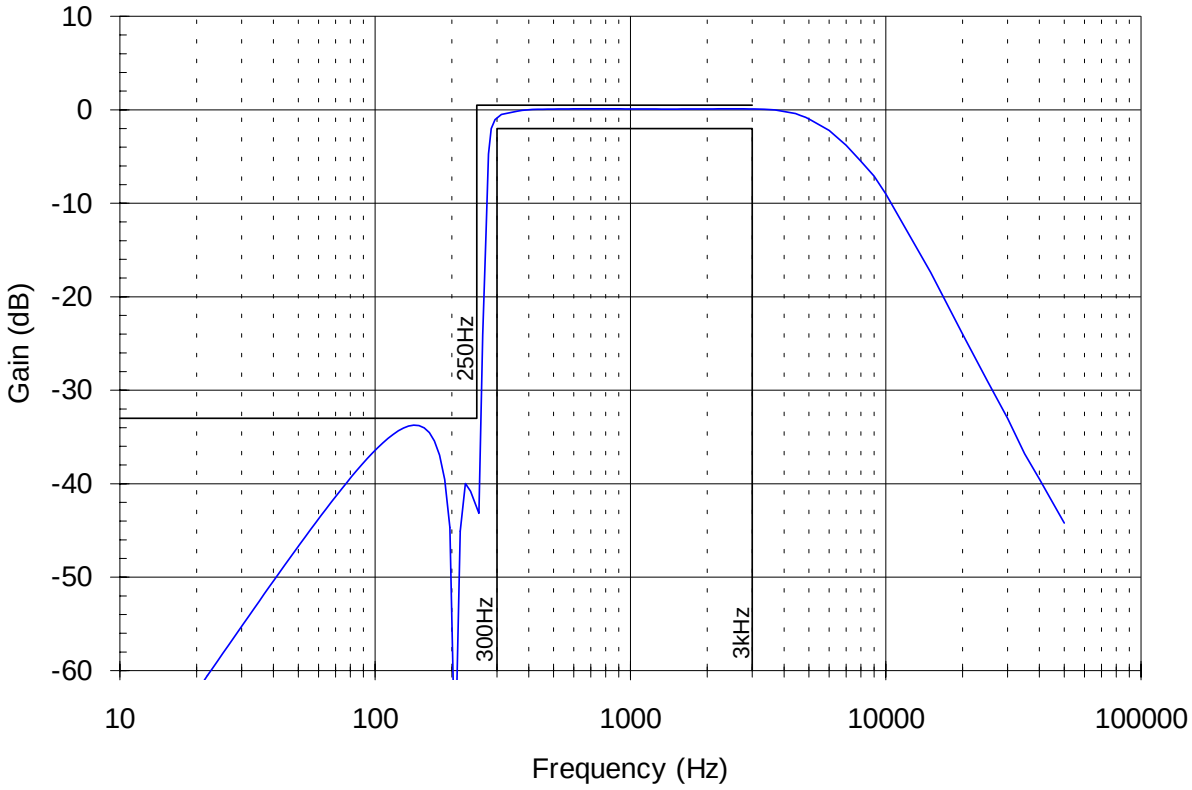


Figure 3: Audio Band-Pass Filter Frequency Response

6.2 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = -40°C to +85°C.

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs

Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

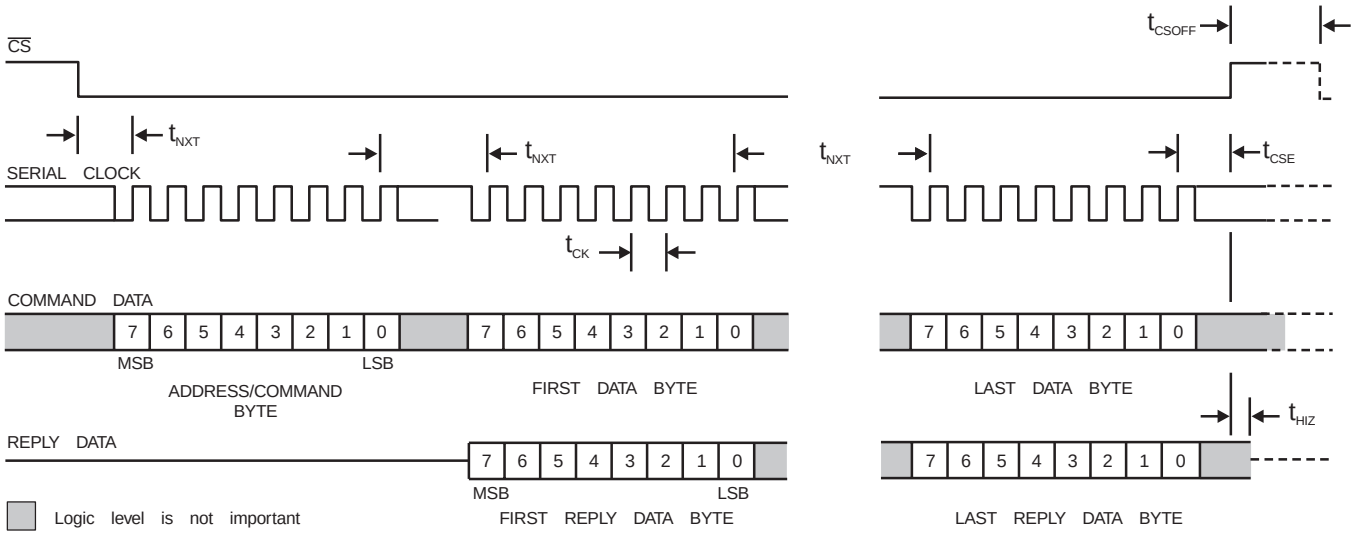
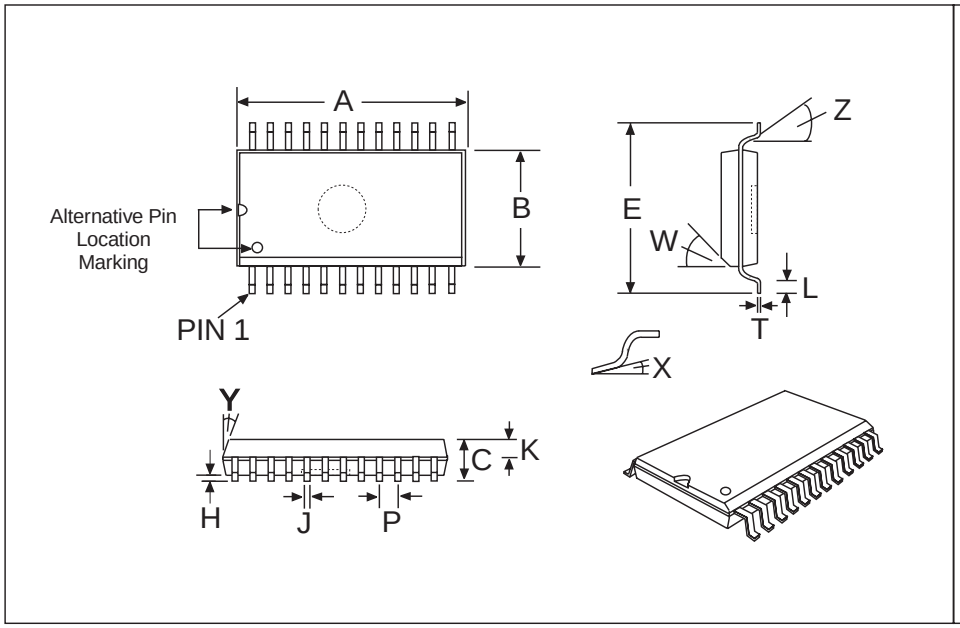


Figure 4: "C-BUS" Timing

6.3 Packaging

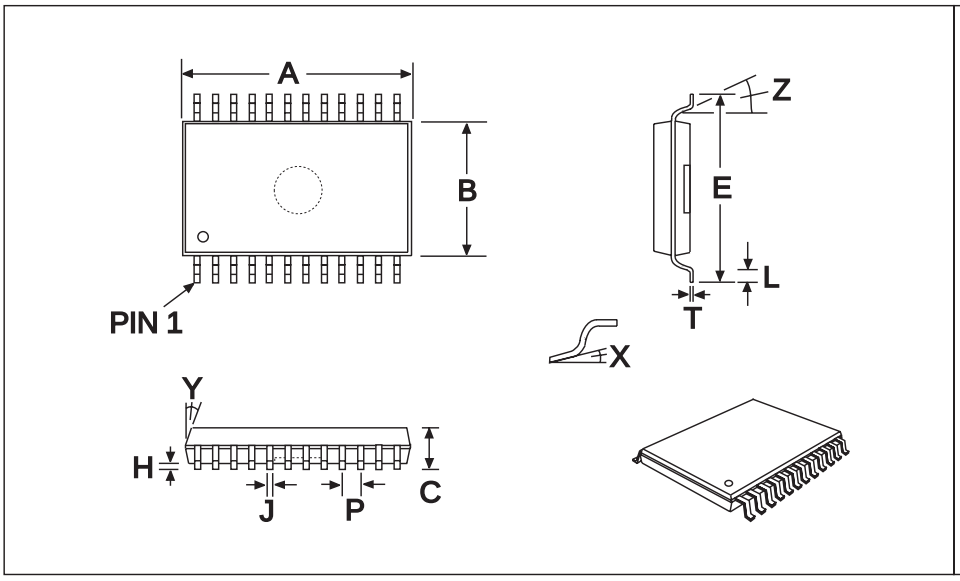


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin SOIC Mechanical Outline: *Order as part no. MX828DW*

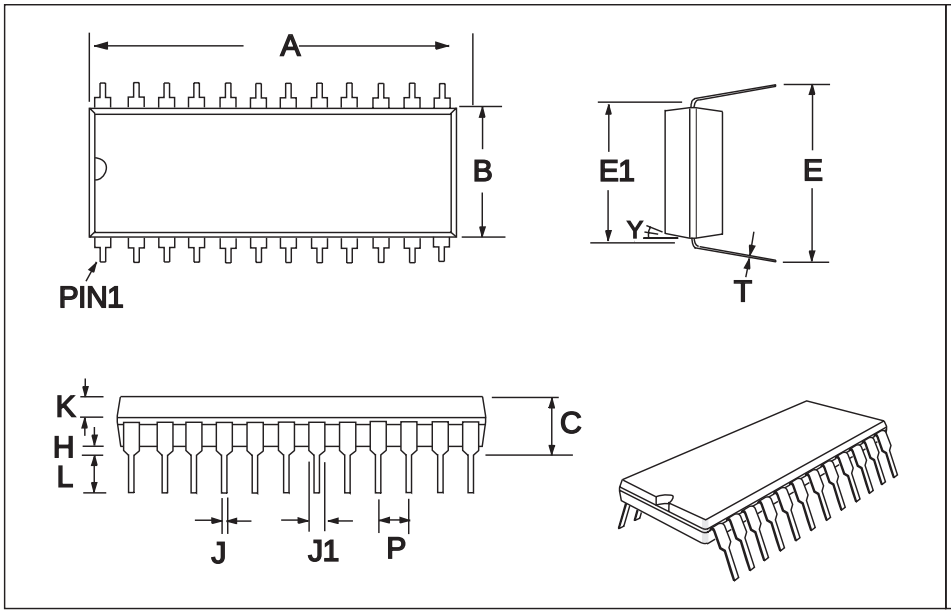


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SSOP Mechanical Outline: *Order as part no. MX828DS*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: Figure 5: 24-pin PDIP Mechanical Outline: Order as part no. MX828P