Genesys Logic, Inc.

GL861

USB 2.0 Controller for PC-DTV Application

Datasheet

Preliminary Revision 1.01

Dec. 27, 2005

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Revision History

Revision	Date	Description
1.00	2005/6/15	First lease
1.01	2005/12/27	Remove application circuit

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CHAPTER 1 GENERAL DESCRIPTION

The GL861 is a high performance USB 2.0 controller for PC-DTV application. With the Genesys Logic's highly recognized self-developed USB high-speed transceiver, GL861 provides up to 480Mbps bandwidth for fulfilling the mass bandwidth demand of video transferring. GL861 also supports USB isochronous mode to provide certain bandwidth to insure user can get satisfied usage experience on video application even running high bandwidth consumption devices concurrently. The GL861's low power consumption, low operation temperature characteristics also make it easy to implement a high quality bus-power DTV or any DTV combo devices without worrying about the thermal or power scarcity issues caused by USB controller.

CHAPTER 2 FEATURES

- USB specification compliance
  - Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Complies with 12Mbps Universal Serial Bus specification rev. 2.0.
  - Support USB 2.0 Isochronous Video pipe to 24MB/s.
- Demodulator interface
  - MPEG2-TS
- Demux built-in
  - 34 PID filtering
- Non-processing video streaming (USB High-speed connection)
- Support 4 USB endpoints
  - Endpoint 0: Control PIPE.
  - Endpoint 1: Isochronous/Bulk data in (configurable).
  - Endpoint 2: Interrupt OUT.
  - Endpoint 3: Interrupt IN.
- Embedded 8052 micro-controller
  - Operate @ 15 MHz clock.
  - 8K ROM.
- Support firmware stored in external FLASH memory for development of customer's firmware
- Support USB remote wakeup.
- Maximum 15 GPIO ports.
- 3.3V operation.
- Capability to support on-line download program
- Available in 100-pin QFP and 48-pin LQFP package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

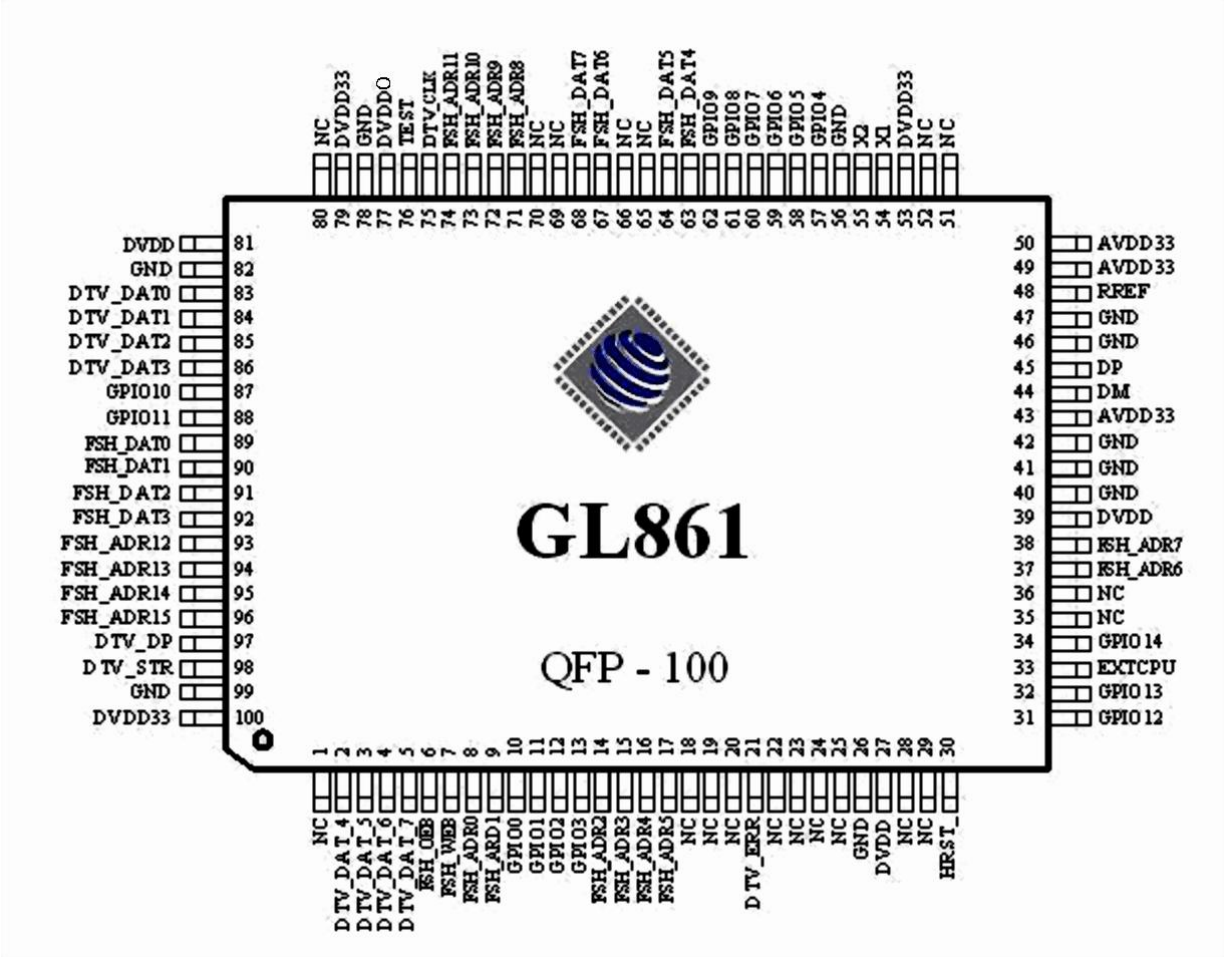


Figure 3.1 - 100 Pin QFP Pinout Diagram

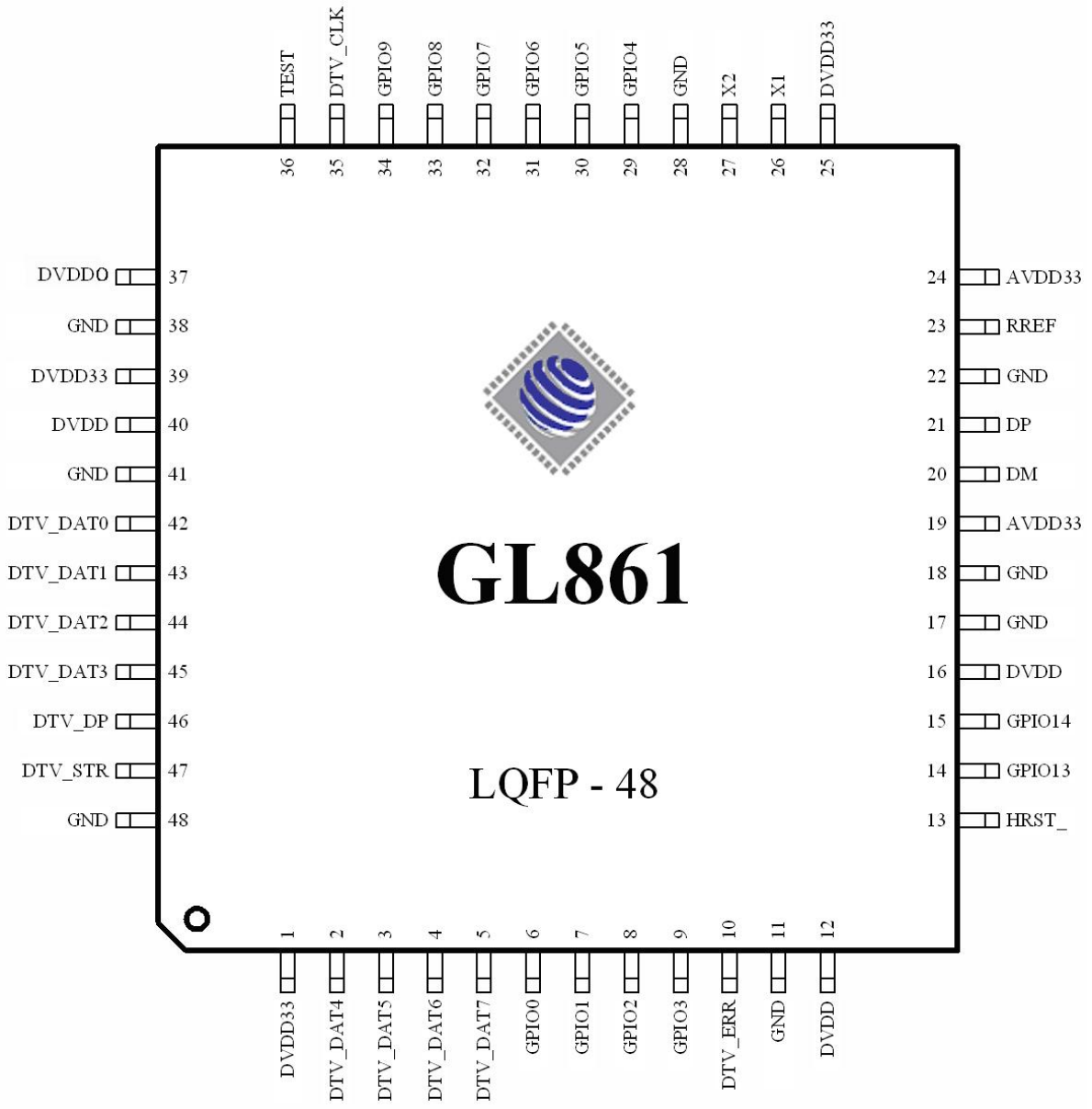


Figure 3.2 - 48 Pin LQFP Pinout Diagram

3.2 Pin List

Two package types: Type 1

- 100-pin QFP package with built-in ICE and flash memory interface
- 15 GPIO pins

Type 2

- 48-pin LQFP package
- 12 GPIO pins

Table 3.1 - 100-Pin QFP Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	NC	-	26	GND	P	51	NC	-	76	TEST	I
2	DTV_DAT4	I	27	DVDD	P	52	NC	-	77	DVDDO	P
3	DTV_DAT5	I	28	NC	-	53	DVDD33	P	78	GND	P
4	DTV_DAT6	I	29	NC	-	54	X1	I	79	DVDD33	P
5	DTV_DAT7	I	30	HRST_	I	55	X2	I/O	80	NC	-
6	FSH_OEB	I	31	GPIO12	I/O	56	GND	P	81	DVDD	P
7	FSH_WEB	I	32	GPIO13	I/O	57	GPIO4	I/O	82	GND	P
8	FSH_ADR0	I/O	33	EXTCPU	I	58	GPIO5	I/O	83	DTV_DAT0	I
9	FSH_ADR1	I/O	34	GPIO14	I/O	59	GPIO6	I/O	84	DTV_DAT1	I
10	GPIO0	I/O	35	NC	-	60	GPIO7	I/O	85	DTV_DAT2	I
11	GPIO1	I/O	36	NC	-	61	GPIO8	I/O	86	DTV_DAT3	I
12	GPIO2	I/O	37	FSH_ADR6	I/O	62	GPIO9	I/O	87	GPIO10	I/O
13	GPIO3	I/O	38	FSH_ADR7	I/O	63	FSH_DAT4	I/O	88	GPIO11	I/O
14	FSH_ADR2	I/O	39	DVDD	P	64	FSH_DAT5	I/O	89	FSH_DAT0	I/O
15	FSH_ADR3	I/O	40	GND	P	65	NC	-	90	FSH_DAT1	I/O
16	FSH_ADR4	I/O	41	GND	P	66	NC	-	91	FSH_DAT2	I/O
17	FSH_ADR5	I/O	42	GND	P	67	FSH_DAT6	I/O	92	FSH_DAT3	I/O
18	NC	-	43	AVDD33	P	68	FSH_DAT7	I/O	93	FSH_ADR12	I/O
19	NC	-	44	DM	I/O	69	NC	-	94	FSH_ADR13	I/O
20	NC	I	45	DP	I/O	70	NC	-	95	FSH_ADR14	I/O
21	DTV_ERR	I	46	GND	P	71	FSH_ADR8	I/O	96	FSH_ADR15	I/O
22	NC	-	47	GND	P	72	FSH_ADR9	I/O	97	DTV_DP	I
23	NC	-	48	RREF		73	FSH_ADR10	I/O	98	DTV_STR	I
24	NC	-	49	AVDD33	P	74	FSH_ADR11	I/O	99	GND	P
25	NC	-	50	AVDD33	P	75	DTV_CLK	I/O	100	DVDD33	P

Table 3.2 - 48-Pin LQFP Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DVDD33	P	13	HRST_	I	25	DVDD33	P	37	DVDDO	P
2	DTV_DAT4	I	14	GPIO13	I/O	26	X1	I	38	GND	P
3	DTV_DAT5	I	15	GPIO14	I/O	27	X2	I/O	39	DVDD33	P
4	DTV_DAT6	I	16	DVDD	P	28	GND	P	40	DVDD	P
5	DTV_DAT7	I	17	GND	P	29	GPIO4	I/O	41	GND	P
6	GPIO0	I/O	18	GND	P	30	GPIO5	I/O	42	DTV_DAT0	I
7	GPIO1	I/O	19	AVDD33	P	31	GPIO6	I/O	43	DTV_DAT1	I
8	GPIO2	I/O	20	DM	I/O	32	GPIO7	I/O	44	DTV_DAT2	I
9	GPIO3	I/O	21	DP	I/O	33	GPIO8	I/O	45	DTV_DAT3	I
10	DTV_ERR	P	22	GND	P	34	GPIO9	I/O	46	DTV_DP	I/O
11	GND	P	23	RREF	A	35	DTV_CLK	I/O	47	DTV_STR	I/O
12	DVDD	P	24	AVDD33	P	36	TEST	I	48	GND	P

3.3 Pin Descriptions

Table 3.3 - 100-Pin QFP Pin Descriptions

Pin Name	Pin#	Type	Description
DVDDO	77	P	1.8V output
DVDD	27,39,81	P	1.8V core power
DTV_DAT0~7	83~86,2~5	I	MPEG2-TS data bit 0~7
FSH_OEB	6	I	Read strobe of ICE /Output enable for flash memory. Low active
FSH_WEB	7	I	Write strobe of ICE /Write enable for flash memory. Low active.
FSH_ADR0~15	8,9,14~17, 37,38,71~74, 93~96	I/O	Port 0 and Port 2 for ICE mode/ Address of flash memory
GPIO0~14	10~13,57~62, 87,88,31,32,34	I/O (pu: GPIO0, 1, 7, 8, 12, 13, 14 pd: GPIO3, 10)	15 GPIOs
DTV_ERR	21	I	Error indication for MPEG2-TS stream
GND	26,40,41,42, 46,47,56,78, 82,99	P	Ground
HRST_	30	I (pu)	Hardware reset, low active
EXTCPU	33	I	Use external CPU mode for ICE development.
AVDD33	43,49,50	P	3.3V analog power
DM	44	I/O	USB D-
DP	45	I/O	USB D+
RREF	48	A	Reference R
X1	54	I	12M crystal in
X2	55	O	12M crystal out
FSH_DAT4	63	I/O	Data bus of flash memory/ ALE signal of ICE
FSH_DAT5~7	64,67,68	I/O	Data bus of flash memory
DTV_CLK	75	I	MPEG clock input from demodulator
TEST	76	I (pd)	Test mode
FSH_DAT0	89	I/O	Data bus of flash memory/ Clock output for ICE
FSH_DAT1	90	I/O	Data bus of flash memory/ RST pin for ICE mode
FSH_DAT2	91	I/O	Data bus of flash memory/ Interrupt 0 of ICE mode
FSH_DAT3	92	I/O	Data bus of flash memory/ Interrupt 1 of ICE mode
DTV_DP	97	I	MPEG data valid from demodulator
DTV_STR	98	I	MPEG packet start from demodulator
DVDD33	53,79,100	P	3.3V power
NC	1,18~20,22~25, 28,29,35,36,51 ,52,65,66,69,70 ,80	-	No connection

Table 3.4- 48-Pin LQFP Pin Descriptions

Pin Name	Pin#	Type	Description
DVDDO	37	P	1.8V output
DVDD	12,16,37,40	P	1.8V core power
DTV_DAT0~7	42~45,2~5	I	MPEG2-TS data bit 0~7
GPIO0~9, 13,14	6~9,29~34, 14,15	I/O (pu: GPIO0, 1, 7, 8, 13, 14 pd: GPIO10)	12 GPIOs
DTV_ERR	10	I	Error indication for MPEG2-TS stream
GND	11,17,18,22, 28,38,41,48	P	Digital ground
HRST	13	I (pu)	Hardware reset, low active
AVDD33	19,24	P	Analog power
DM	20	I/O	USB D-
DP	21	I/O	USB D=
RREF	23	A	Reference R
X1	26	I	12M crystal in
X2	27	I/O	12M crystal out
DTV_CLK	35	I	MPEG clock input from demodulator
TEST	36	I (pd)	Test mode
DVDD33	1,25,39	P	3.3V power
DTV_DP	46	I	MPEG data valid from demodulator
DTV_STR	47	I	MPEG packet start from demodulator

Notation:

Type	**O**	Output
	I	Input
	P	Power / Ground
	A	Analog
	pu	Internal pull up
	pd	Internal pull down

CHAPTER 4 FUNCTIONAL DESCRIPTION

4.1 Function Block

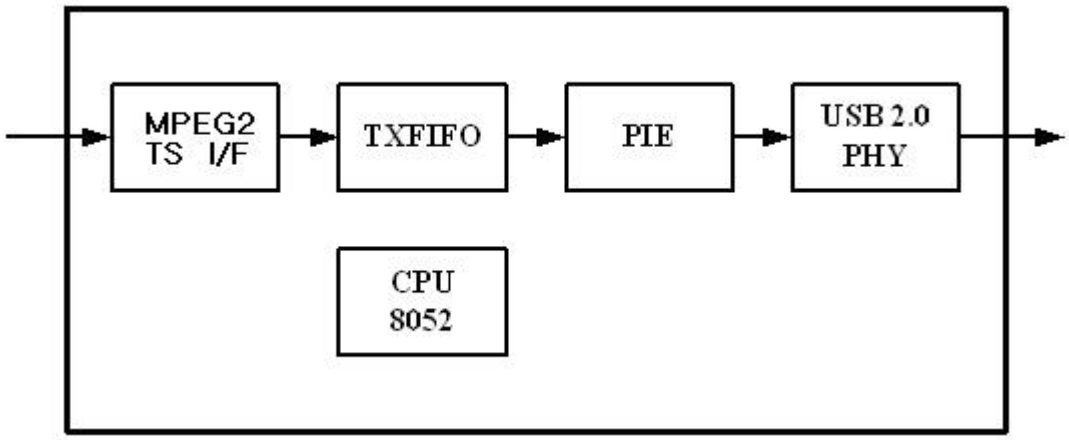


Figure 4.1 - Block Diagram

- **DTV Interface**

  GL861 can link with various MPEG2-TS demodulators on market for DTV terrestrial application. GL861 also builds in PID filter for channel demultiplex operation. That will make USB full speed application more realizable and no extra component is needed. This function can filter totally 34 PID by setting.

- **TXFIFO**

  GL861 builds in 6K bytes internal buffer for high bandwidth application. This 6K internal buffer can be used as transmitted buffer of isochronous pipe or bulk pipe.

- **PIE**

  PIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0*. It co-works with CPU to play the role of the chip's kernel. The main functions of PIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB1.1, bit stuffing/de-stuffing is implemented in UTMI, not in PIE.

- **USB 2.0 PHY (UTMI)**

  UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB2.0 test modes, and serial/parallel conversion.

- **CPU**

  CPU is the micro-processor unit of GL861. It is an 8-bit 8052 processor with 8K ROM and 256 bytes RAM. It operates at 15Mhz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, μC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for various configurations. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

4.2 Operation Mode

For customized firmware, flash memory can be used as external program memory of CPU. This is for customer to develop their own firmware and only available for 100-pin package type.

CHAPTER 5 ELECTRICAL CHARACTERISTICS

5.1 Maximum Ratings

Table 5.1 - Maximum Ratings

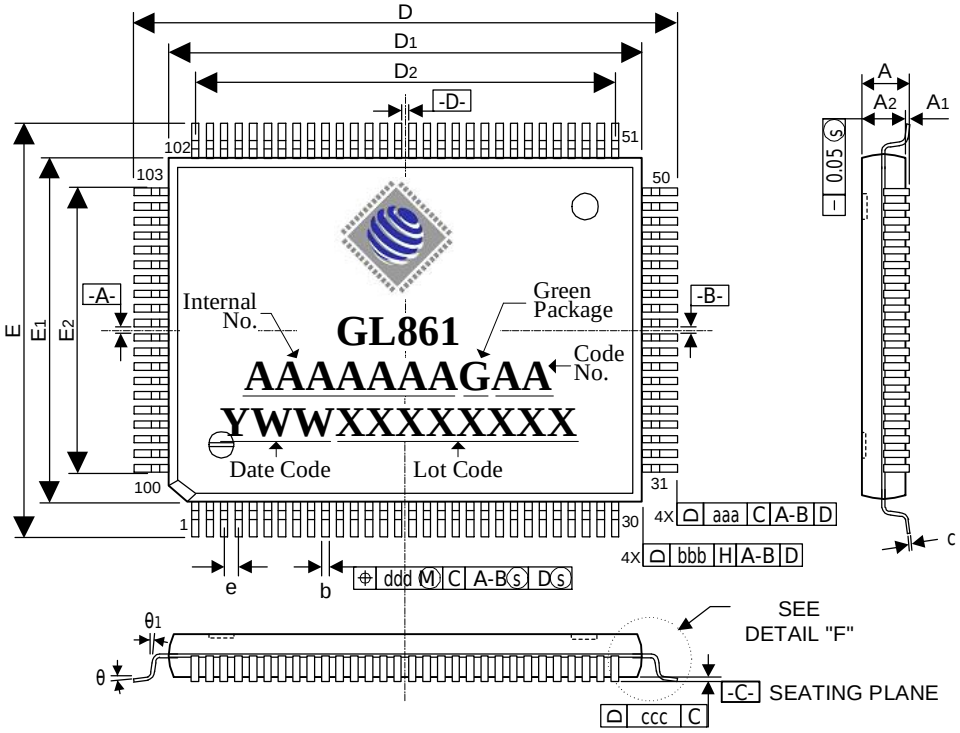
Symbol	Parameter	Min.	Max.	Unit
V_{IN}	3.3V Input Voltage	3.0	3.6	V
T_A	Ambient Temperature under bias	0	+100	^oC
F_{OSC}	Frequency	12 MHz ± 500ppm		

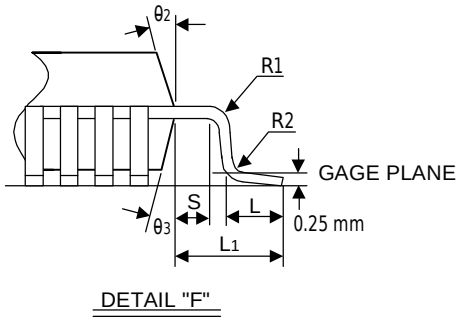
5.2 DC Characteristics

Table 5.2 - DC Characteristics Except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_D	Power Dissipation	-	-	-	mA
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	0.9	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.36	1.48	1.62	V
V_{THL}	HIGH to LOW threshold voltage	1.36	1.48	1.62	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	-	µA
R_{DN}	Pad internal pull down resister	-	-	-	Ω
R_{UP}	Pad internal pull up resister	-	-	-	Ω

CHAPTER 6 PACKAGE DIMENSION





DETAIL "F"

NOTES :

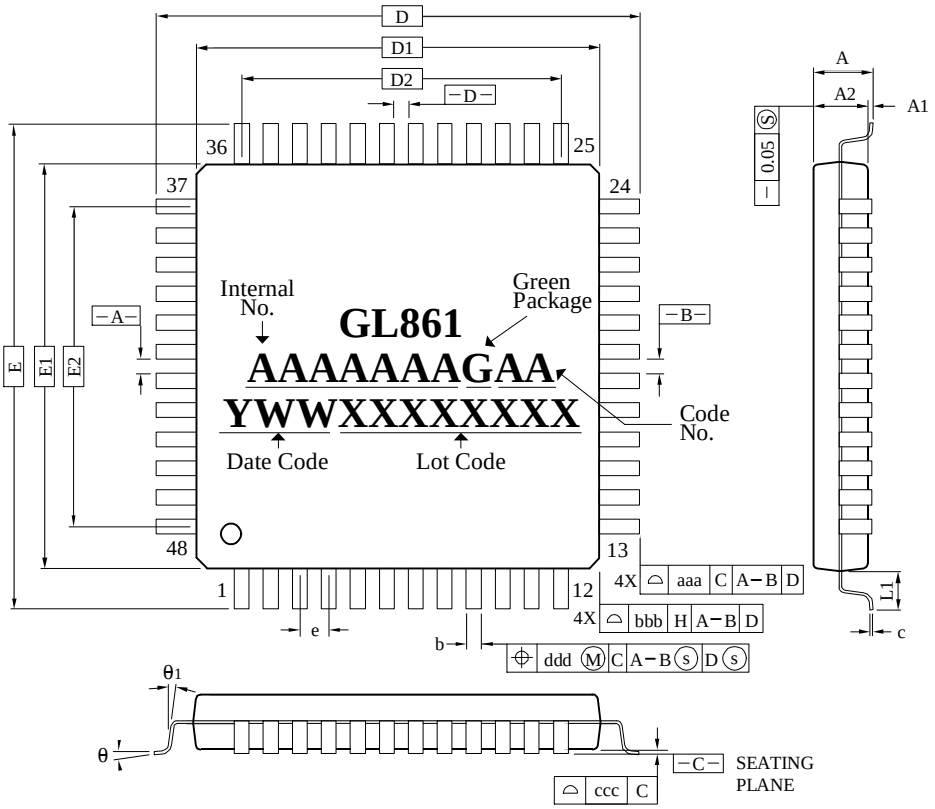
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

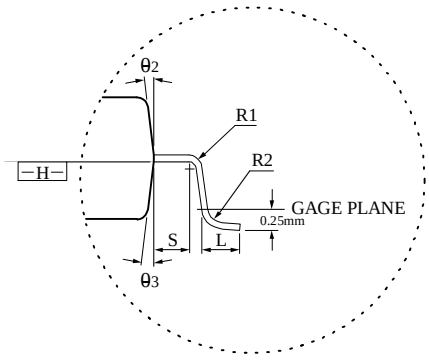
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
E	17.20 BASIC			0.677 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	18.85 BASIC			0.742 BASIC		
E2	12.35 BASIC			0.486 BASIC		
R1	0.13	—	—	0.005	—	—
R2	0.13	—	0.30	0.005	—	0.012
θ	0	—	7	0	—	7
θ1	0	—	—	0	—	—
θ2	15 REF			15 REF		
θ3	15 REF			15 REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BASIC			0.026 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.13			0.005		
ddd	0.10			0.004		

Figure 6.1 - GL861 100 Pin QFP Package





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 6.2 - GL861 48 Pin LQFP Package

CHAPTER 7 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL861	100-pin QFP	
GL861	48-pin LQFP	

