

DSP56853

Preliminary Product Brief DSP56853 16-bit Digital Signal Processors

- 120 MIPS at 120MHz
- 12K x 16-bit Program SRAM
- 4K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- Access up to 2M words of program memory or 8M of data memory
- Chip Select Logic for glue-less interface to ROM and SRAM
- Six (6) independent channels of DMA
- Enhanced Synchronous Serial Interfaces (ESSI)
- Two (2) Serial Communication Interfaces (SCI)
- Serial Port Interface (SPI)
- 8-bit Parallel Host Interface
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time-of-Day (TOD)
- 128 LQFP package
- Up to 41 GPIO

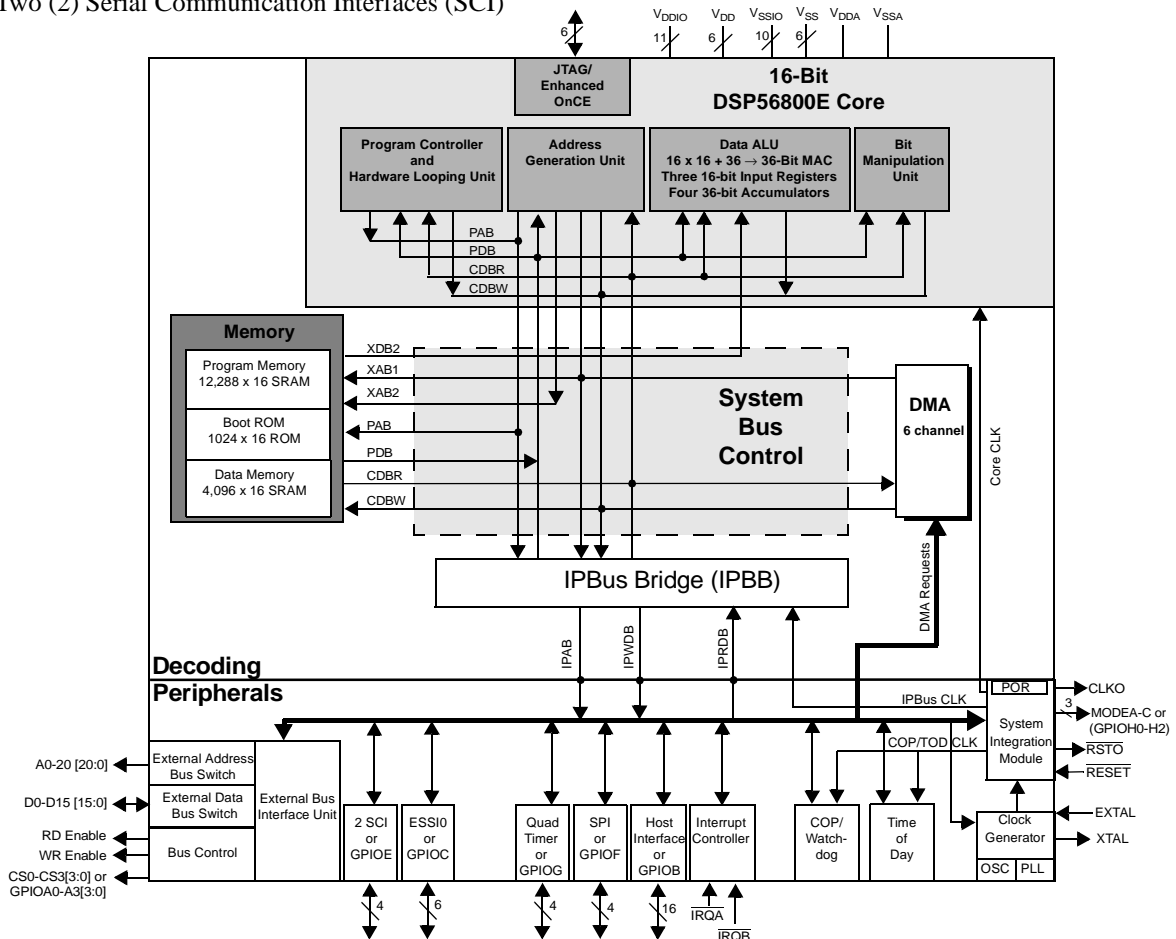


Figure 1. DSP56853 Block Diagram

DSP56800E Core Features

The DSP56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C Compilers, enabling rapid development of optimized control applications. Features of the DSP56800E core include:

- Efficient 16-bit DSP engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16×16 -bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

DSP56853 Memory Features

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
 - $12K \times 16$ -bit Program SRAM
 - $4K \times 16$ -bit Data SRAM
 - $1K \times 16$ -bit Boot ROM
- Off-Chip Memory Expansion (EMI)
 - Access up to 2M words of program memory or 8M data memory
 - Chip Select Logic for glue-less interface to ROM and SRAM

DSP56853 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer with four (4) external pins*
- Two (2) Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer

- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging
- Six (6) independent channels of DMA
- 8-bit Parallel Host Interface*
- Time-of-Day (TOD)
- Up to 41 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

DSP56853 Description

The DSP56853 is a member of the DSP56800E core-based family of Digital Signal Processors (DSPs). This device combines the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals on a single chip to create an extremely cost-effective solution. The low cost, flexibility, and compact program code make this device well-suited for many applications. The DSP56853 includes peripherals that are especially useful for teledatacom devices; Internet appliances; portable devices; TAD; voice recognition; hands-free devices; and general purpose applications.

“Best in Class” Development Environment

The Software Development Kit (SDK) provides fully-debugged peripheral drivers, libraries and interfaces that allow a programmer to create his own unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

Product Documentation

The four documents listed below are required for a complete description and proper design with the DSP56853. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/semiconductors/.

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit DSP core processor and the instruction set	DSP56800ERM/D
DSP56853 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56853	DSP5685xUM/D
DSP56853 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56853/D
DSP56853 Product Brief	Summary description and block diagram of the DSP56853 core, memory, peripherals and interfaces (this document)	DSP56853PB/D

Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to order parts.

Table 1. Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56853	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	128	120	DSP56853FG120

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