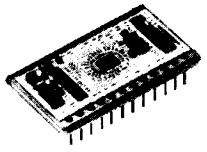
DAC-02315 AND DGL-02316

12 BIT DEGLITCHED D/A CONVERTER
35 MHz Update Rate; Voltage Output



DAC-02315

DGL-02316

DESCRIPTION

The DAC-02315 and DGL-02316 is a 12 bit, 35 MHz update rate, deglitched DAC hybrid pair with a low impedance voltage output. Packaged in small, 24 pin DDIP hybrids, the DAC-02315 and DGL-02316 offer a −55°C to +125°C operating temperature range and screening to MIL-STD-883B, revision C.

The DAC-02315 and DGL-02316 pair offers 35 nsec settling for a full scale change offset and pedestal errors trimmable to zero with external potentiometers.

With its 12 bit resolution, low glitch voltage output and small hermetic packages, the DAC-02315 and DGL-02316 is ideal for the most demanding low noise applications such as vector-stroke CRT display, waveform generators and automatic test equipment.

FEATURES

- *HIGH SPEED – 35 MHz UPDATE RATE FOR FULL SCALE CHANGES*
- *LOW GLITCH – 14mVpp GLITCH VOLTAGE 38ns GLITCH DURATION*
- *SMALL SIZE – 24 PIN DDIP HYBRIDS*
- *−55°C TO +125°C OPERATION*
- *MIL-STD-883 SCREENING AVAILABLE*
- *FULL FUNCTION – EVALUATION CARD AVAILABLE*

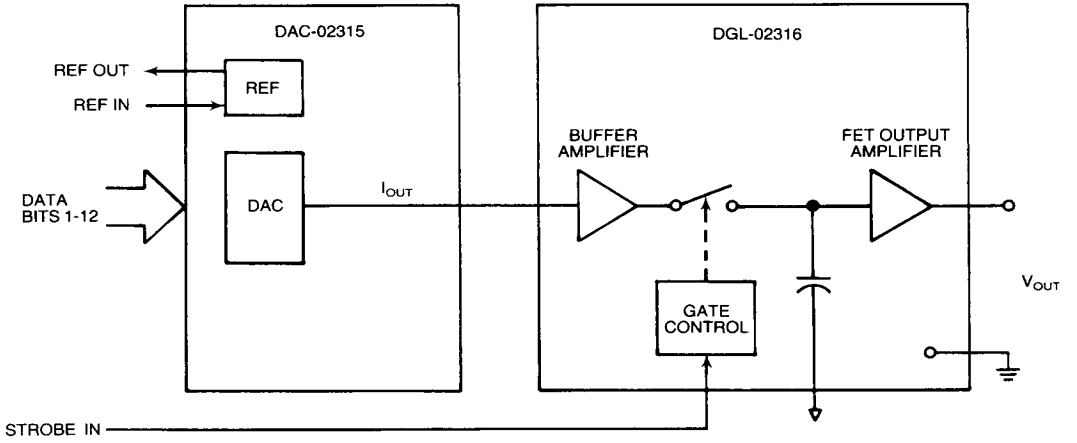


FIGURE 1. DAC-02315/DGL-02316 BLOCK DIAGRAM

TABLE 1. DAC-02315/DGL-02316 SPECIFICATIONS

Typical values at 25°C and nominal power supply voltages unless otherwise specified.

PARAMETER	UNITS	VALUE			
ACCURACY					
Linearity Error (2K max load)	% FSR	+0.0125 max			
Linearity Tempco	PPM/°C	±5			
Offset (trimmable to zero)	mV	25 typ, 100 max			
Offset Tempco	mV/°C	0.2 typ, 0.5 max			
Pedestal	mV	25 typ, 100 max			
Pedestal Tempco	μV/°C	60 typ, 150 max			
Monotonicity	bits	12			
DYNAMIC CHARACTERISTICS					
Settling Time (½ LSB)					
Full Scale Change	nsec	35 typ, 50 max			
1 LSB Change	nsec	20 typ			
Update Rate	MHz	35 min			
Slew Rate	V/μsec	400 min			
Glitch Amplitude (20 MHz Filtered)	mV	14 max			
Glitch Duration (20 MHz Filtered)	nsec	38 max			
DIGITAL INPUTS					
Logic Compatibility		ECL			
Data Inputs					
Logic 1	V	−0.81 to −0.96 (100μA max)			
Logic 0	V	−1.65 to −1.85 (1 A max)			
Coding					
Unipolar		Complementary Binary			
Bipolar		Complementary Offset Binary			
ANALOG OUTPUTS					
Voltage Range	V	+0.5 max			
Steady State Current	mA	±1 max (for 0.01%)			
Transient Current	mA	±50 max			
Output Impedance	Ohms	5 typ, 10 max			
REFERENCE AND SIGN OFFSET					
Internal +10.000V Ref					
Accuracy	%FS	±0.1 max			
Max Current Out	mA	15 max			
Optional External Ref	V	+10 ±10%			
Ref Current Requirement					
Ref Input	mA	4.0 typ, 4.4 max			
Sign Offset	mA	8.0 typ, 8.8 max			
POWER SUPPLIES					
Voltage	V	+15	−15	−5.2	−1.3
Regulation for Full Accuracy	%	±2	±2	±5	±3
Current	mA typ	85	112	45	0.5
	mA max	100	125	65	2.0
TEMPERATURE RANGE					
-1 Option (Case)	°C	−55 to +125			
-3 Option (Case)	°C	0 to + 70			
Storage	°C	−65 to +150			
PHYSICAL CHARACTERISTICS					
Package (each hybrid)		24 Pin DDIP			
Size	in (mm)	1.4 x 0.8 x 0.2 (35.56 x 20.32 x 5.08)			
Weight	oz (g)	0.4 (11.2)			

INTRODUCTION

The DAC-02315 and DGL-02316 is composed of two hybrids: a D/A converter and track/hold deglitcher. These modules may be purchased separately by the user to assemble in his own system. The DAC-04300 evaluation card includes, in addition to the hybrid pair, TTL/ECL translators, input latches, trim potentiometers and a careful layout with distributed capacitors to optimize glitch and settling time characteristics. Figure 2 illustrates the DAC-04300 Evaluation Card schematic as a layout example.

The DAC-02315 generates analog output currents which are digitally controlled, binary weighted, discrete fractions of a reference voltage. Typically, the internal reference of the DAC is used for this purpose, although external regulated references may also be employed. The analog output is controlled by a ladder network of thin film precision resistors, controlled by bipolar transistor switches turned on and off in accordance with the digital input code.

The DGL-02316 track/hold deglitcher includes a voltage holding capacitor connected to the input signal through a switch. The input signal and output voltages are both buffered by amplifiers. The switch is controlled by an ECL logic gate signal which determines whether the holding capacitor voltage and output voltage will track the input signal (switch closed, logic 0) or will be held constant, retaining the value of the input at the moment the switch opens (switch open, logic 1). Figure 3 illustrates output waveforms of the DAC-02315/DGL-02316.

The following applications information includes the characteristics both of the DAC-04300 evaluation card and of the individual modules as part of a D/A converter.

DEGLITCHING

Glitches (voltage spikes) in the output of the conventional D/A converters are primarily caused by data skew and by switches which cause faster turn-on than turn-off times. Thus, whenever a code change occurs, there will be a short period of time (measured in nsec) when some spurious codes will exist. The DAC will attempt to follow these codes, resulting in a transient known as a glitch. The worst case occurs at the major carry point when the input codes are transitioning from 1000...0 to 0111...1. The spurious code may then be 1111...1, and the D/A output will momentarily slew full scale.

The DAC-02315/DGL-02316 minimizes these glitches by using a carefully designed low transient track and hold amplifier (deglitcher) after the D/A. Thus, the deglitcher can be gated into the hold mode during the D/A output transient and released into the track mode after the transients have settled out. The resultant output then makes a very clean transition from one value to another. Using this technique, glitches are not only greatly reduced, but are only a function of deglitcher design, and hence are the same for any transition and can be effectively filtered out.

INPUT LATCHES

Input latches must be employed in order to minimize data skew and digital feedthrough errors associated with high speed digital circuitry. ECL MC-10H76 registers are recommended either directly or in tandem with TTL/ECL MC-10124 translators, as shown in the schematic in figure 2. Figure 4 illustrates an appropriate input latch configuration.

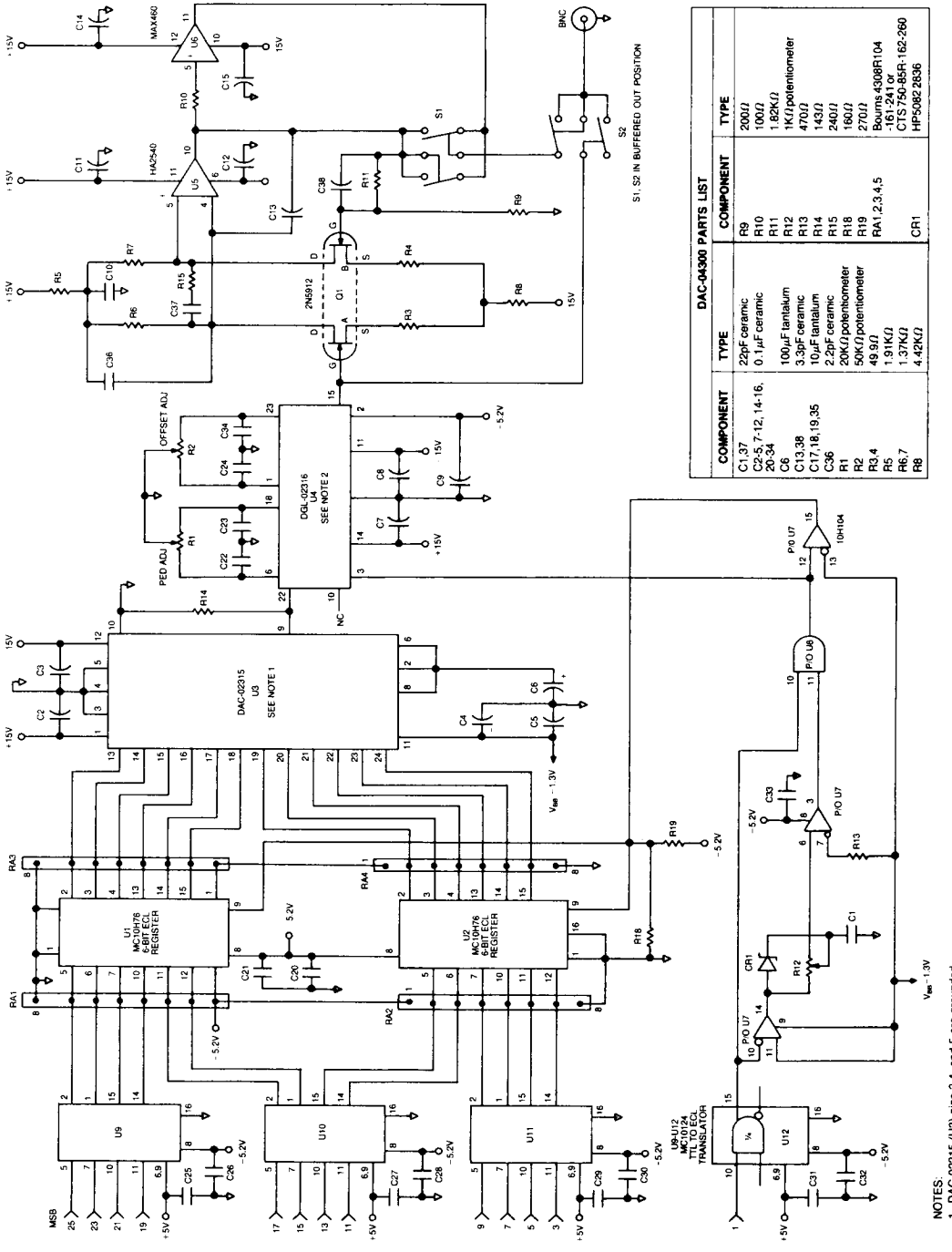
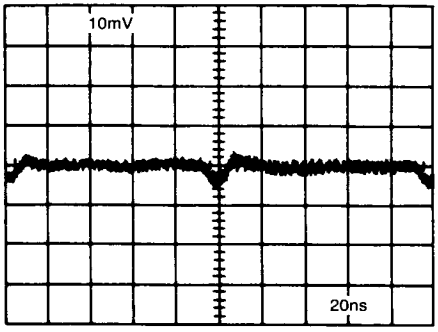
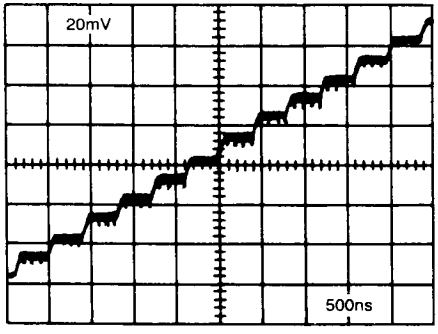


FIGURE 2. DAC-04300 EVALUATION CARD SCHEMATIC



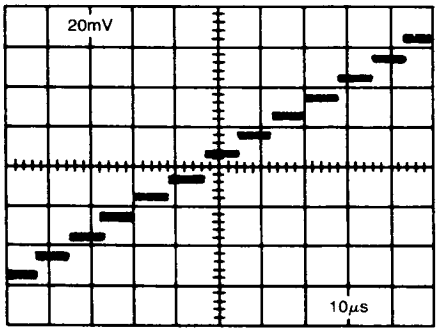
10MHz Clock, 10MHz Filter

MAJOR TRANSITION

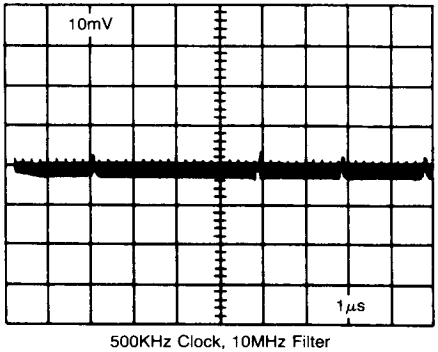


10MHz Clock, 10MHz Filter

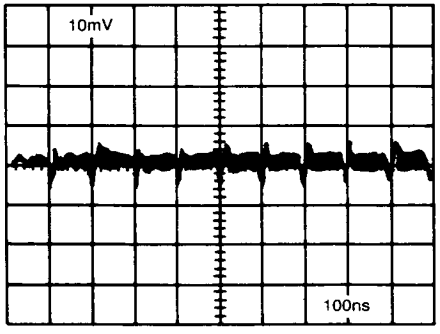
MAJOR TRANSITION



500KHz Clock, 10MHz Filter



500KHz Clock, 10MHz Filter



10MHz Clock, 10MHz Filter

Note: All scope photos referenced to ±5V FSR

FIGURE 3. OUTPUT WAVEFORMS

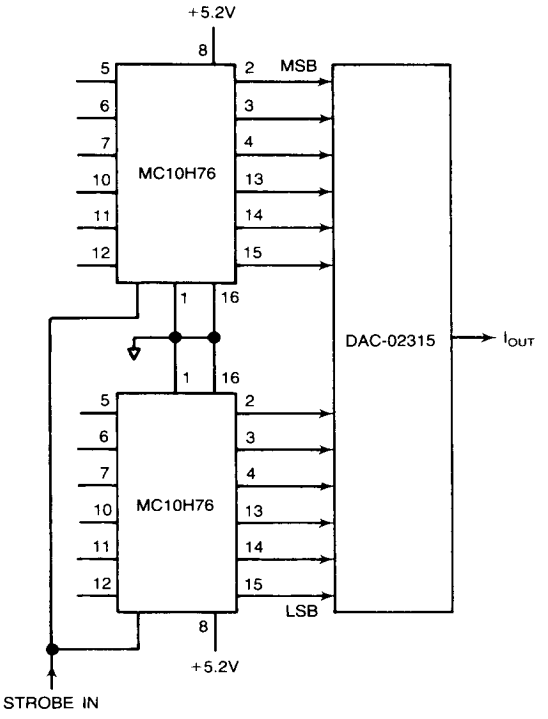


FIGURE 4. INPUT LATCH CONFIGURATION

TIMING

As illustrated in figure 5, the user's strobe pulse activates the timing circuit in the deglitcher. The timing circuit simultaneously opens the T/H amplifier switch so that its output remains constant. The latch is activated so that the input data bits are converted to an analog current by the D/A converter. After the analog current conversion has been completed, the T/H amplifier switch is closed again. The T/H amplifier then tracks the D/A converter, converting the D/A current into a voltage. The system output becomes stable after the T/H settles out.

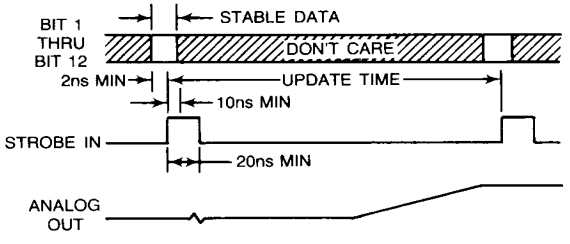


FIGURE 5. DAC-02315/DGL-02316 OUTPUT WAVEFORMS

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DAC-02315/DGL-02316 deglitched D/A converter, high frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be kept to a minimum; in particular, the DAC-02315 output (pin 9) and DGL-02316 analog input (pin 22).

Figure 6 illustrates a recommended layout with regard to DAC-02315/DGL-02316 and input latch relative positioning. A large area ground plane must be used to keep ground impedances as low as possible. Digital inputs and analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output must be kept as close to the D/A converter package as possible. Circuit connections to the external adjustment (offset, gain and pedestal) pins must be kept separated from digital lines to minimize noise coupling.

Figure 6 illustrates a recommended layout. Figure 12 illustrates the suggested physical positioning of these components to achieve optimal performance.

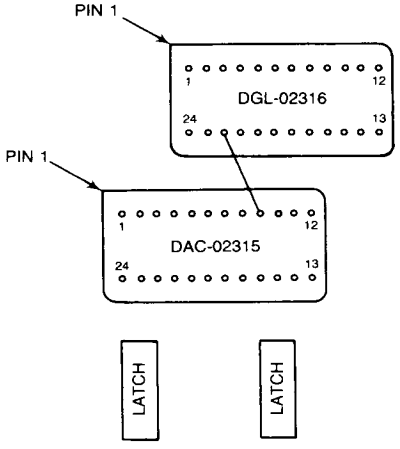


FIGURE 6. RECOMMENDED LAYOUT

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each power supply for minimum noise operation. Figure 7 illustrates a recommended power supply decoupling scheme for the DAC-02315/DGL-02316. All capacitors must be mounted as close as possible to the hybrid packages. Note that the offset and pedestal trim adjustments are also decoupled (see figure 8).

EXTERNAL TRIMS

Factory adjustment of DAC-02315/DGL-02316 gain, offset and pedestal errors result in performance which is adequate for most applications. For more critical requirements, the DGL-02316 provides pins for externally trimming offset and pedestal errors to zero. Figure 8 illustrates trim pot values and circuit connections for external trims. Figure 9 illustrates scope traces during output trim adjustments.

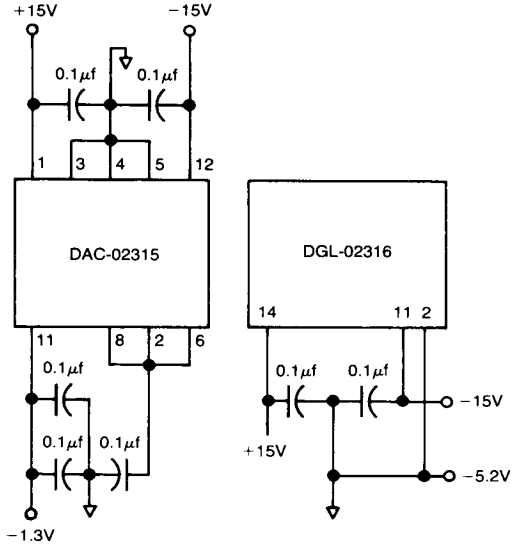


FIGURE 7. POWER SUPPLY DECOUPLING

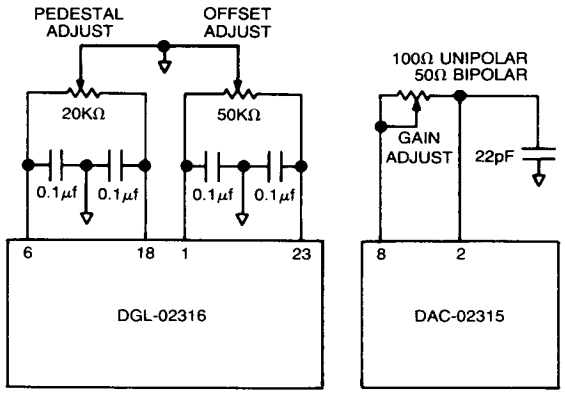


FIGURE 8. PEDESTAL, GAIN AND OFFSET TRIM CIRCUITS

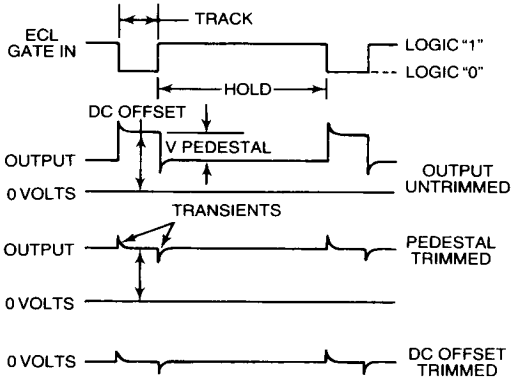


FIGURE 9. SCOPE TRACES DURING OUTPUT TRIM ADJUSTMENTS

REFERENCE

The DAC-02315 has an internal reference supply and is factory calibrated with this supply. Fixed external references of +10VDC±10% can be accomodated and the output current will be linearly proportional to the reference voltage over this range.

ANALOG OUTPUT

Figure 10 illustrates a scheme for achieving ±5V output. Since the DAC-02315/DGL-02316 is rated for ±0.5V at ±1mA, an output buffer amplifier must be used to achieve higher output voltage levels and to maintain 12 bit linearity, under heavy load.

OUTPUT CODING

The DAC-02315 accepts either complementary binary input data for unipolar analog output or bipolar complementary offset binary data for bipolar analog output. Table 2 illustrates the Bit Weight Table for the DAC-02315.

DAC-04300 EVALUATION CARD

Figure 11 illustrates the block diagram for the DAC-04300 VME demo card which incorporates TTL/ECL translators, ECL latches, DAC-02315, DGL-02316, output buffer amplifiers, and timing diagram circuitry to achieve 12-bit, 35 MHz performance. Figure 12 illustrates switch configurations for output drive options (±0.5V into 1kΩ and ±5.0V into 50Ω or 1kΩ). Figure 13 illustrates the mechanical outline of the card and Table 3 delineates the DAC-040300 evaluation card pin-out.

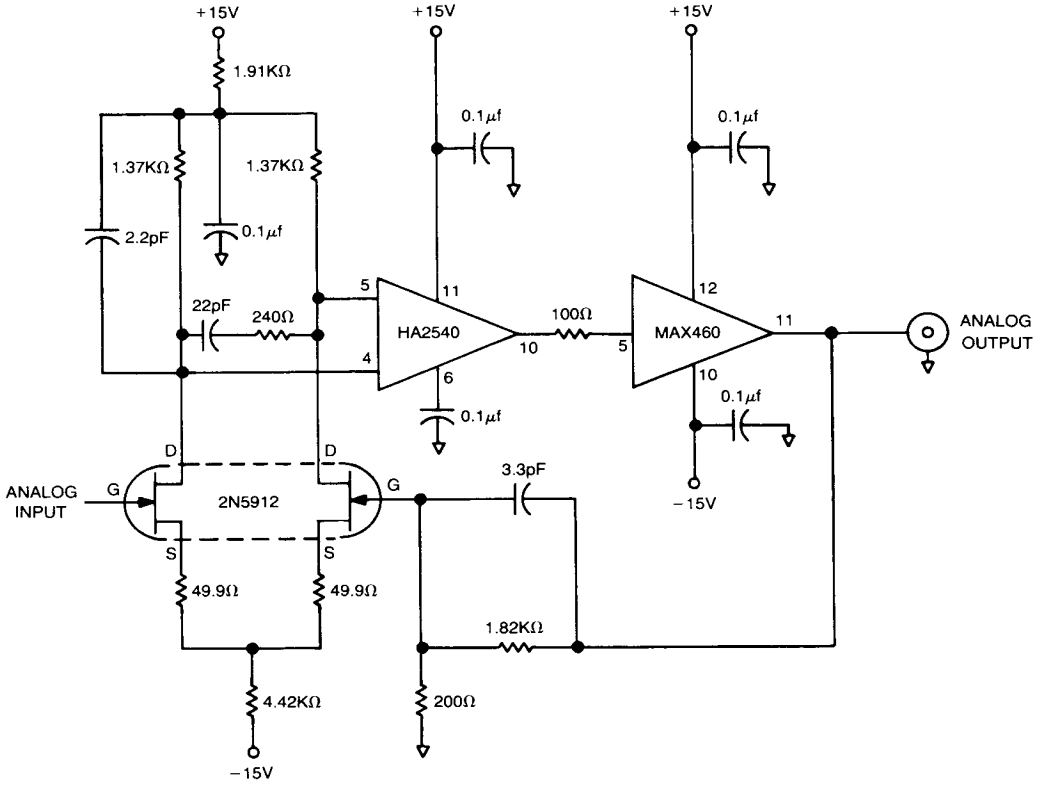


FIGURE 10. +5V ANALOG OUTPUT CIRCUIT

TABLE 2. BIT WEIGHT TABLE

ANALOG OUTPUT		DIGITAL BIT INPUTS											
UNIPOLAR COMPLEMENTARY BINARY	BIPOLAR COMPLEMENTARY OFFSET BINARY	MSB 1	2	3	4	5	6	7	8	9	10	11	LSB 12
+F.S. −1 LSB	+F.S. −1 LSB	0	0	0	0	0	0	0	0	0	0	0	0
+¾ F.S.	+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1
+½ F.S.	+1 LSB	0	1	1	1	1	1	1	1	1	1	1	0
+½ F.S.	0	0	1	1	1	1	1	1	1	1	1	1	1
+½ F.S. −1 LSB	−1 LSB	1	0	0	0	0	0	0	0	0	0	0	0
+¼ F.S.	−½ F.S.	1	0	1	1	1	1	1	1	1	1	1	1
+1 LSB	−F.S. +1 LSB	1	1	1	1	1	1	1	1	1	1	1	0
0	−F.S.	1	1	1	1	1	1	1	1	1	1	1	1

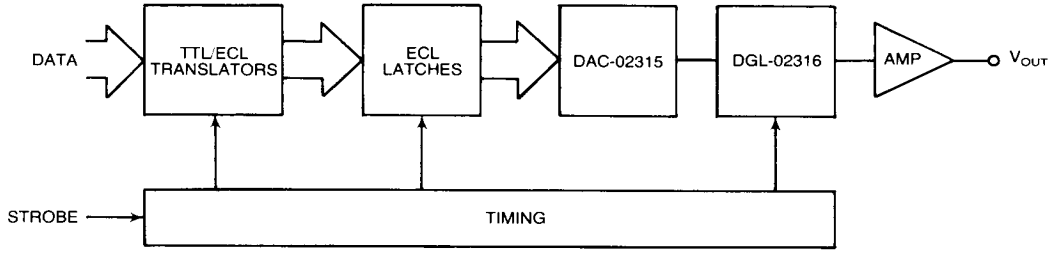


FIGURE 11. DAC-04300 EVALUATION CARD BLOCK DIAGRAM

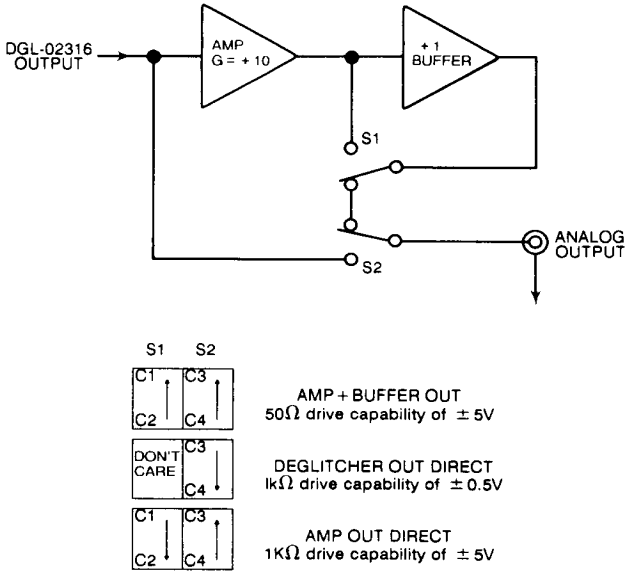
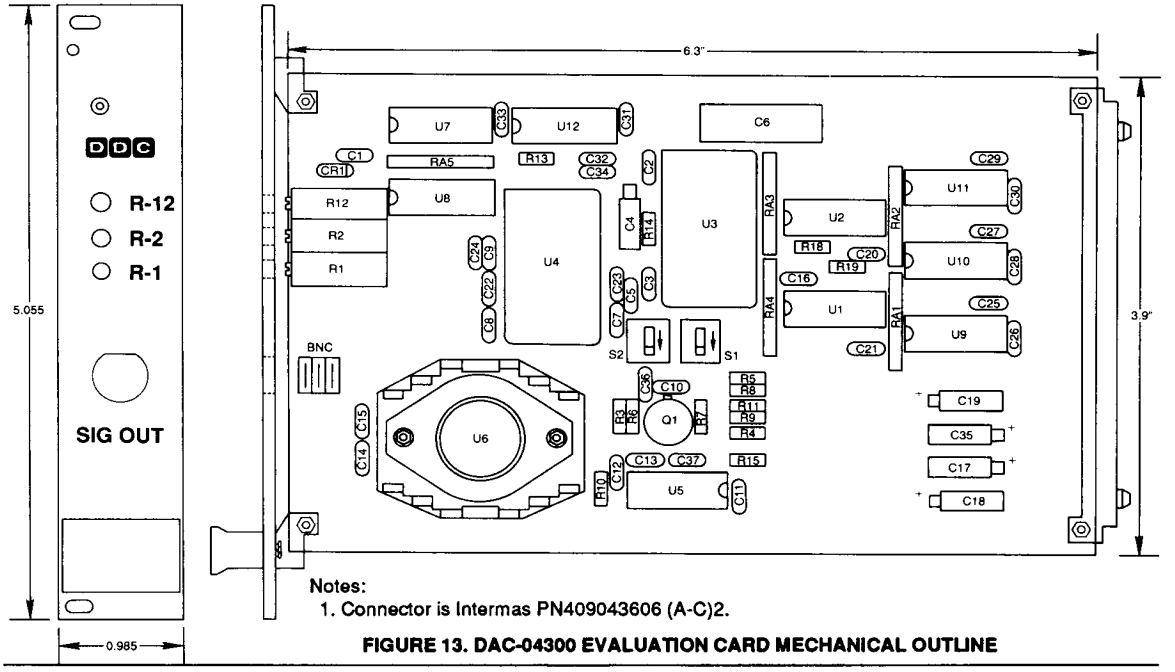


FIGURE 12. DAC-04300 OUTPUT OPTIONS



Notes:
1. Connector is Intermas PN409043606 (A-C)2.

FIGURE 13. DAC-04300 EVALUATION CARD MECHANICAL OUTLINE

TABLE 3. DAC-02315 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15VDC Input	13	Bit 1 (MSB)
2	Ref. Out	14	Bit 2
3	Ground*	15	Bit 3
4	Ground*	16	Bit 4
5	Ground*	17	Bit 5
6	Signal Offset	18	Bit 6
7	Feedback 2	19	Bit 7
8	Ref. In	20	Bit 8
9	Output	21	Bit 9
10	Feedback 1	22	Bit 10
11	$-1.3VDC = V_{bb}$	23	Bit 11
12	−15VDC	24	Bit 12 (LSB)

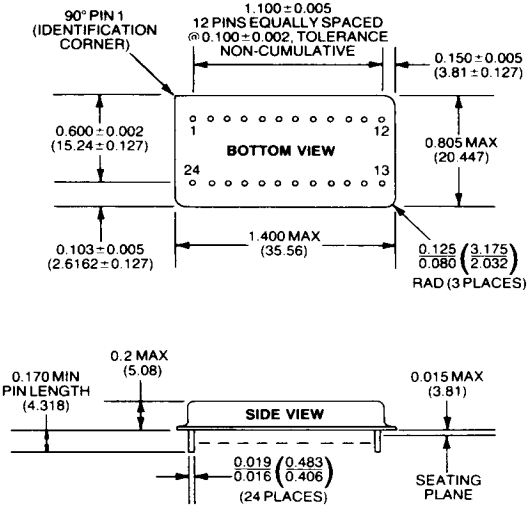
*All grounds are tied to the case.

TABLE 4. DGL-02316 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Offset Adjust	13	Analog Ground
2	−5.2 VDC	14	+15 VDC
3	Gate Input	15	Output
4	Digital Ground	16	Analog Ground
5	NC	17	NC
6	Pedestal Adjust	18	Pedestal Adjust
7	Analog Ground	19	NC
8	NC	20	NC
9	Analog Ground	21	Analog Ground
10	NC	22	Analog Input
11	−15 VDC	23	Offset Adjust
12	Analog Ground	24	Analog Ground

TABLE 5. DAC-04300 PIN FUNCTIONS

PIN	FUNCTION	PIN	FUNCTION
C1	Strobe	C18	Ground
C2	Ground	C19	Bit 4
C3	Bit 12 (LSB)	C20	Ground
C4	Ground	C21	Bit 3
C5	Bit 11	C22	Ground
C6	Ground	C23	Bit 2
C7	Bit 10	C24	Ground
C8	Ground	C25	Bit 1 (MSB)
C9	Bit 9	C26	Ground
C10	Ground	C27	−5.2 VDC
C11	Bit 8	C28	+5 VDC
C12	Ground	C29	+15 VDC
C13	Bit 7	C30	−15 VDC
C14	Ground	C31	Ground
C15	Bit 6	C32	No Connection
C16	Ground	A1 to	
C17	Bit 5	A32	Ground



Notes:
(1.) Dimensions are shown in inches (millimeters).
(2.) Load identification numbers are for reference only.
(3.) Lead spacing dimensions apply only at seating plane.
(4.) Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
(5.) Case tied to analog ground.

FIGURE 14. 24 PIN DDIP MECHANICAL OUTLINE

ORDERING INFORMATION

DAC-02315-112

- Reliability Grade:
  - 0 = Standard DDC procedures.
  - 1 = Fully compliant with MIL-STD 883.
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Operating Temperature Range (Case):
  - 1 = −55°C to +125°C
  - 3 = 0°C to +70°C
- Type:
  - DAC-02315
  - DGL-02316

DAC-04300 Evaluation Card