TS4997

2 x 1W differential input stereo audio amplifier with programmable 3D effects

Features

- Operating range from V_{CC}= 2.7V to 5.5V
- 1W output power per channel @ V_{CC}=5V, THD+N=1%, R_L=8Ω
- Ultra low standby consumption: 10nA typ.
- 80dB PSRR @ 217Hz with grounded inputs
- High SNR: 106dB(A) typ.
- Fast startup time: 45ms typ.
- Pop&click-free circuit
- Dedicated standby pin per channel
- Lead-free QFN16 4x4mm package

Applications

- Cellular mobile phones
- Notebook and PDA computers
- LCD monitors and TVs
- Portable audio devices

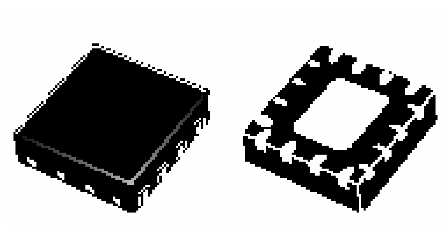
Description

The TS4997 is designed for top-class stereo audio applications. Thanks to its compact and power-dissipation efficient QFN16 package with exposed pad, it suits a variety of applications.

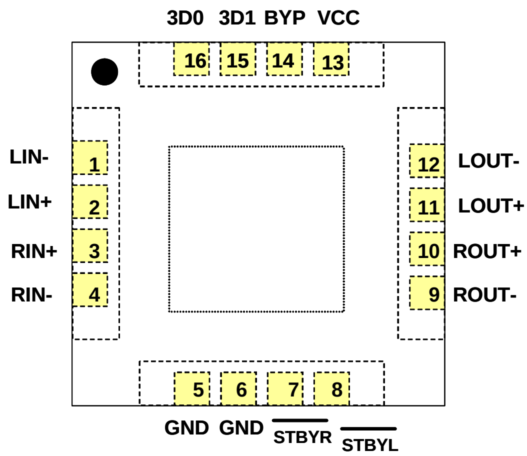
With a BTL configuration, this audio power amplifier is capable of delivering 1W per channel of continuous RMS output power into an 8Ω load @ 5V.

3D effects enhancement is programmed through a two digital input pin interface that allows more flexibility on each output audio sound channel.

QFN16 4x4mm



Pin connections (top view)



Each output channel (left and right), also has its own external controlled standby mode pin to reduce the supply current to less than 10nA per channel. The device also features an internal thermal shutdown protection.

The gain of each channel can be configured by external gain setting resistors.

Contents

1 Typical application schematics 3

2 Absolute maximum ratings 4

3 Electrical characteristics 5

4 Application information 20

4.1 General description 20

4.2 Differential configuration principle 20

4.3 Gain in typical application schematic 20

4.4 Common mode feedback loop limitations 21

4.5 Low frequency response 22

4.6 3D effect enhancement 22

4.7 Power dissipation and efficiency 23

4.8 Footprint recommendation 25

4.9 Decoupling of the circuit 25

4.10 Standby control and wake-up time t_{WU} 26

4.11 Shutdown time 27

4.12 Pop performance 27

4.13 Single-ended input configuration 27

4.14 Notes on PSRR measurement 28

5 QFN16 package information 30

6 Ordering information 32

7 Revision history 33

1 Typical application schematics

Figure 1 shows a typical application for the TS4997 with a gain of +6dB set by the input resistors.

Figure 1. Typical application schematics

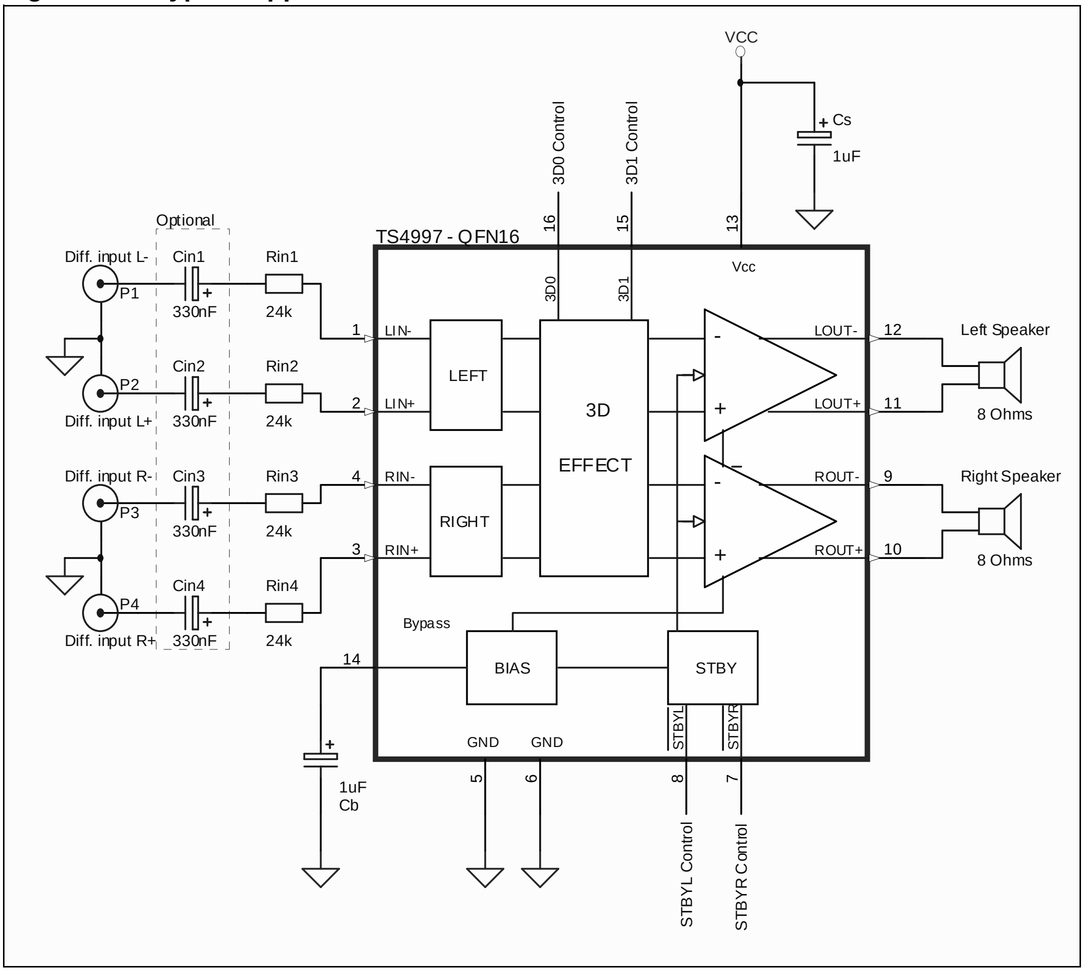


Table 1. External component descriptions

Components	Functional description
R_{IN}	Input resistors that set the closed loop gain in conjunction with a fixed internal feedback resistor (Gain = R_{feed}/R_{IN}, where R_{feed} = 50kΩ).
C_{IN}	Input coupling capacitors that block the DC voltage at the amplifier input terminal. Thanks to common mode feedback, these input capacitors are optional. However, if they are added, they form with R_{IN} a 1st order high pass filter with -3dB cut-off frequency ($f_{cut\text{-}off} = 1 / (2 \times \pi \times R_{IN} \times C_{IN})$).
C_S	Supply bypass capacitors that provides power supply filtering.
C_B	Bypass pin capacitor that provides half supply filtering.

2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient	120	°C/W
P_d	Power dissipation	Internally limited	
ESD	Human body model (3) Digital pins STBYL, STBYR, 3D0, 3D1	2 1.5	kV
ESD	Machine model	200	V
	Latch-up immunity	200	mA

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3V / GND - 0.3V.
3. All voltage values are measured from each pin with respect to supplies.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{ICM}	Common mode input voltage range	GND to V_{CC} - 1V	V
V_{IL}	3D0 - 3D1 maximum low input voltage	0.4	V
V_{IH}	3D0 - 3D1 minimum high input voltage	1.3	V
V_{STBY}	Standby voltage input: Device ON Device OFF	$1.3 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
R_L	Load resistor	≥ 4	Ω
R_{OUT}/GND	Output resistor to GND (V_{STBY} = GND)	≥ 1	MΩ
TSD	Thermal shutdown temperature	150	°C
R_{thja}	Thermal resistance junction to ambient QFN16(1) QFN16(2)	45 85	°C/W

1. When mounted on a 4-layer PCB with vias.
2. When mounted on a 2-layer PCB with vias.

3 Electrical characteristics

Table 4. V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		7.4	9.6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBYL} = GND, V_{STBYR} = GND, R_L = 8Ω		10	2000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	35	mV
P_o	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	800	1000		mW
THD + N	Total harmonic distortion + noise P_o = 700mW$_{rms}$, G = 6dB, R_L = 8Ω, 20Hz ≤ F ≤ 20kHz		0.5		%
PSRR	Power supply rejection ratio(2), inputs grounded R_L = 8Ω, G = 6dB, C_b = 1µF, V_{ripple} = 200mV$_{pp}$, 3D effect off F = 217Hz F = 1kHz		 80 75		dB
CMRR	Common mode rejection ratio(3) R_L = 8Ω, G = 6dB, C_b = 1µF, V_{incm} = 200mV$_{pp}$, 3D effect off F = 217Hz F = 1kHz		 57 57		dB
SNR	Signal-to-noise ratio A-weighted, G = 6dB, C_b = 1µF, R_L = 8Ω, 3D effect off (THD + N ≤ 0.5%, 20Hz < F < 20kHz)		108		dB
Crosstalk	Channel separation, R_L = 8Ω, G = 6dB, 3D effect off F = 1kHz F = 20Hz to 20kHz		 105 80		dB
V_N	Output voltage noise, F = 20Hz to 20kHz, R_L = 8Ω, G=6dB C_b = 1µF, 3D effect off Unweighted A-weighted		 15 10		µVrms
Gain	Gain value (R_{IN} in kΩ)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time (C_b = 1µF)		46		ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin, R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product, R_L = 8Ω		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{incm})).

Table 5. V_{CC} = +3.3V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		6.6	8.6	mA
I_{STBY}	Standby current (1) No input signal, V_{STBYL} = GND, V_{STBYR} = GND, R_L = 8Ω		10	2000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	35	mV
P_o	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	370	460		mW
THD + N	Total harmonic distortion + noise P_o = 300mW_{rms}, G = 6dB, R_L = 8Ω, 20Hz ≤ F ≤ 20kHz		0.5		%
PSRR	Power supply rejection ratio(2), inputs grounded R_L = 8Ω, G = 6dB, Cb = 1µF, V_{ripple} = 200mV_{pp}, 3D effect off F = 217Hz F = 1kHz		80 75		dB
CMRR	Common mode rejection ratio(3) R_L = 8Ω, G = 6dB, C_b = 1µF, V_{incm} = 200mV_{pp}, 3D effect off F = 217Hz F = 1kHz		57 57		dB
SNR	Signal-to-noise ratio A-weighted, G = 6dB, C_b = 1µF, RL = 8Ω, 3D effect off (THD + N ≤ 0.5%, 20Hz < F < 20kHz)		104		dB
Crosstalk	Channel separation, R_L = 8Ω, G = 6dB, 3D effect off F = 1kHz F = 20Hz to 20kHz		105 80		dB
V_N	Output voltage noise, F = 20Hz to 20kHz, R_L = 8Ω, G=6dB C_b = 1µF, 3D effect off Unweighted A-weighted		15 10		µVrms
Gain	Gain value (R_{IN} in kΩ)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time (C_b = 1µF)		47		ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product R_L = 8Ω		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{incm})).

Table 6. V_{CC} = +2.7V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, left and right channel active		6.2	8.1	mA
I_{STBY}	Standby current (1) No input signal, V_{STBYL} = GND, V_{STBYR} = GND, R_L = 8Ω		10	2000	nA
V_{oo}	Output offset voltage No input signal, R_L = 8Ω		1	35	mV
P_o	Output power THD = 1% Max, F = 1kHz, R_L = 8Ω	220	295		mW
THD + N	Total harmonic distortion + noise P_o = 200mW_{rms}, G = 6dB, R_L = 8Ω, 20Hz ≤ F ≤ 20kHz		0.5		%
PSRR	Power supply rejection ratio(2), inputs grounded R_L = 8Ω, G = 6dB, Cb = 1µF, V_{ripple} = 200mV_{pp}, 3D effect off F = 217Hz F = 1kHz		 76 73		dB
CMRR	Common mode rejection ratio(3) R_L = 8Ω, G = 6dB, C_b = 1µF, V_{incm} = 200mV_{pp}, 3D effect off F = 217Hz F = 1kHz		 57 57		dB
SNR	Signal-to-noise ratio A-weighted, G = 6dB, C_b = 1µF, RL = 8Ω, 3D effect off (THD + N ≤ 0.5%, 20Hz < F < 20kHz)		102		dB
Crosstalk	Channel separation, R_L = 8Ω, G = 6dB, 3D effect off F = 1kHz F = 20Hz to 20kHz		 105 80		dB
V_N	Output voltage noise, F = 20Hz to 20kHz, R_L = 8Ω, G=6dB C_b = 1µF, 3D effect off Unweighted A-weighted		 15 10		µVrms
Gain	Gain value (R_{IN} in kΩ)	$\frac{40k\Omega}{R_{IN}}$	$\frac{50k\Omega}{R_{IN}}$	$\frac{60k\Omega}{R_{IN}}$	V/V
t_{WU}	Wake-up time (C_b = 1µF)		46		ms
t_{STBY}	Standby time (C_b = 1µF)		10		µs
Φ_M	Phase margin at unity gain R_L = 8Ω, C_L = 500pF		65		Degrees
GM	Gain margin R_L = 8Ω, C_L = 500pF		15		dB
GBP	Gain bandwidth product R_L = 8Ω		1.5		MHz

1. Standby mode is active when V_{STBY} is tied to GND.
2. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the sinusoidal signal superimposed upon V_{CC}.
3. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{incm})).

Table 7. Index of graphics

Description	Figure	Page
THD+N vs. output power	Figure 2 to 13	page 9 to page 10
THD+N vs. frequency	Figure 14 to 19	page 11
PSRR vs. frequency	Figure 20 to 28	page 12 to page 13
PSRR vs. common mode input voltage	Figure 29	page 13
CMRR vs. frequency	Figure 30 to 35	page 13 to page 14
CMRR vs. common mode input voltage	Figure 36	page 14
Crosstalk vs. frequency	Figure 37 to 39	page 14 to page 15
SNR vs. power supply voltage	Figure 40 to 45	page 15 to page 16
Differential DC output voltage vs. common mode input voltage	Figure 46 to 48	page 16
Current consumption vs. power supply voltage	Figure 49	page 16
Current consumption vs. standby voltage	Figure 50 to 52	page 17
Standby current vs. power supply voltage	Figure 53	page 17
Frequency response	Figure 54 to 56	page 17 to page 18
Output power vs. load resistance	Figure 57	page 18
Output power vs. power supply voltage	Figure 58 to 59	page 18
Power dissipation vs. output power	Figure 60 to 62	page 18 to page 19
Power derating curves	Figure 63	page 19

Figure 2. THD+N vs. output power

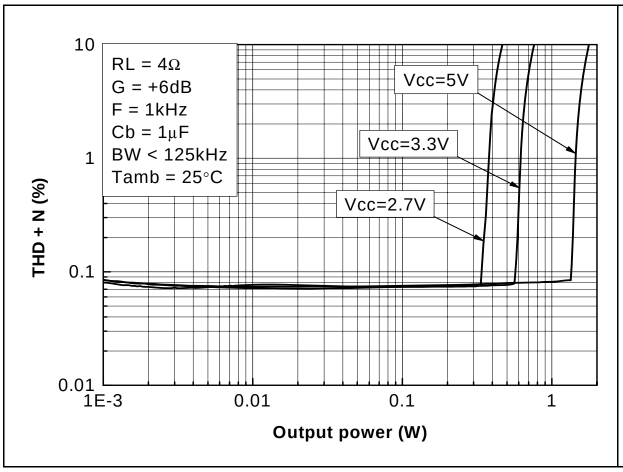


Figure 3. THD+N vs. output power

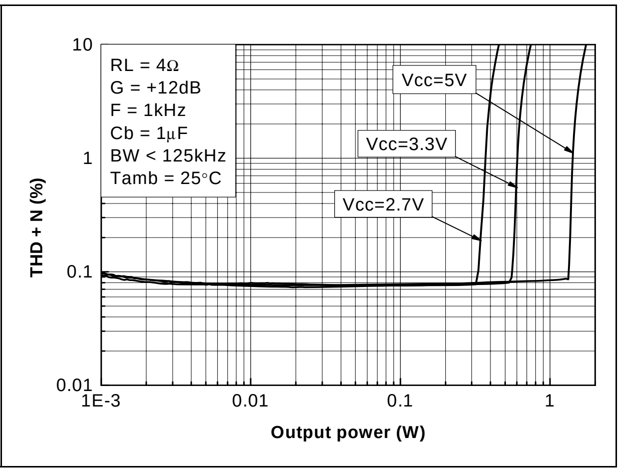


Figure 4. THD+N vs. output power

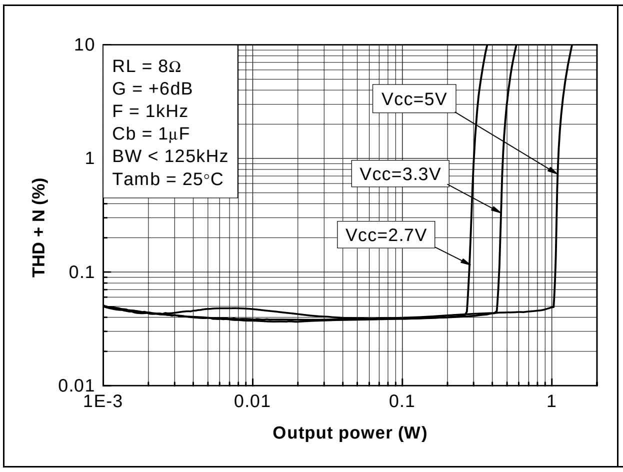


Figure 5. THD+N vs. output power

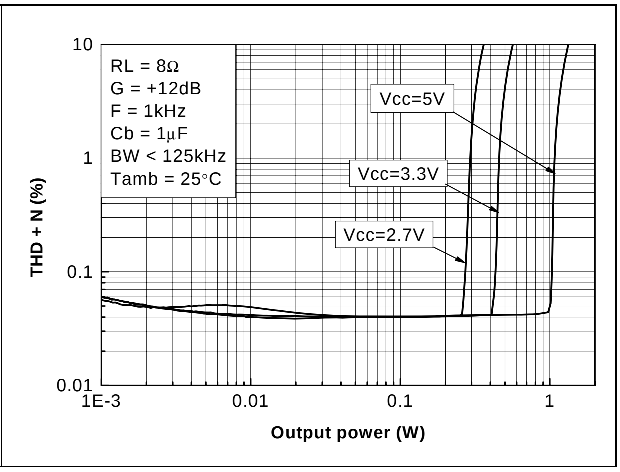


Figure 6. THD+N vs. output power

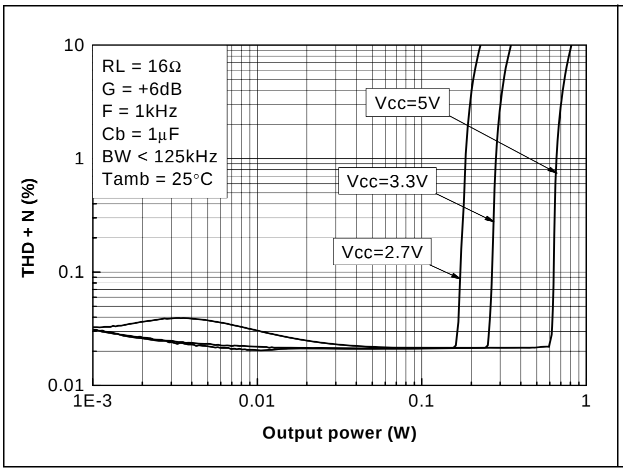


Figure 7. THD+N vs. output power

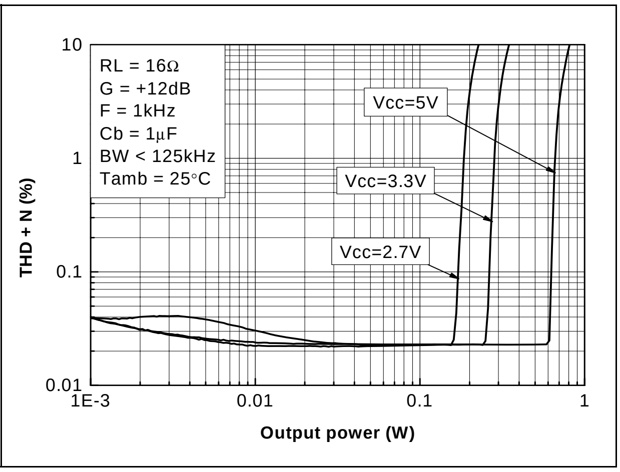


Figure 8. THD+N vs. output power

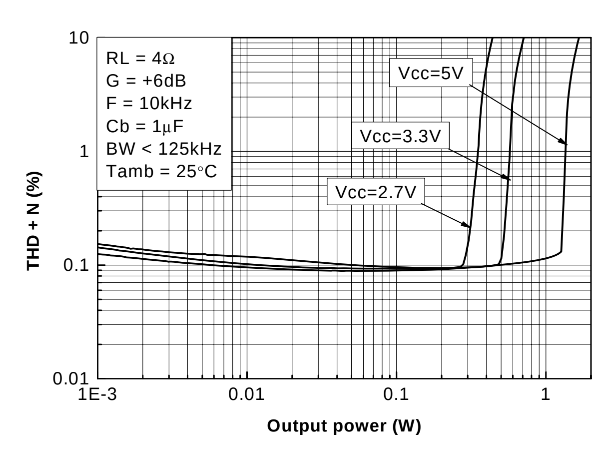


Figure 9. THD+N vs. output power

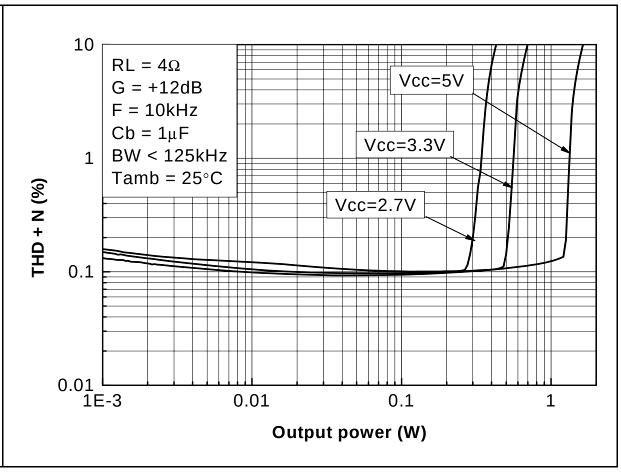


Figure 10. THD+N vs. output power

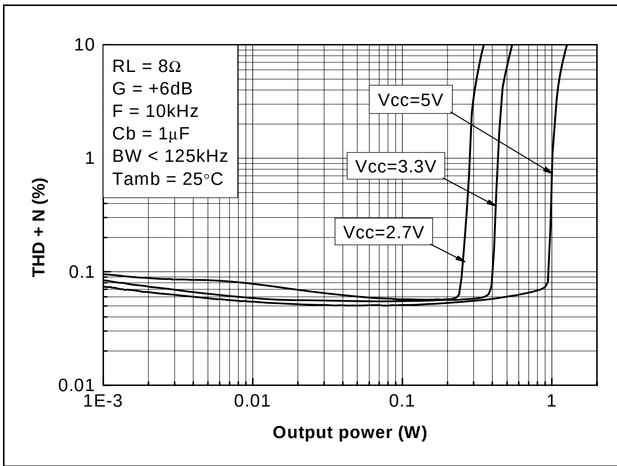


Figure 11. THD+N vs. output power

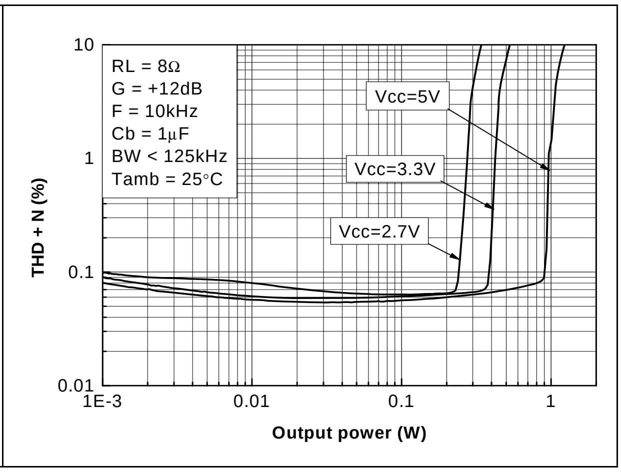


Figure 12. THD+N vs. output power

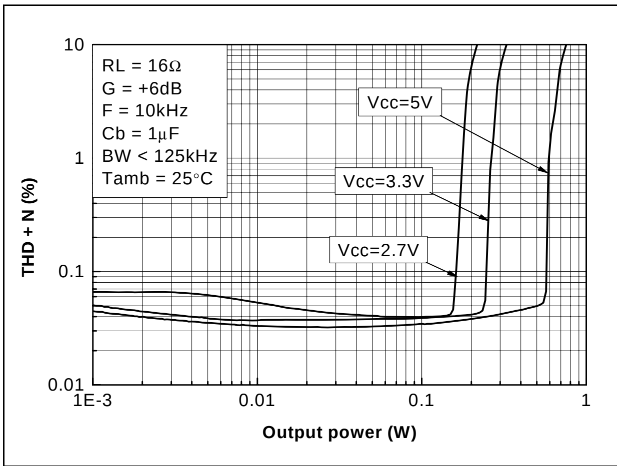


Figure 13. THD+N vs. output power

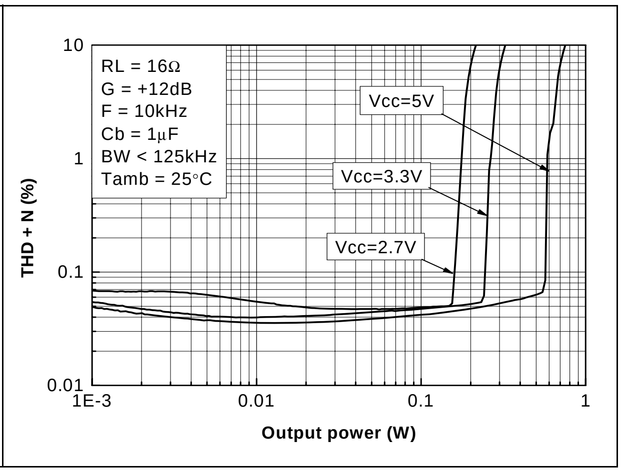


Figure 14. THD+N vs. frequency

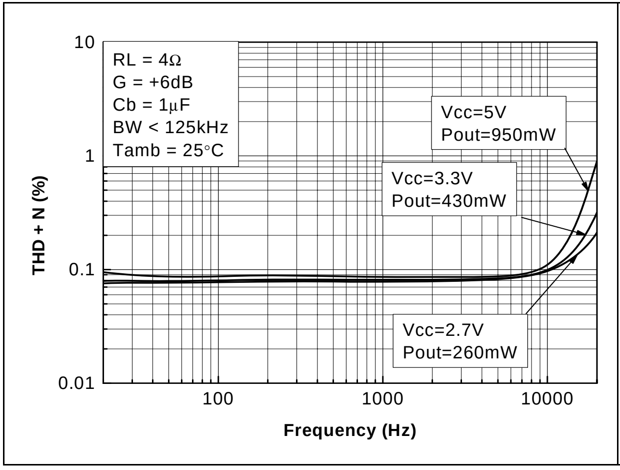


Figure 15. THD+N vs. frequency

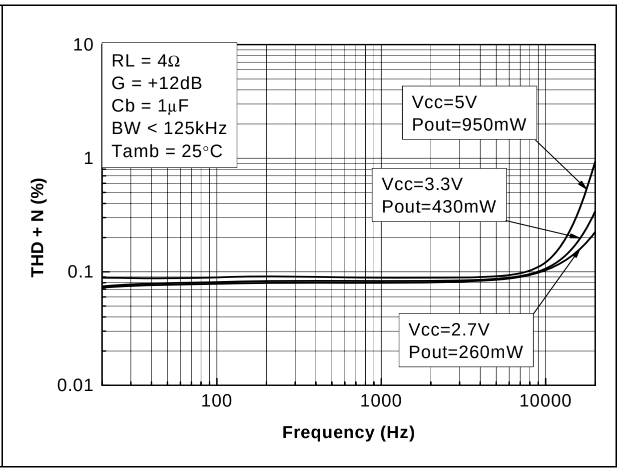


Figure 16. THD+N vs. frequency

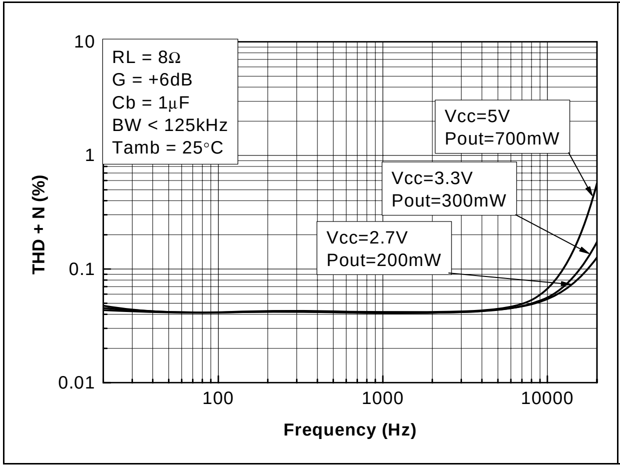


Figure 17. THD+N vs. frequency

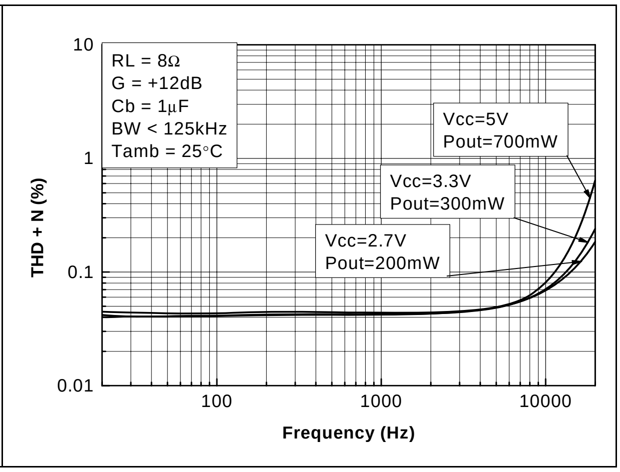


Figure 18. THD+N vs. frequency

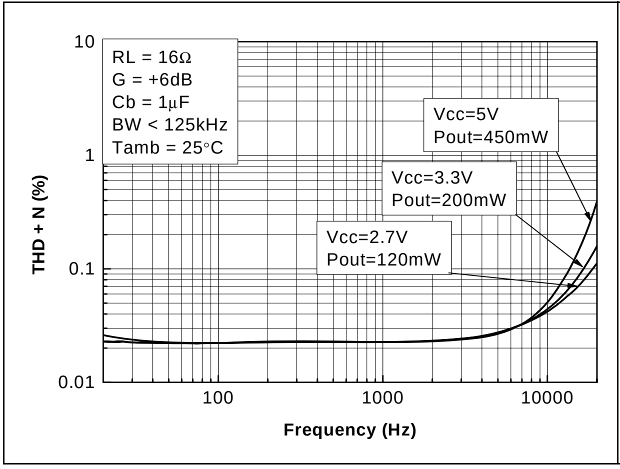


Figure 19. THD+N vs. frequency

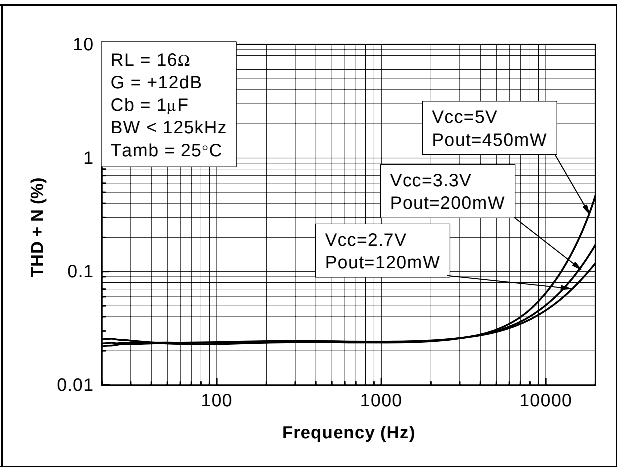


Figure 20. PSRR vs. frequency

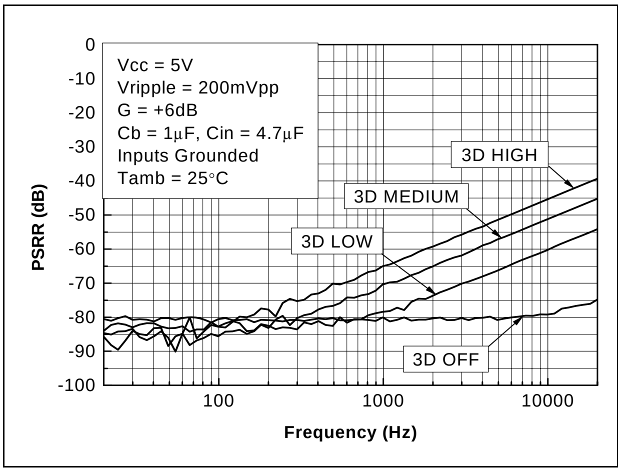


Figure 21. PSRR vs. frequency

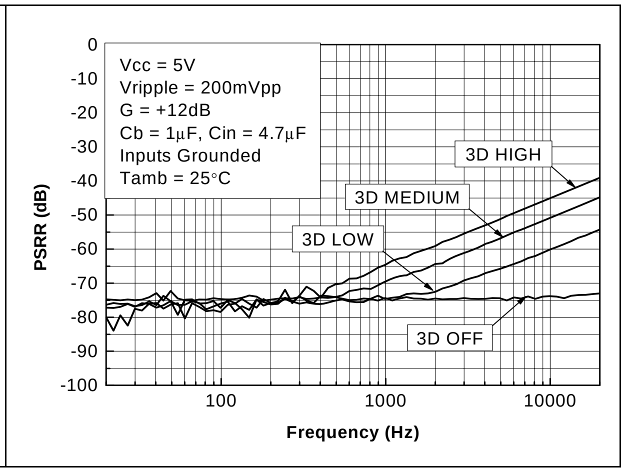


Figure 22. PSRR vs. frequency

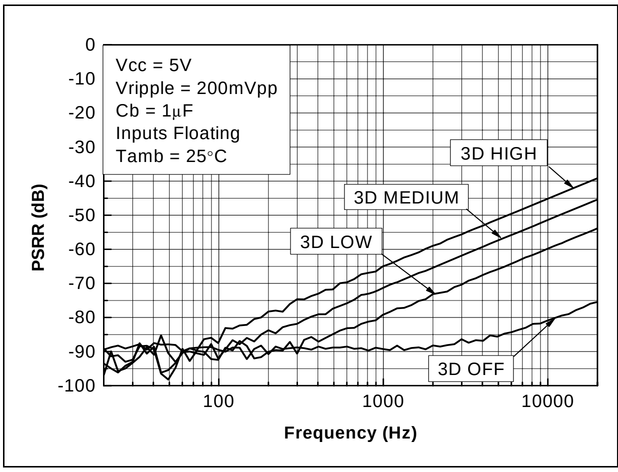


Figure 23. PSRR vs. frequency

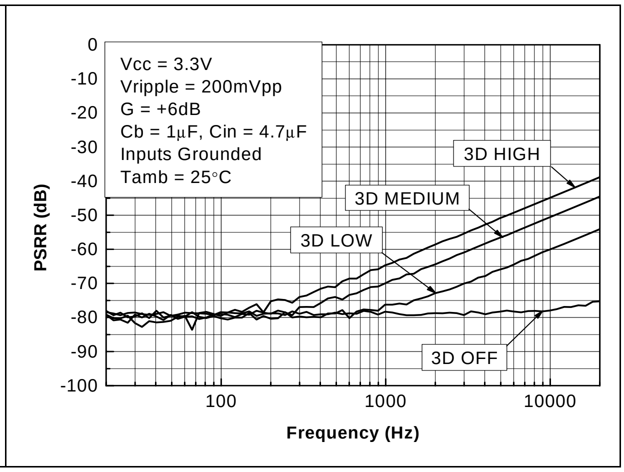


Figure 24. PSRR vs. frequency

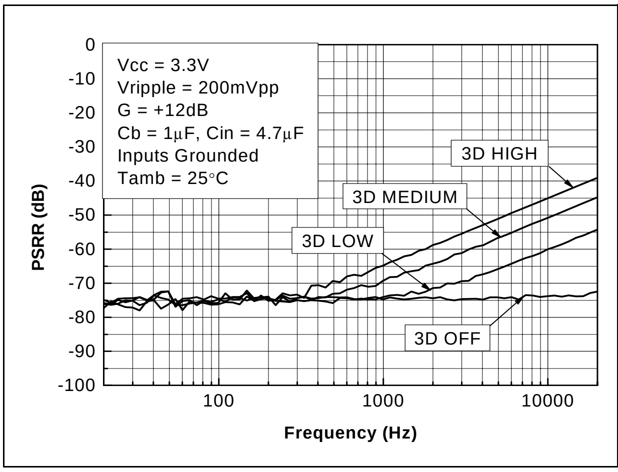


Figure 25. PSRR vs. frequency

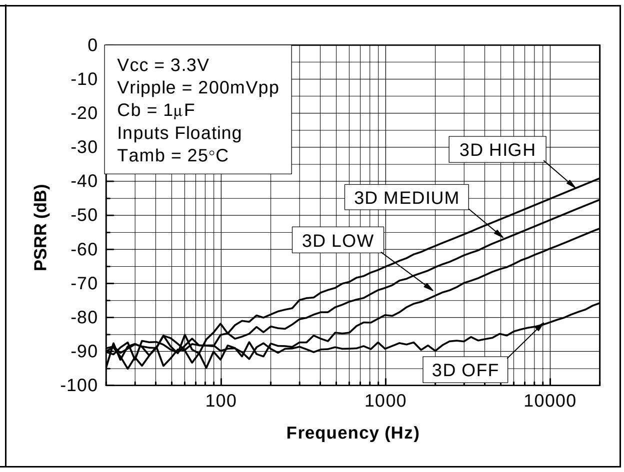


Figure 26. PSRR vs. frequency

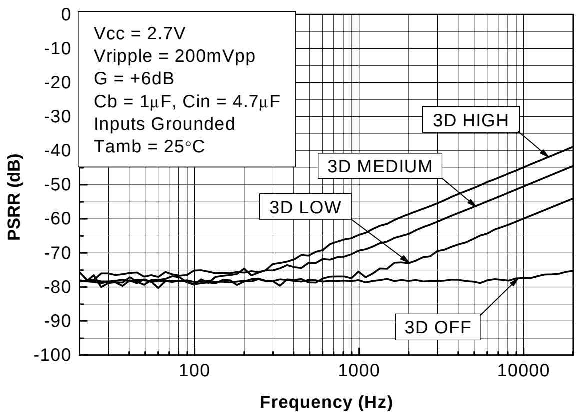


Figure 27. PSRR vs. frequency

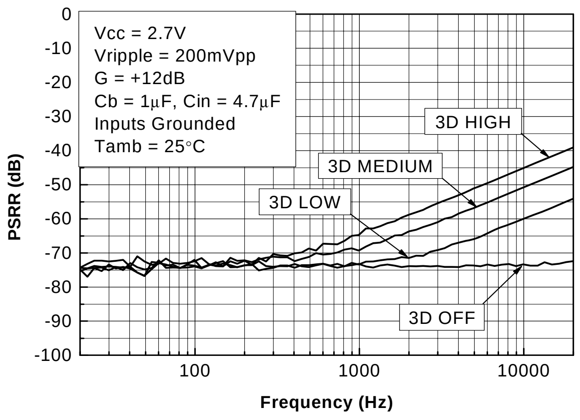


Figure 28. PSRR vs. frequency

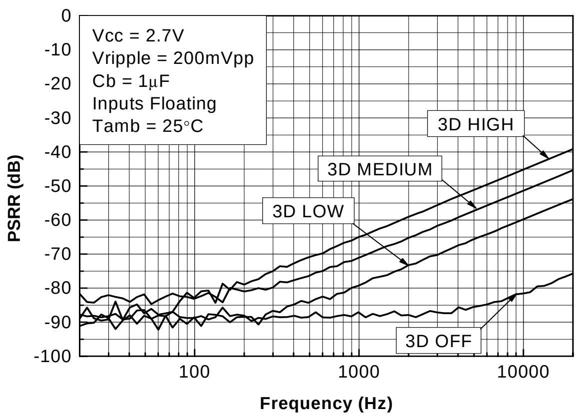


Figure 29. PSRR vs. common mode input voltage

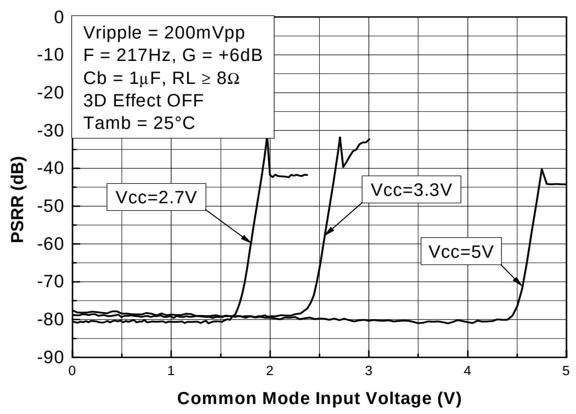


Figure 30. CMRR vs. frequency

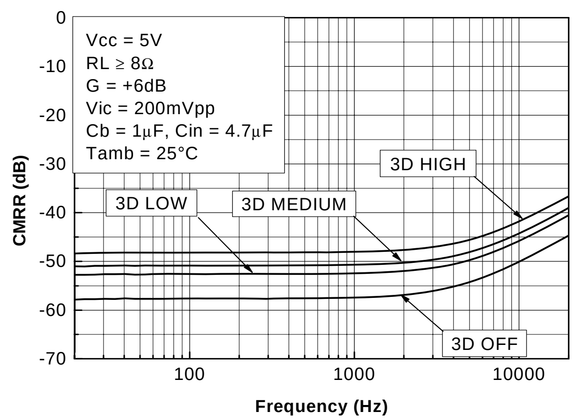


Figure 31. CMRR vs. frequency

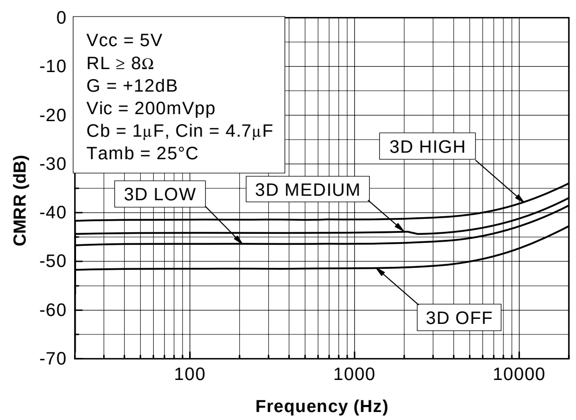


Figure 32. CMRR vs. frequency

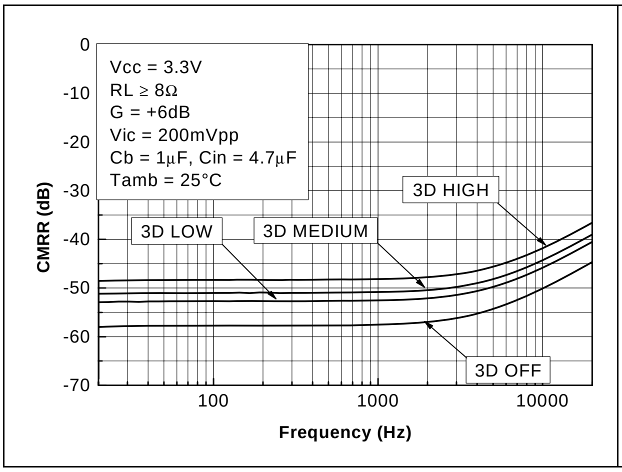


Figure 33. CMRR vs. frequency

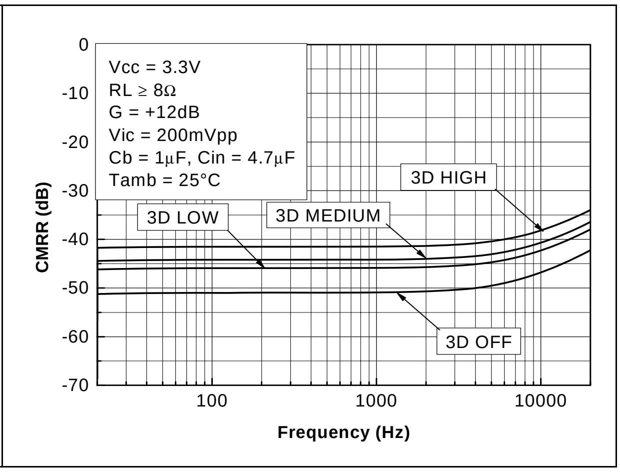


Figure 34. CMRR vs. frequency

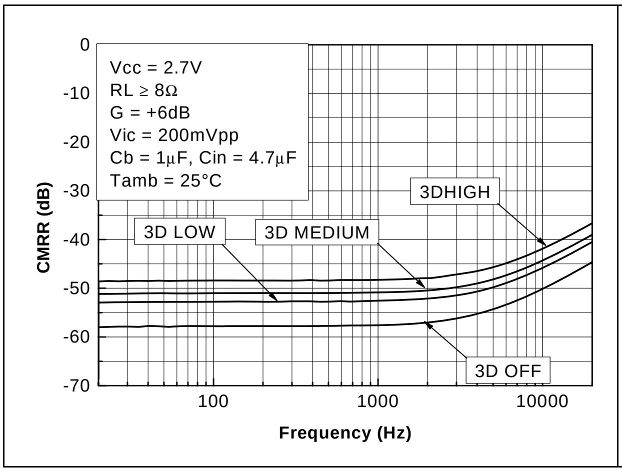


Figure 35. CMRR vs. frequency

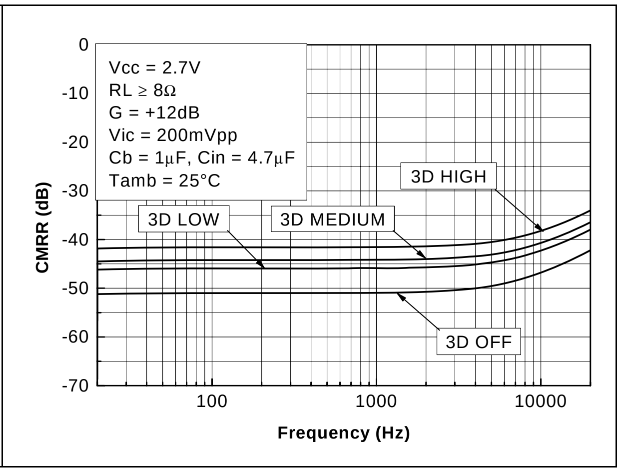


Figure 36. CMRR vs. common mode input voltage

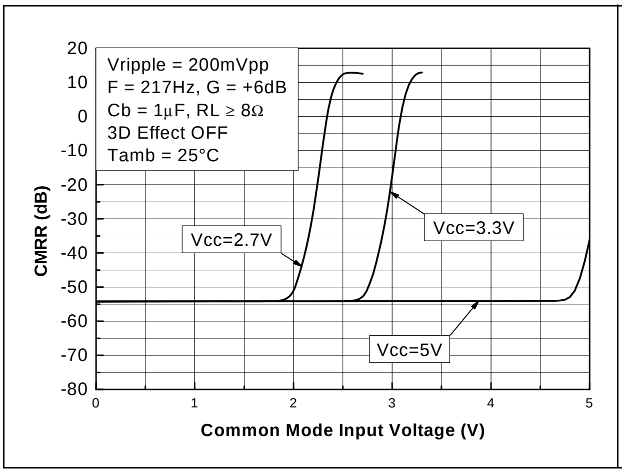


Figure 37. Crosstalk vs. frequency

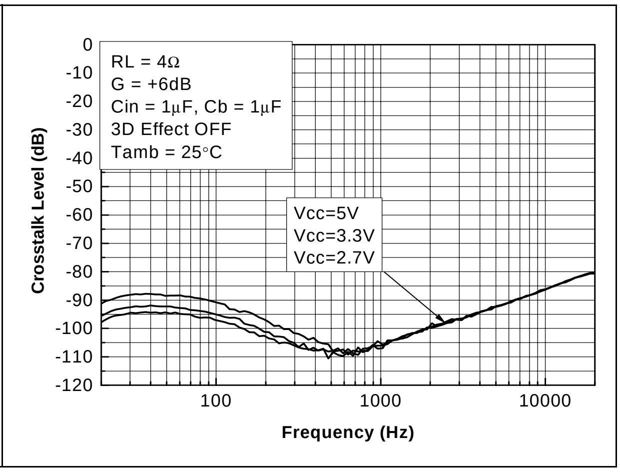


Figure 38. Crosstalk vs. frequency

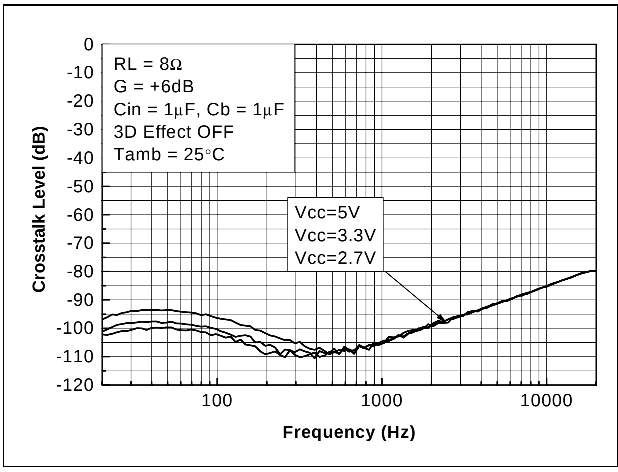


Figure 39. Crosstalk vs. frequency

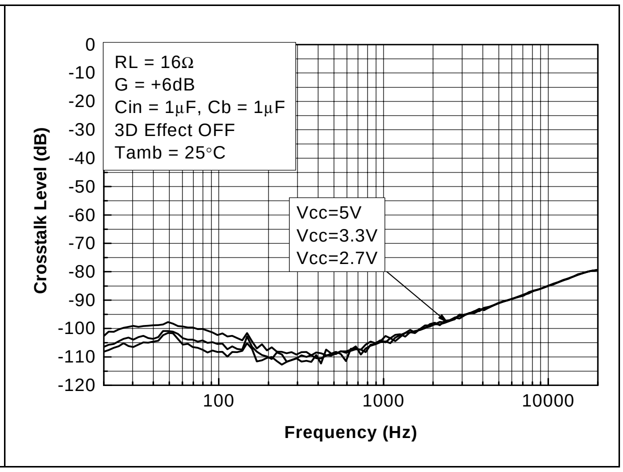


Figure 40. SNR vs. power supply voltage

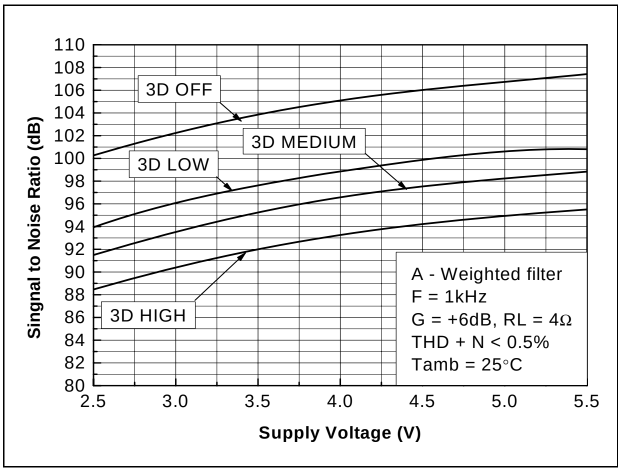


Figure 41. SNR vs. power supply voltage

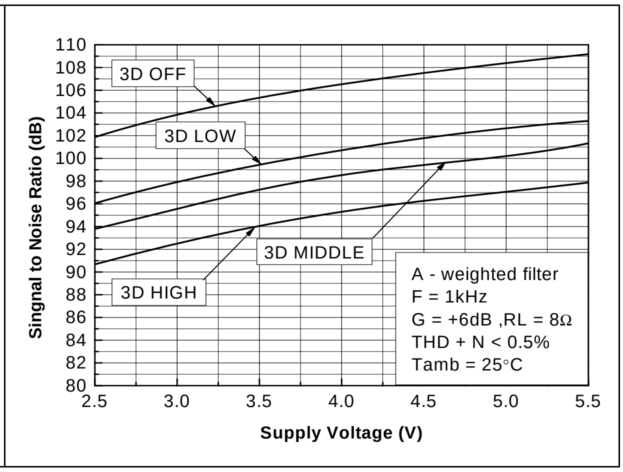


Figure 42. SNR vs. power supply voltage

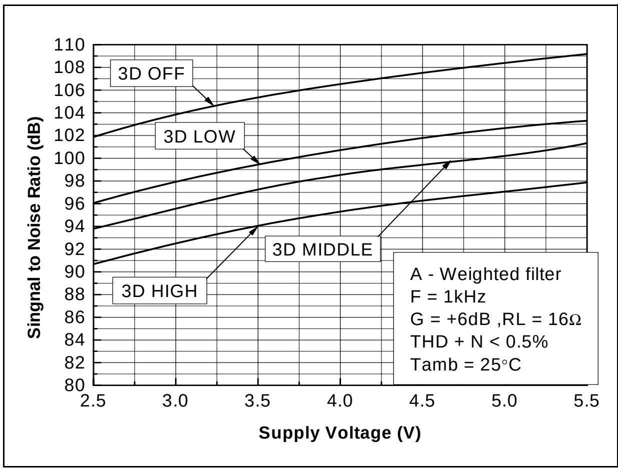


Figure 43. SNR vs. power supply voltage

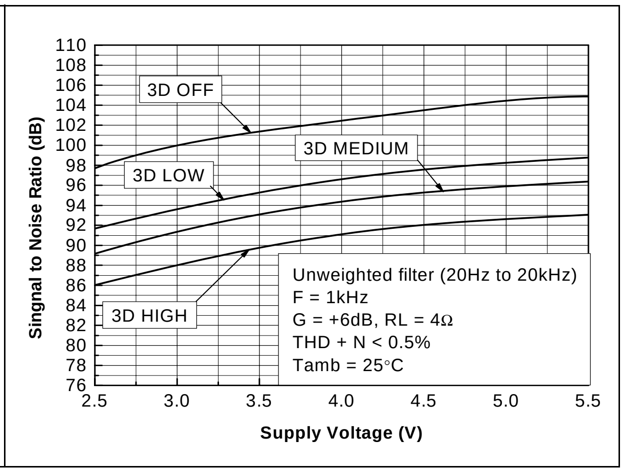


Figure 44. SNR vs. power supply voltage

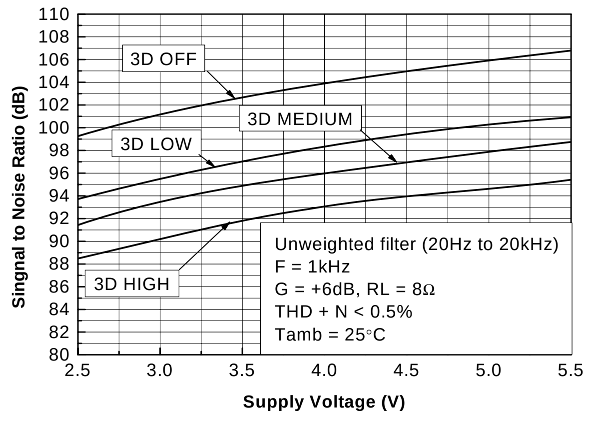


Figure 45. SNR vs. power supply voltage

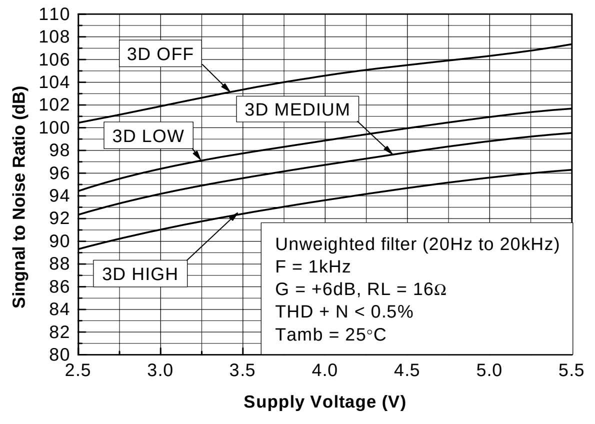


Figure 46. Differential DC output voltage vs. common mode input voltage

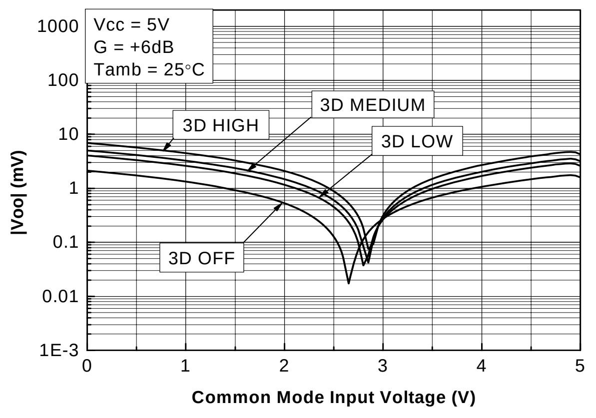


Figure 47. Differential DC output voltage vs. common mode input voltage

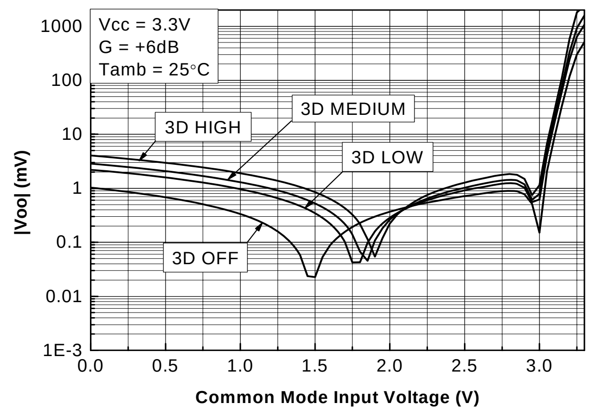


Figure 48. Differential DC output voltage vs. common mode input voltage

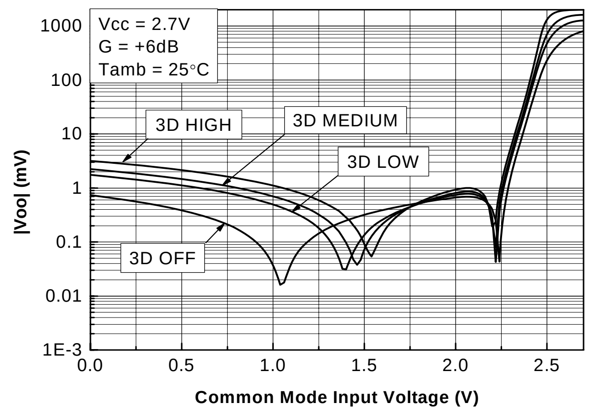


Figure 49. Current consumption vs. power supply voltage

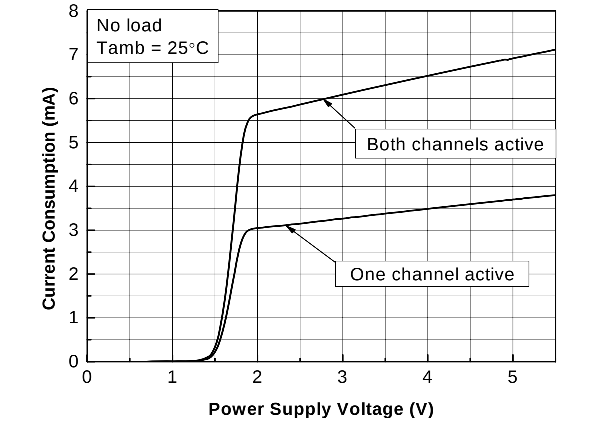


Figure 50. Current consumption vs. standby voltage

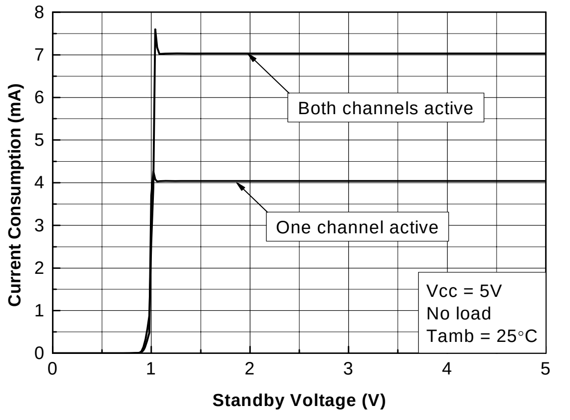


Figure 51. Current consumption vs. standby voltage

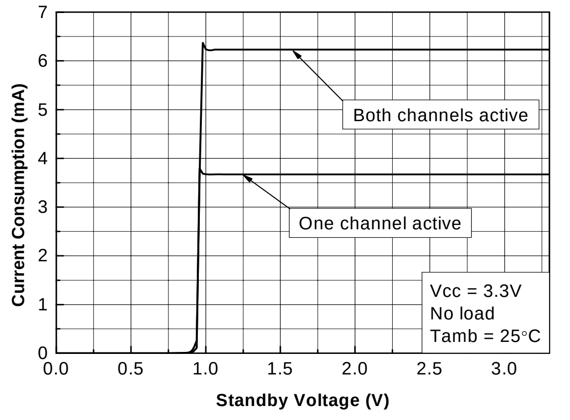


Figure 52. Current consumption vs. standby voltage

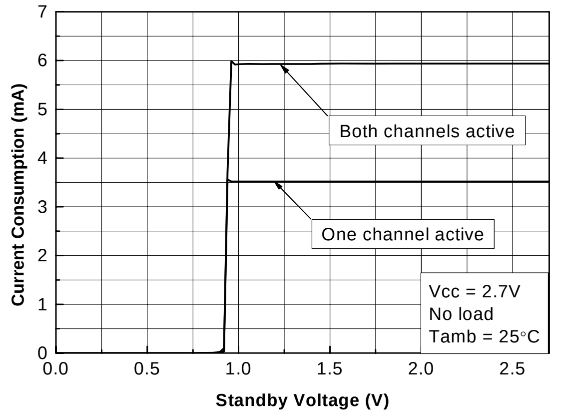


Figure 53. Standby current vs. power supply voltage

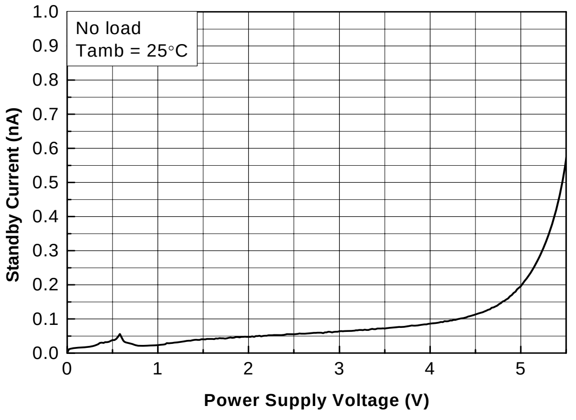


Figure 54. Frequency response

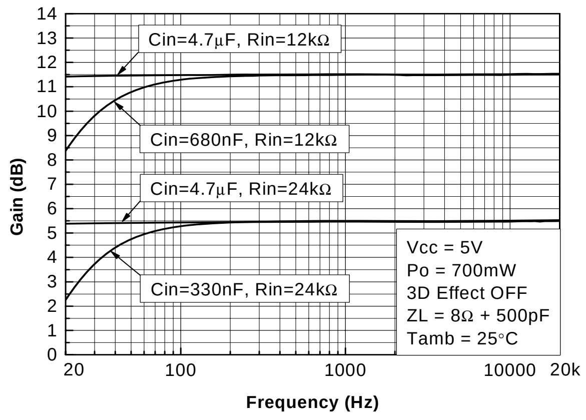


Figure 55. Frequency response

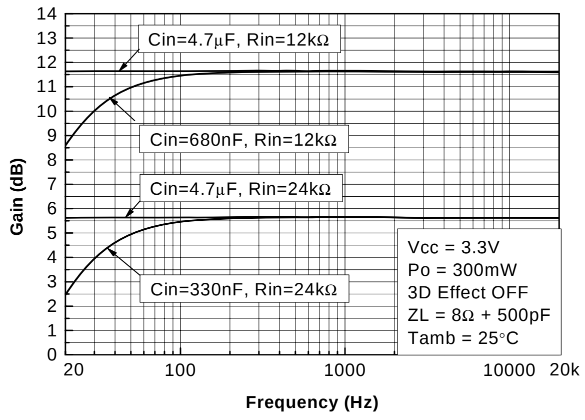


Figure 56. Frequency response

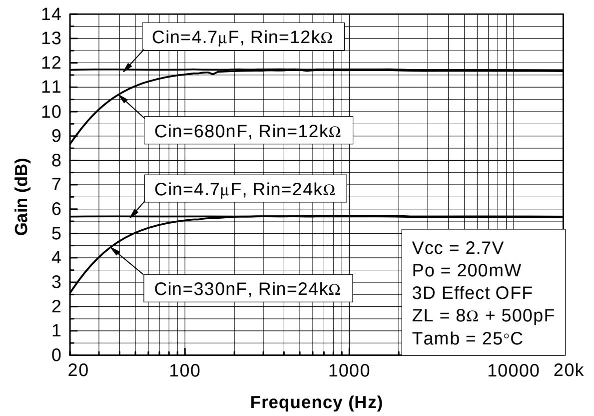


Figure 57. Output power vs. load resistance

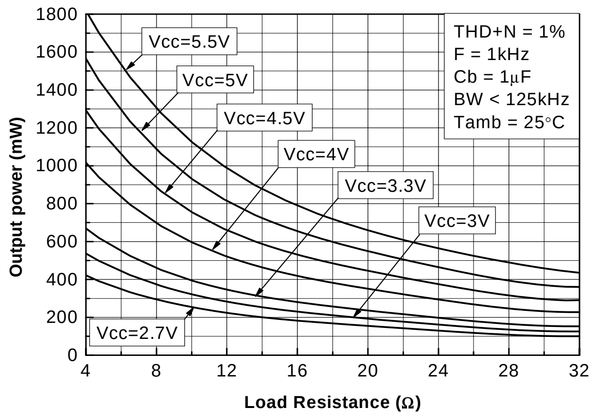


Figure 58. Output power vs. power supply voltage

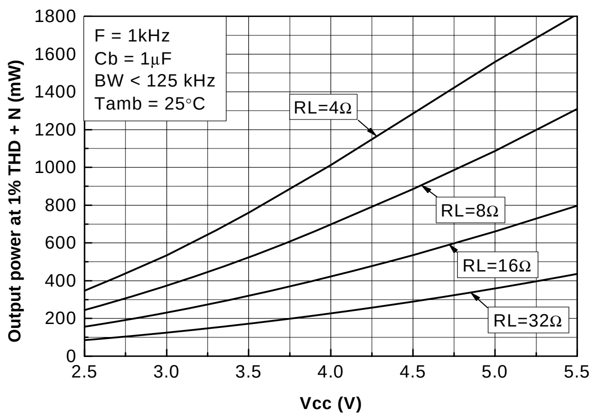


Figure 59. Output power vs. power supply voltage

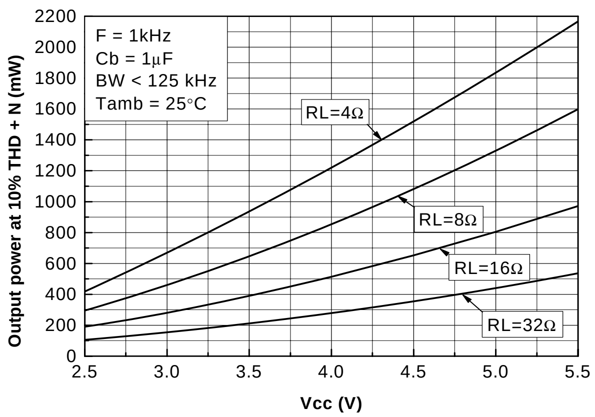


Figure 60. Power dissipation vs. output power

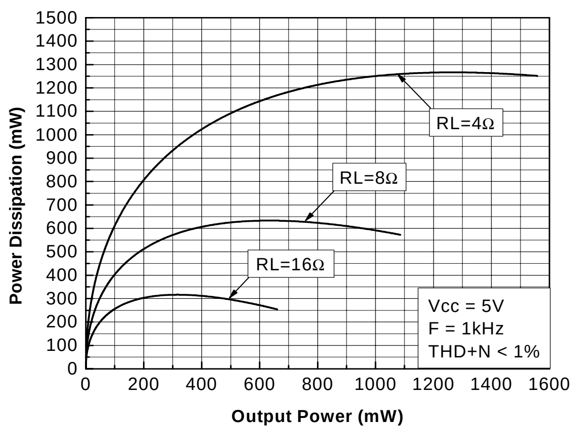


Figure 61. Power dissipation vs. output power

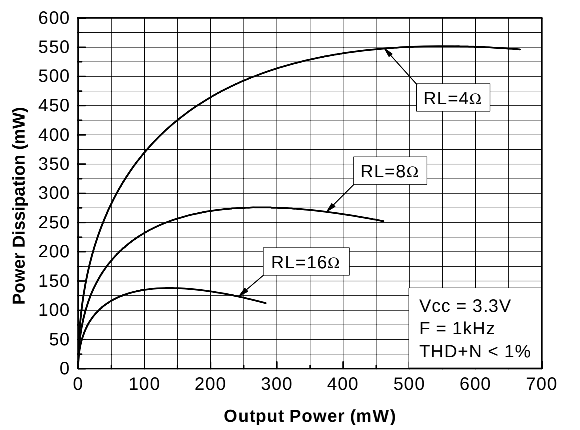


Figure 62. Power dissipation vs. output power

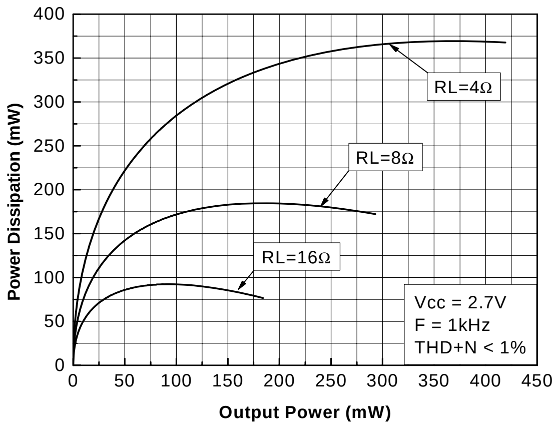


Figure 63. Power derating curves

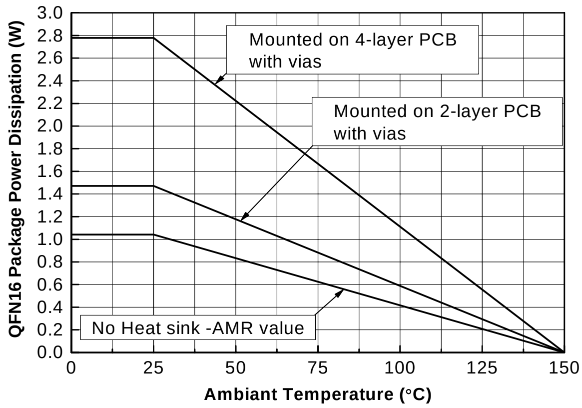


Table 8. Output noise, T_{amb} = 25°C

Conditions	3D effect level	Unweighted filter (20Hz to 20kHz) V_{CC} = 2.7V to 5.5V	A-weighted filter V_{CC} = 2.7V to 5.5V
Inputs floating	OFF	10µVrms	6µVrms
Inputs floating	LOW	18µVrms	12µVrms
Inputs floating	MEDIUM	24µVrms	15µVrms
Inputs floating	HIGH	34µVrms	22µVrms
Inputs grounded, G=6dB	OFF	15µVrms	10µVrms
Inputs grounded, G=6dB	LOW	28µVrms	19µVrms
Inputs grounded, G=6dB	MEDIUM	36µVrms	24µVrms
Inputs grounded, G=6dB	HIGH	52µVrms	35µVrms
Inputs grounded, G=12dB	OFF	20µVrms	14µVrms
Inputs grounded, G=12dB	LOW	39µVrms	26µVrms
Inputs grounded, G=12dB	MEDIUM	50µVrms	33µVrms
Inputs grounded, G=12dB	HIGH	71µVrms	48µVrms

4 Application information

4.1 General description

The TS4997 integrates two monolithic full-differential input/output power amplifiers with two selectable standby pins dedicated for each channel. The gain of each channel is set by external input resistors.

The TS4997 also features 3D effect enhancements that can be programmed through a two digital input pin interface that allows changing 3D effect levels in three steps.

4.2 Differential configuration principle

The TS4997 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows maximum output voltage swing, and therefore, to maximize the output power. Moreover, as the load is connected differentially instead of single-ended, output power is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- High PSRR (power supply rejection ratio),
- High common mode noise rejection,
- Virtually no pops&clicks without additional circuitry, giving a faster startup time compared to conventional single-ended input amplifiers,
- Easier interfacing with differential output audio DAC,
- No input coupling capacitors required due to common mode feedback loop.

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However, to reach maximum performance in all tolerance situations, it is recommended to keep this option.

The only constraint is that the differential function is directly linked to external resistor mismatching, therefore you must pay particular attention to this mismatching in order to obtain the best performance from the amplifier.

4.3 Gain in typical application schematic

A typical differential application is shown in *Figure 1 on page 3*.

The value of the differential gain of each amplifier is dependent on the values of external input resistors R_{IN1} to R_{IN4} and of integrated feedback resistors with fixed value. In the flat region of the frequency-response curve (no C_{IN} effect), the differential gain of each channel is expressed by the relation given in *Equation 1*.

Equation 1

$$A_{V_{diff}} = \frac{V_{O+} - V_{O-}}{Diff_{input+} - Diff_{input-}} = \frac{R_{feed}}{R_{IN}} = \frac{50k\Omega}{R_{IN}}$$

where $R_{IN} = R_{IN1} = R_{IN2} = R_{IN3} = R_{IN4}$ expressed in kΩ and R_{feed} = 50kΩ (value of internal feedback resistors).

Due to the tolerance on the internal 50kΩ feedback resistors, the differential gain will be in the range (no tolerance on R_{IN}):

$$\frac{40k\Omega}{R_{IN}} \le A_{V_{diff}} \le \frac{60k\Omega}{R_{IN}}$$

The difference of resistance between input resistors of each channel have direct influence on the PSRR, CMRR and other amplifier parameters. In order to reach maximum performance, we recommend matching the input resistors R_{IN1}, R_{IN2}, R_{IN3}, and R_{IN4} with a maximum tolerance of 1%.

Note: For the rest of this section, Av_{diff} will be called A_V to simplify the mathematical expressions.

4.4 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{ICM} limitation of the input stage (see *Table 3 on page 4*), the common mode feedback loop can fulfil its role only within the defined range. This range depends upon the values of V_{CC}, R_{IN} and R_{feed} (A_V). To have a good estimation of the V_{ICM} value, use the following formula:

Equation 2

$$V_{ICM} = \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times R_{feed}}{2 \times (R_{IN} + R_{feed})} = \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 50k\Omega}{2 \times (R_{IN} + 50k\Omega)} (V)$$

with V_{CC} in volts, R_{IN} in kΩ and

$$V_{ic} = \frac{Diff_{input+} + Diff_{input-}}{2} \quad (V)$$

The result of the calculation must be in the range:

$$GND \le V_{ICM} \le V_{CC} - 1V$$

Due to the +/-20% tolerance on the 50kΩ feedback resistors R_{feed} (no tolerance on R_{IN}), it is also important to check that the V_{ICM} remains in this range at the tolerance limits:

$$\frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 40k\Omega}{2 \times (R_{IN} + 40k\Omega)} \le V_{ICM} \le \frac{V_{CC} \times R_{IN} + 2 \times V_{ic} \times 60k\Omega}{2 \times (R_{IN} + 60k\Omega)} (V)$$

If the result of the V_{ICM} calculation is not in this range, an input coupling capacitor must be used.

Example: V_{CC} = 2.7V, A_V = 2, and V_{ic} = 2.2V.

With internal resistors R_{feed} = 50kΩ, calculated external resistors are $R_{IN} = R_{feed}/A_V$ = 25kΩ, V_{CC} = 2.7V and V_{ic} = 2.2V, which gives V_{ICM} = 1.92V. Taking into account the tolerance on the feedback resistors, with R_{feed} = 40kΩ the common mode input voltage is V_{ICM} = 1.87V and with R_{feed} = 60kΩ, it is V_{ICM} = 1.95V.

These values are not in range from GND to V_{CC} - 1V = 1.7V, therefore input coupling capacitors are required. Alternatively, you can change the V_{ic} value.

4.5 Low frequency response

The input coupling capacitors block the DC part of the input signal at the amplifier inputs. In the low frequency region, C_{IN} starts to have an effect. C_{IN} and R_{IN} form a first-order high pass filter with a -3dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}} (Hz)$$

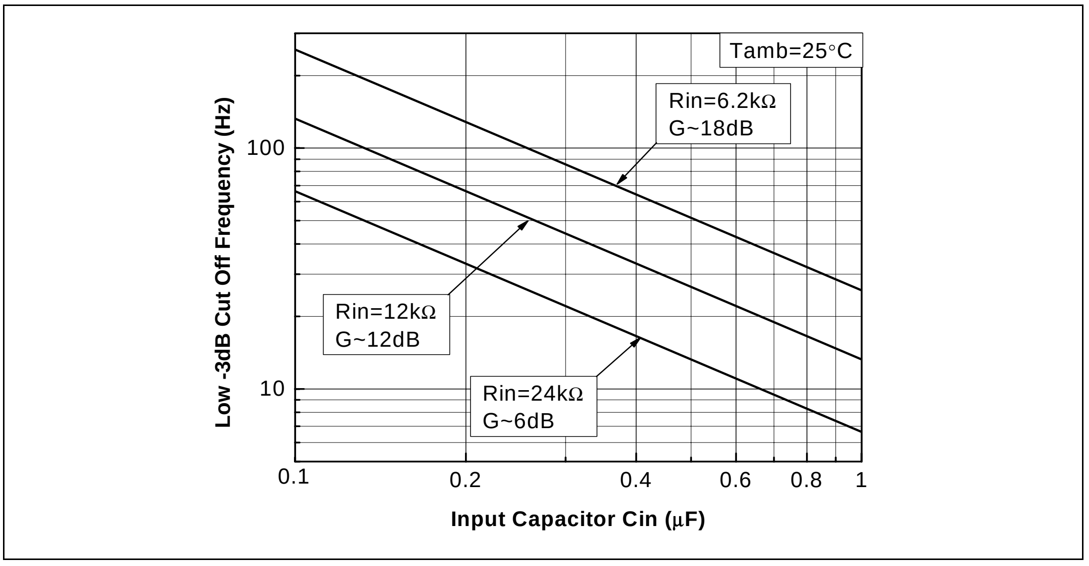
with R_{IN} expressed in Ω and C_{IN} expressed in F.

So, for a desired -3dB cut-off frequency we can calculate C_{IN}:

$$C_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times F_{CL}} (F)$$

From *Figure 64*, you can easily establish the C_{IN} value required for a -3 dB cut-off frequency for some typical cases.

Figure 64. -3dB lower cut-off frequency vs. input capacitance



4.6 3D effect enhancement

The TS4997 features 3D audio effect which can be programmed at three discrete levels (LOW, MEDIUM, HIGH) through input pins 3D1 and 3D0 which provide a digital interface. The correspondence between the logic levels of this interface and 3D effect levels are shown in *Table 9*.

The 3D audio effect applied to stereo audio signals evokes perception of spatial hearing and improves this effect in cases where the stereo speakers are too close to each other, such as in small handheld devices, or mobile equipment.

The perceived amount of 3D effect is also dependent on many factors such as speaker position, distance between speakers and listener, frequency spectrum of audio signal, or difference of signal between left and right channel. In some cases, the volume can increase when switching on the 3D effect. This factor is dependent on the composition of the stereo audio signal and its frequency spectrum.

Table 9. 3D effect settings

3D effect level	3D0	3D1
OFF	0	0
LOW	0	1
MEDIUM	1	0
HIGH	1	1

4.7 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

The output voltage is:

$$V_{out} = V_{peak} \sin\omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{{V_{peak}}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

Equation 3

$$I_{ccAVG} = 2\frac{V_{peak}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

Equation 4

$$P_{supply} = V_{CC}\, I_{ccAVG} \text{ (W)}$$

Therefore, the **power dissipated by each amplifier** is:

$P_{diss} = P_{supply} - P_{out}$ (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out} \text{(W)}$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{out}} = 0$$

and its value is:

Equation 5

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

Equation 6

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4Vcc}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The TS4997 is stereo amplifier so it has two power amplifiers. Each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of each amplifier's maximum power dissipation. It is calculated as follows:

- $P_{diss\ 1}$ = Power dissipation of left channel power amplifier
- $P_{diss\ 2}$ = Power dissipation of right channel power amplifier
- Total $P_{diss} = P_{diss\ 1} + P_{diss\ 2}$ (W)

In most cases, $P_{diss\ 1} = P_{diss\ 2}$, giving:

$$TotalP_{diss} = 2 \times P_{diss1} = \frac{4\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - 2P_{out} (W)$$

The maximum die temperature allowable for the TS4997 is 150°C. In case of overheating, a thermal shutdown protection set to 150°C, puts the TS4997 in standby until the temperature of the die is reduced by about 5°C.

To calculate the maximum ambient temperature T_{amb} allowable, you need to know:

- the power supply voltage value, V_{CC}
- the load resistor value, R_L
- the package type, R_{THJA}

Example: V_{CC}=5V, R_L=8Ω, R_{THJA}QFN16=85°C/W (with 2-layer PCB with vias).

Using the power dissipation formula given in *Equation 5*, the maximum dissipated power per channel is:

$P_{dissmax}$ = 633mW

And the power dissipated by both channels is:

Total $P_{dissmax}$ = 2 x $P_{dissmax}$ = 1266mW

T_{amb} is calculated as follows:

Equation 7

$$T_{amb} = 150°C - R_{TJHA} \times TotalP_{dissmax}$$

Therefore, the maximum allowable value for T_{amb} is:

T_{amb} = 150 - 85 x 2 x 1.266=42.4°C

If a 4-layer PCB with vias is used, R_{THJA}QFN16 = 45°C/W and the maximum allowable value for T_{amb} in this case is:

T_{amb} = 150 - 45 x 2 x 1.266 = 93°C

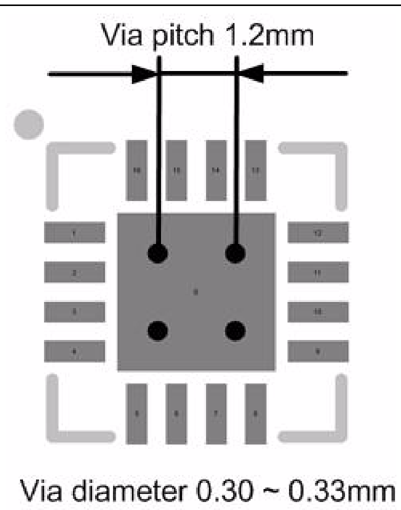
4.8 Footprint recommendation

Footprint soldering pad dimensions are given in *Figure 72 on page 31*. As discussed in the previous section, the maximum allowable value for ambient temperature is dependent on the thermal resistance junction to ambient R_{THJA}. Decreasing the R_{THJA} value causes better power dissipation.

Based on best thermal performance, it is recommended to use 4-layer PCBs with vias to effectively remove heat from the device. It is also recommended to use vias for 2-layer PCBs to connect the package exposed pad to heatsink cooper areas placed on another layer.

For proper thermal conductivity, the vias must be plated through and solder-filled. Typical thermal vias have the following dimensions: 1.2mm pitch, 0.3mm diameter.

Figure 65. QFN16 footprint recommendation



4.9 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4997: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_b.

The C_S capacitor has particular influence on the THD+N at high frequencies (above 7kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1µF, one can expect THD+N performance similar to that shown in the datasheet.

In the high frequency region, if C_S is lower than 1µF, then THD+N increases and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is greater than 1µF, then those disturbances on the power supply rail are more filtered.

The C_b capacitor has an influence on the THD+N at lower frequencies, but also impacts PSRR performance (with grounded input and in the lower frequency region).

4.10 Standby control and wake-up time t_{WU}

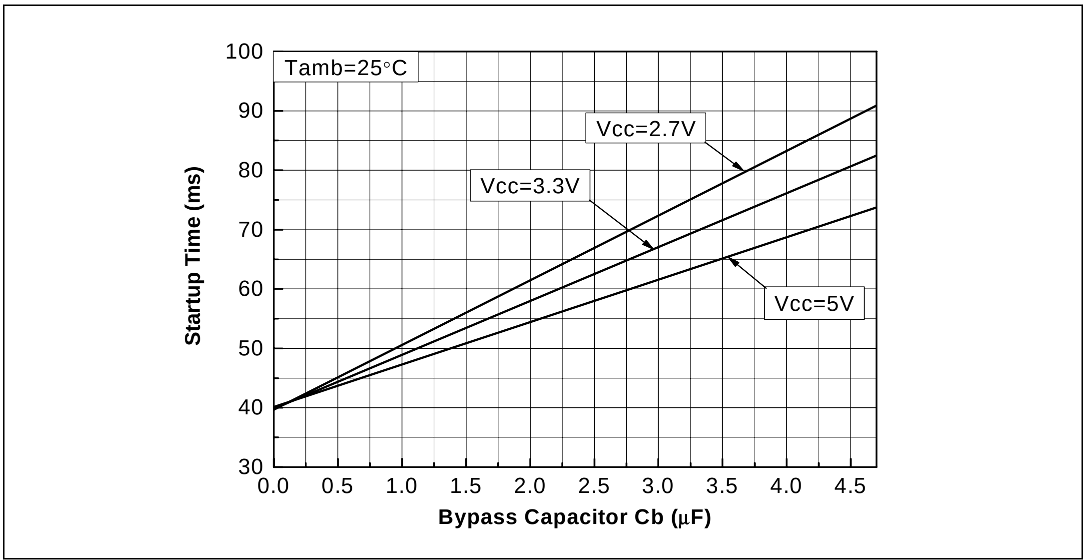
The TS4997 has two dedicated standby pins (STBYL, STBYR). These pins allow to put each channel in standby mode or active mode independently. The amplifier is designed to reach close to zero pop when switching from one mode to the other.

When both channels are in standby ($V_{STBYL} = V_{STBYR}$ = GND), the circuit is in shutdown mode. When at least one of the two standby pins is released to put the device ON, the bypass capacitor C_b starts to be charged. Because C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or t_{WU} and is specified in *Table 4 on page 5*, with C_b=1µF.

During the wake-up phase, the TS4997 gain is close to zero. After the wake-up time, the gain is released and set to its nominal value. If C_b has a value different from 1µF, then refer to the graph in *Figure 66* to establish the corresponding wake-up time.

When a channel is set to standby mode, the outputs of this channel are in high impedance state.

Figure 66. Typical startup time vs. bypass capacitor



4.11 Shutdown time

When the standby command is activated (both channels put into standby mode), the time required to put the two output stages of each channel in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode when both channels are in standby, the Bypass pin and L_{IN}*+,* L_{IN}*-,* R_{IN}*+,* R_{IN}*- pins are shorted to ground by internal switches. This allows a quick discharge of* C_b *and* C_{IN} *capacitors.*

4.12 Pop performance

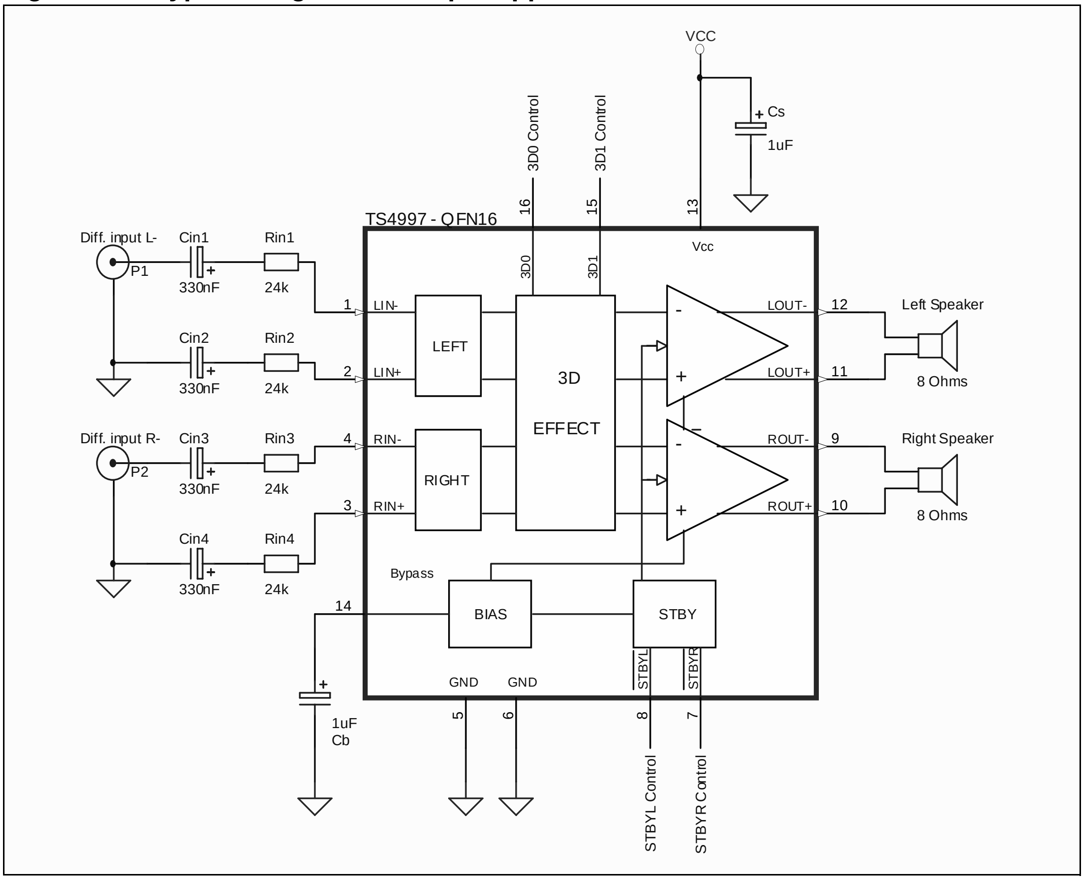
Due to its fully differential structure, the pop performance of the TS4997 is close to perfect. However, due to mismatching between internal resistors R_{feed}, external resistors R_{IN} and external input capacitors C_{IN}, some noise might remain at startup. To eliminate the effect of mismatched components, the TS4997 includes pop reduction circuitry. With this circuitry, the TS4997 is close to zero pop for all possible common applications.

In addition, when the TS4997 is in standby mode, due to the high impedance output stage in this configuration, no pop is heard.

4.13 Single-ended input configuration

It is possible to use the TS4997 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic diagram in *Figure 67* shows an example of this configuration for a gain of +6dB set by the input resistors.

Figure 67. Typical single-ended input application



The component calculations remain the same for the gain. In single-ended input configuration, the formula is:

$$Av_{SE} = \frac{V_{O+} - V_{O-}}{V_e} = \frac{R_{feed}}{R_{IN}} = \frac{50k\Omega}{R_{IN}}$$

with R_{IN} expressed in kΩ

4.14 Notes on PSRR measurement

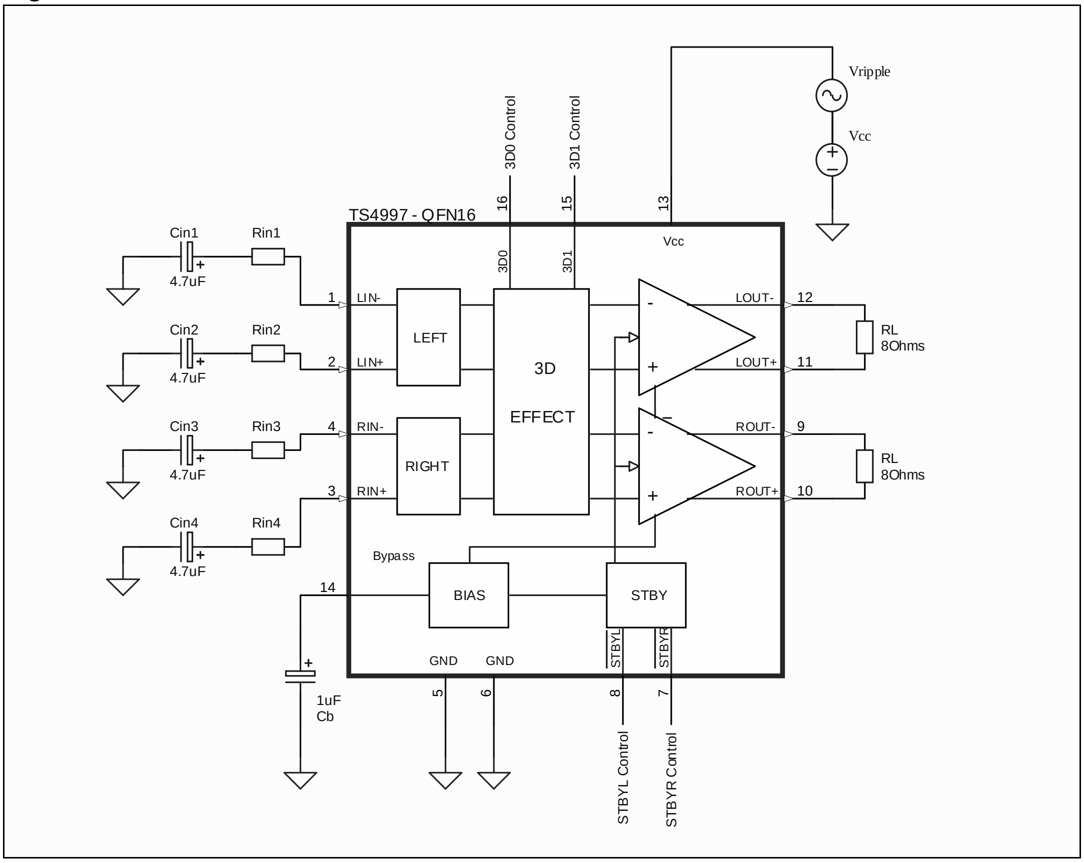
What is the PSRR?

The PSRR is the power supply rejection ratio. The PSRR of a device is the ratio between a power supply disturbance and the result on the output. In other words, the PSRR is the ability of a device to minimize the impact of power supply disturbance to the output.

How is the PSRR measured?

The PSRR is measured as shown in *Figure 68*.

Figure 68. PSRR measurement



Principles of operation

- The DC voltage supply (V_{CC}) is fixed
- The AC sinusoidal ripple voltage (V_{ripple}) is fixed
- No bypass capacitor C_S is used

The PSRR value for each frequency is calculated as:

$$PSRR = 20 \times Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right](dB)$$

RMS is an rms selective measurement.

5 QFN16 package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 69. QFN16 package

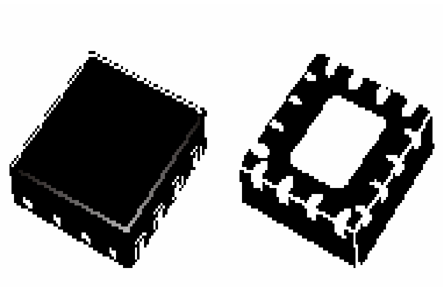


Figure 70. Pinout (top view)

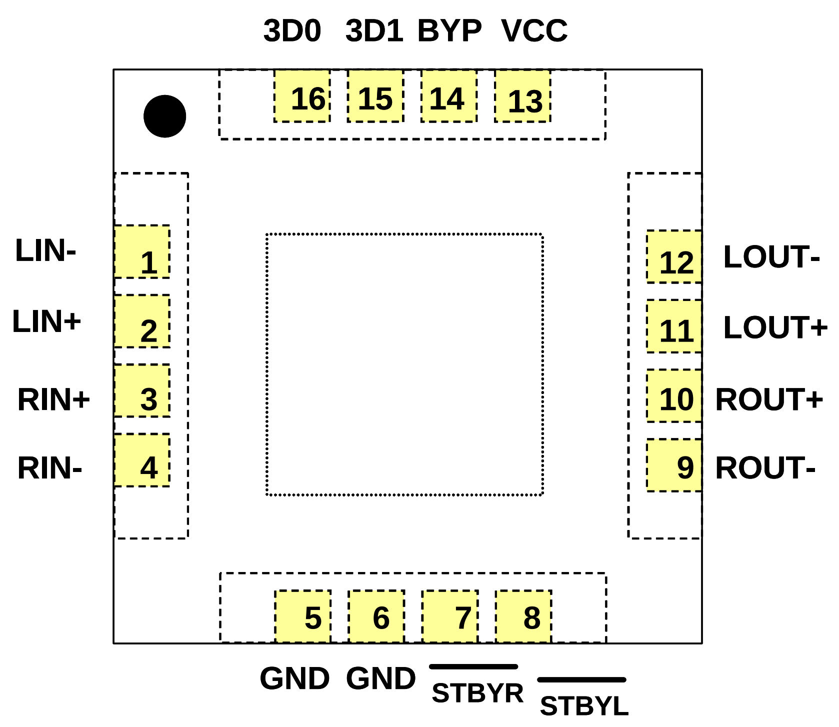
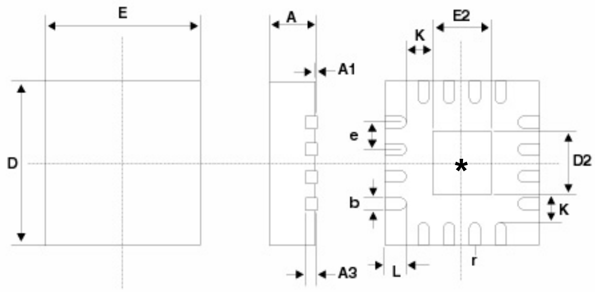


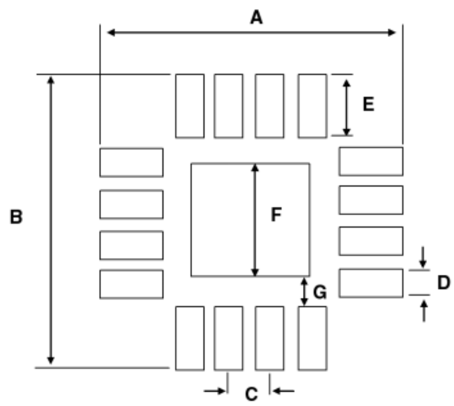
Figure 71. QFN16 4x4mm



* The Exposed Pad is connected to Ground.

Dimensions			
Ref	Millimeters (mm)		
	Min	Typ	Max
A	0.8	0.9	1.0
A1		0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.0	4.15
D2	2.1		2.6
E	3.85	4.0	4.15
E2	2.1		2.6
e		0.65	
K	0.2		
L	0.30	0.40	0.50
r	0.11		

Figure 72. Footprint soldering pad



Footprint data	
Ref	mm
A	4.2
B	4.2
C	0.65
D	0.35
E	0.65
F	2.70

6 Ordering information

Table 10. Order codes

Part number	Temperature range	Package	Packaging	Marking
TS4997IQT	-40°C, +85°C	QFN16 4x4mm	Tape & reel	Q997

7 Revision history

Date	Revision	Changes
10-Jan-2007	1	Preliminary data.
20-Feb-2007	2	First release.