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SP5054

2.6GHz 3-Wire BUS Controlled Synthesiser

DS3048 ISSUE 3.4 May 1996

The SP5054 is a single-chip frequency synthesiser designed for satellite TV tuning systems. It is a programming variant of the SP5055, allowing the design of one tuner with either I^2C bus or 3-wire bus format, depending on which device is inserted. The SP5054, when used with a satellite varactor tuner, forms a complete phase locked loop tuning system.

The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14/15-bit programmable divider controlled by a serially-loaded data register. Four independently programmable open-collector outputs are included. The device has four modes of operation, selected by the Mode Select input; these modes are summarised in Table1.

The comparison frequencies are obtained by the division of the output of a 4MHz crystal controlled on-chip oscillator. The phase comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varactor line driving.

Features

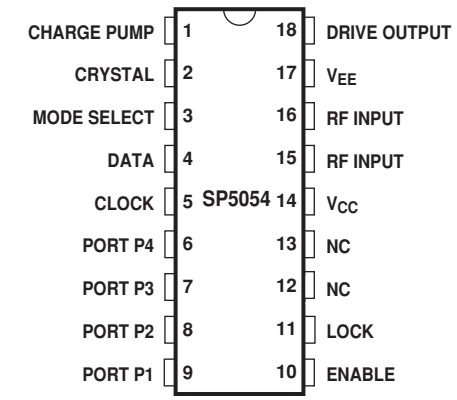
- Complete 2·6GHz Single Chip System
- 62·5kHz, 100kHz and 125kHz Step Size
- Low Power Consumption (325mW Typ.)
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382 *
- Pin Compatible with SP5055 *
- Low Radiation
- Varactor Drive Amplifier Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility
† Normal ESD handling precautions should be observed

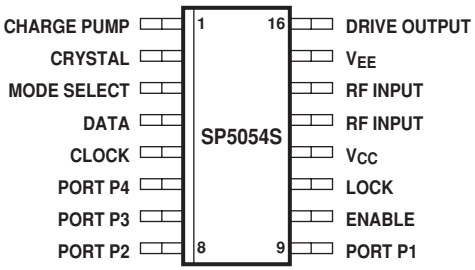
Applications

- Satellite TV
- High IF Cable Tuning Systems

Ordering Information
SP5054 KG DPAS (18-lead plastic package)
SP5054S KG MPAS (16-lead miniature plastic package)



DP18



MP16

Figure 1 - Pin connections – top view

Electrical Characteristics

T_{AMB} = 220°C to 180°C, V_{CC} = 14·5V to 15·5V. Frequency standard = 4MHz. All pin connections refer to DP package. These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler input voltage	15,16	50		400	mVrms	500MHz to 2·6GHz sinewave
Prescaler input voltage		100		400	mVrms	120MHz and 500MHz, see Fig. 6
Prescaler input impedance	15,16		50		Ω	
Input capacitance			2		pF	
High level input voltage	4,5,10	3		V_{CC}	V	
Low level input voltage	4,5,10	0		0·7	V	
High level input current	4,5,10			1	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	5			5	µA	V_{IN} = 0V, V_{CC} = 5·5V
Low level input current	4,10			−250	µA	V_{IN} = 0V, V_{CC} = 5·5V
High level input current	3			700	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	3			−700	µA	V_{IN} = 0V, V_{CC} = 5·5V
Clock inout hysteresis	5		0·4		V	
Clock rate	5			0·5	MHz	
Data set up time, t_2	4	300			ns	See Fig. 4
Data hold time, t_3	4	600			ns	See Fig. 4
Enable set up time, t_1	10	300			ns	See Fig. 4
Enable hold time, t_5	10	600			ns	See Fig. 4
Clock-to-enable time, t_4	10	300			ns	See Fig. 4
Charge pump output current	1		±150		µA	V pin 1 = 2·0V
Charge pump output leakage current	1			±5	nA	V pin 1 = 2·0V
Drift due to leakage				5	mV/s	At collector of external transistor
Charge pump drive output current	18	1			mA	V pin 18 = 0·7V
Charge pump amplifier gain			6400			I pin 18 = 100µA
Oscillator temperature stability				2	ppm/°C	
Oscillator stability with supply voltage				2	ppm/V	
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 1)
Crystal oscillator drive level	2		40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Ports and Lock Output						
Sink current	6-9,11	10			mA	V_{OUT} = 0·7V
Port leakage current	6-9			10	µA	V_{OUT} = 13·2V
Varactor drive amplifier disable	10	−350			µA	V_{IN} < 0V
Charge pump disable	4	−350			µA	V_{IN} < 0V

NOTE 1. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin		Value		Units	Conditions
	SP5054	SP5054S	Min.	Max.		
Supply voltage	14	12	−0·3	7	V	
RF input voltage	15,16	13,14		2·5	V p-p	
Port voltage	6-9	6-9	−0·3	14	V	Port in off state
	6-9	6-9	−0·3	6	V	Port in on state
Prescaler DC offset	15,16	13-14	−0·3	V_{CC}+0·3	V	
Loop amplifier DC offset	1,18	1,16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
Data bus inputs	4,5,10	4,5,10	−0·3	V_{CC}+0·3	V	With V_{CC} applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5·5V				484	mW	

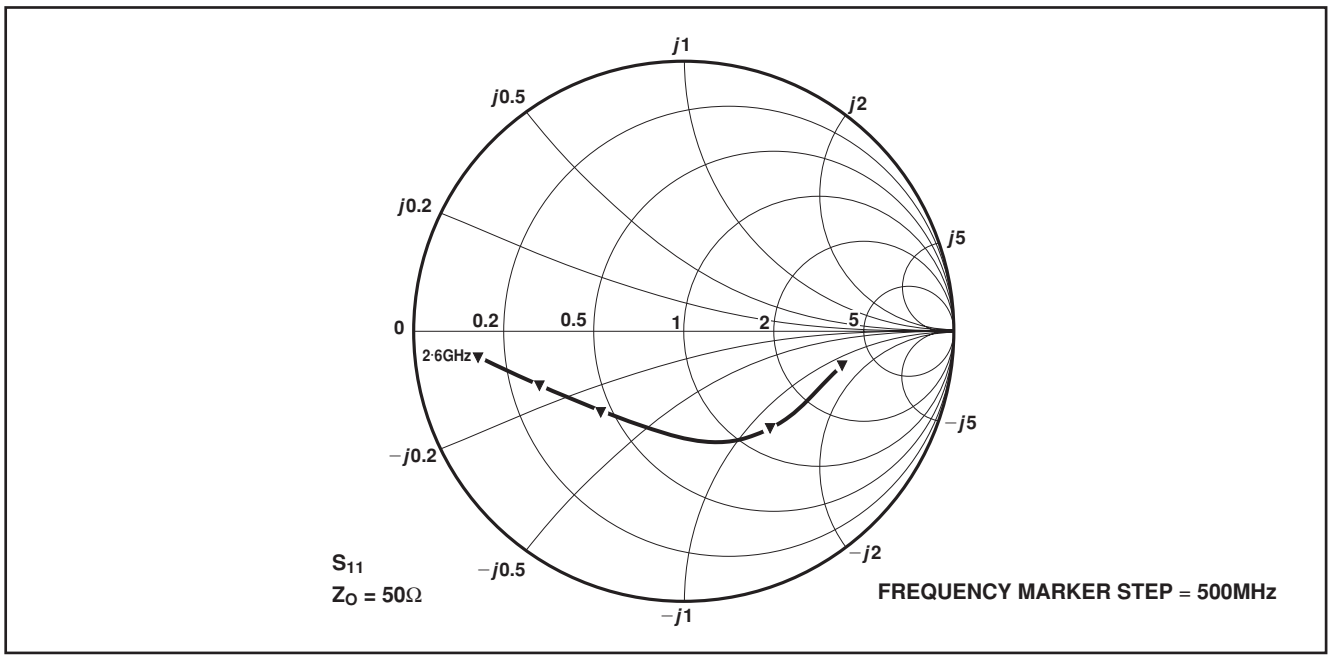


Figure 2 - Typical input impedance

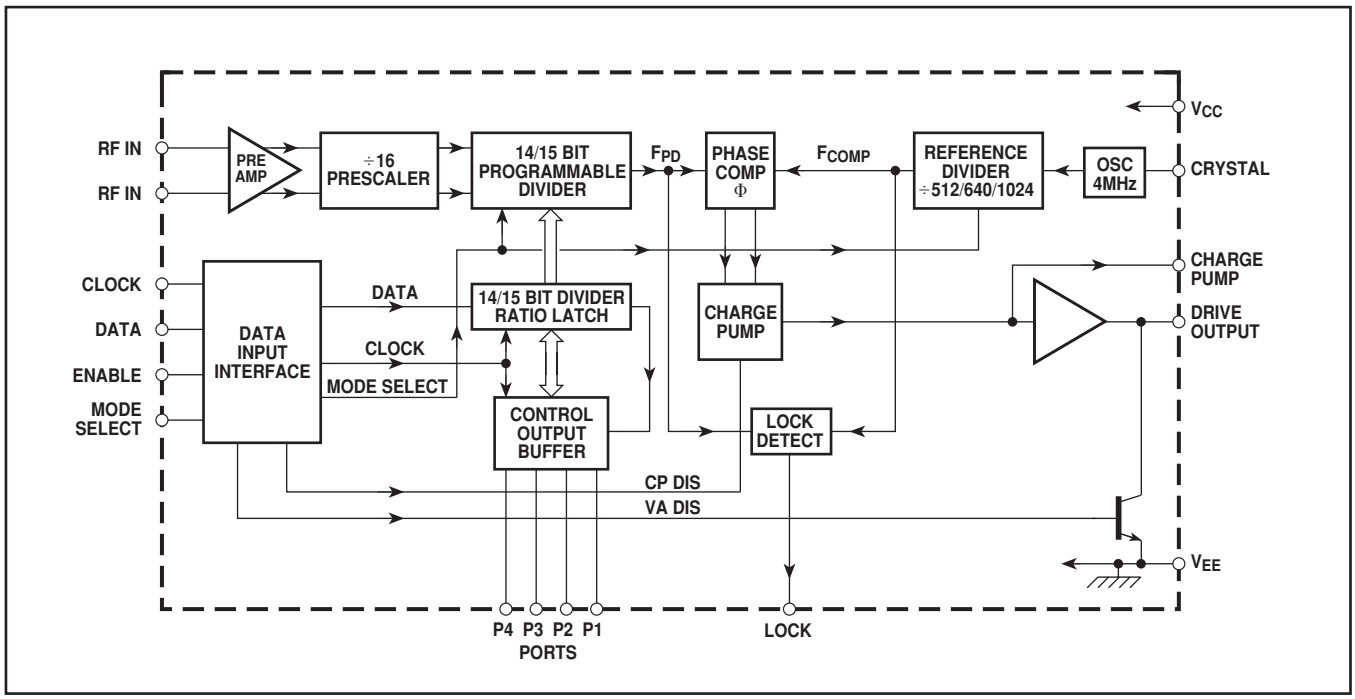


Figure 3 - Block diagram of SP5054

Mode	Mode Select input voltage	Programmable divider bit length	Reference divider ratio	Frequency step size (kHz) *	Maximum operating frequency (GHz)*
3	$0{\cdot}925V_{CC}$ to V_{CC}	14	512	125	2·0479
2	$0{\cdot}675V_{CC}$ to $0{\cdot}825V_{CC}$	15	512	125	2·5
1	Open circuit	15	1024	62·5	2·0479
0	0V to $0{\cdot}325\ V_{CC}$	15	640	100	2·5

Table 1 - SP5054 modes of operation. * Frequencies stated apply when using a 4MHz crystal.

Functional Description

The SP5054 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard Data, Clock and Enable three-wire data bus.

The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period.

The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the Enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format shown in Fig. 4.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3·90625/6·25/7·8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 62·5/100/125kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity.

The SP5054 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'In lock' is indicated by high impedance state.

The SP5054 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the normal data word.

Notes on pin compatibility

The SP5054 may be used in SP5055 applications which require 3-wire bus as opposed to I^2C bus data format. In SP5055 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be made to the Mode Select input (see Table 1). In Mode 3, The SP5054 is programming compatible with the Toshiba TD6380, in Modes 0 and 2 with the TD6381 and in Mode 1 with the TD6382.

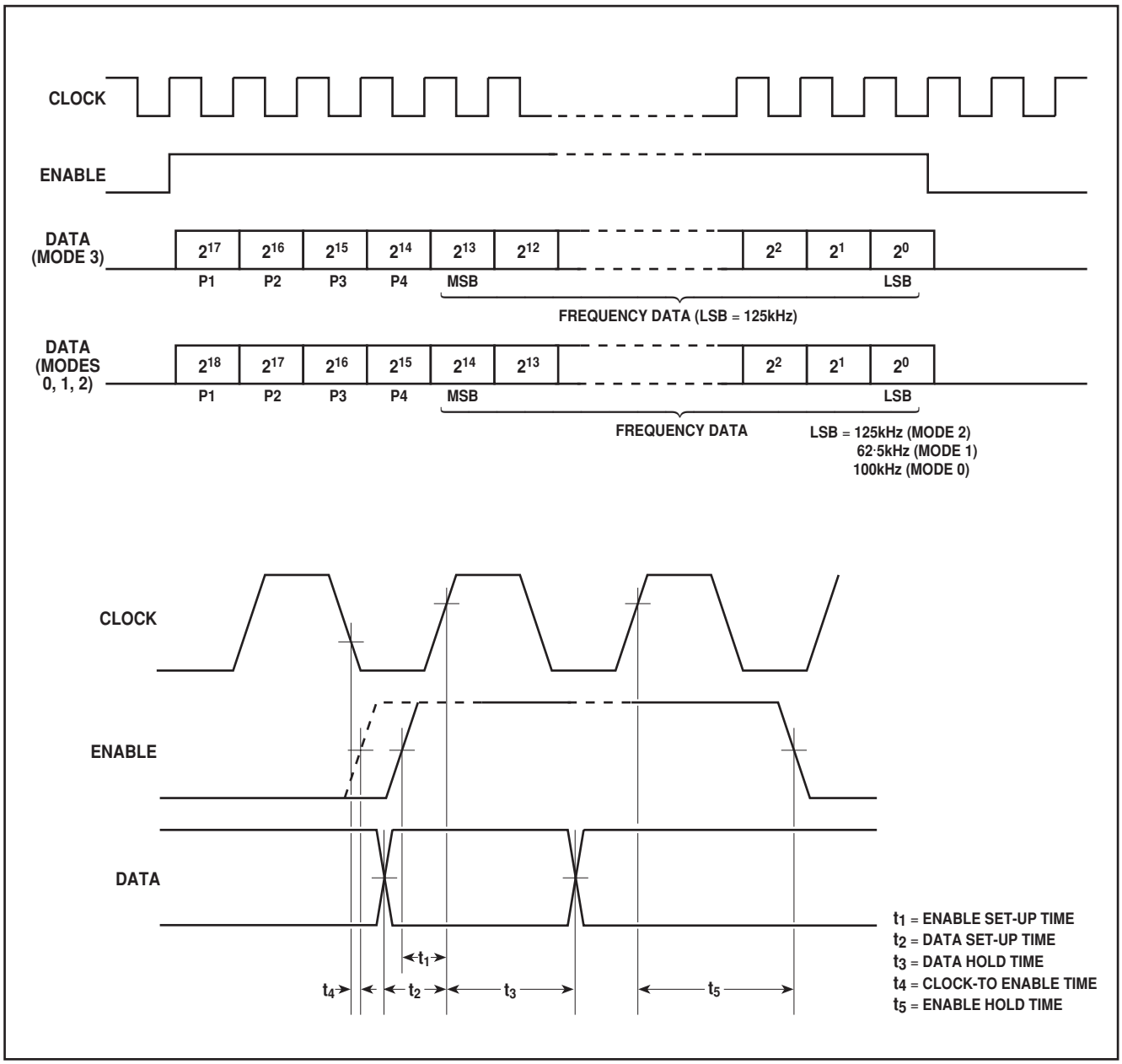


Figure 4 - Data format and timing

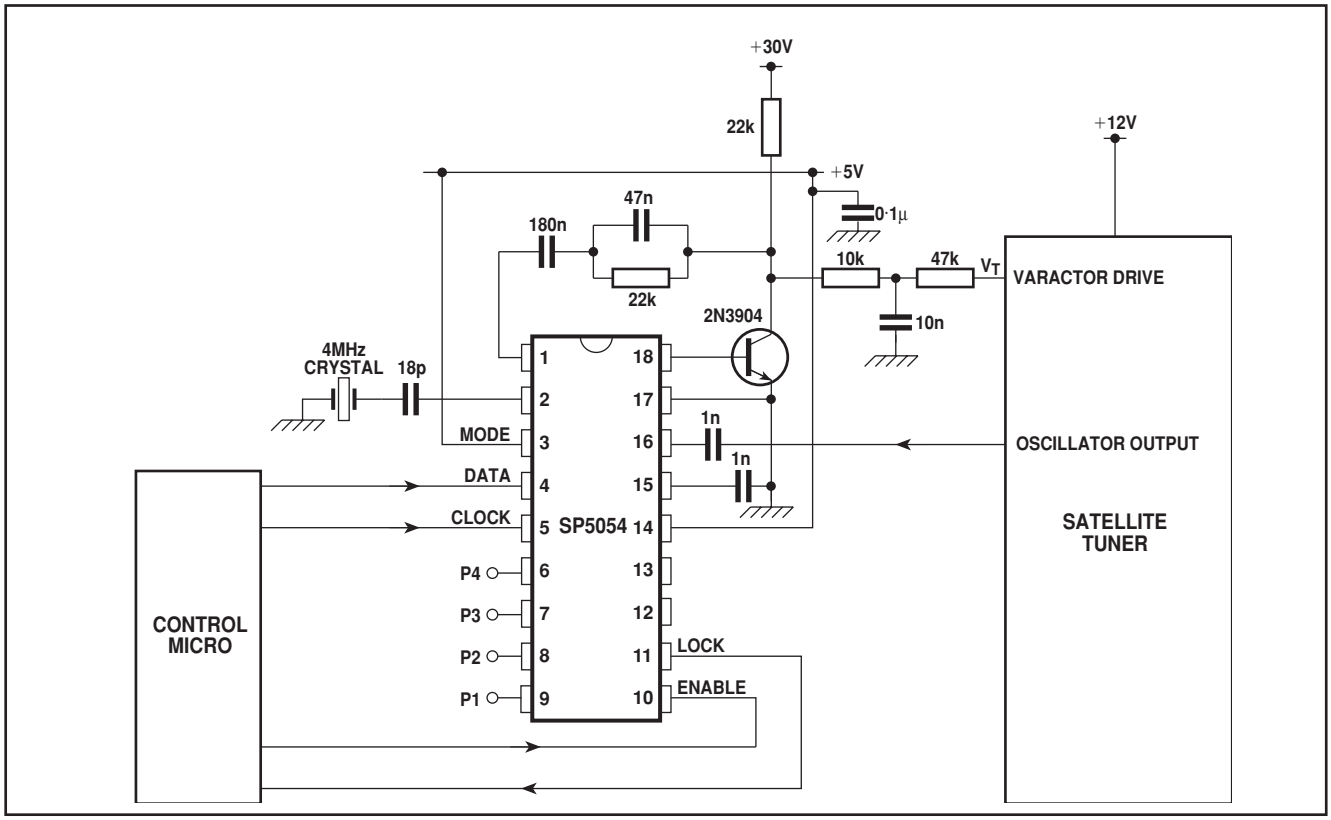


Figure 5 - Typical application (f_{STEP} = 125kHz)

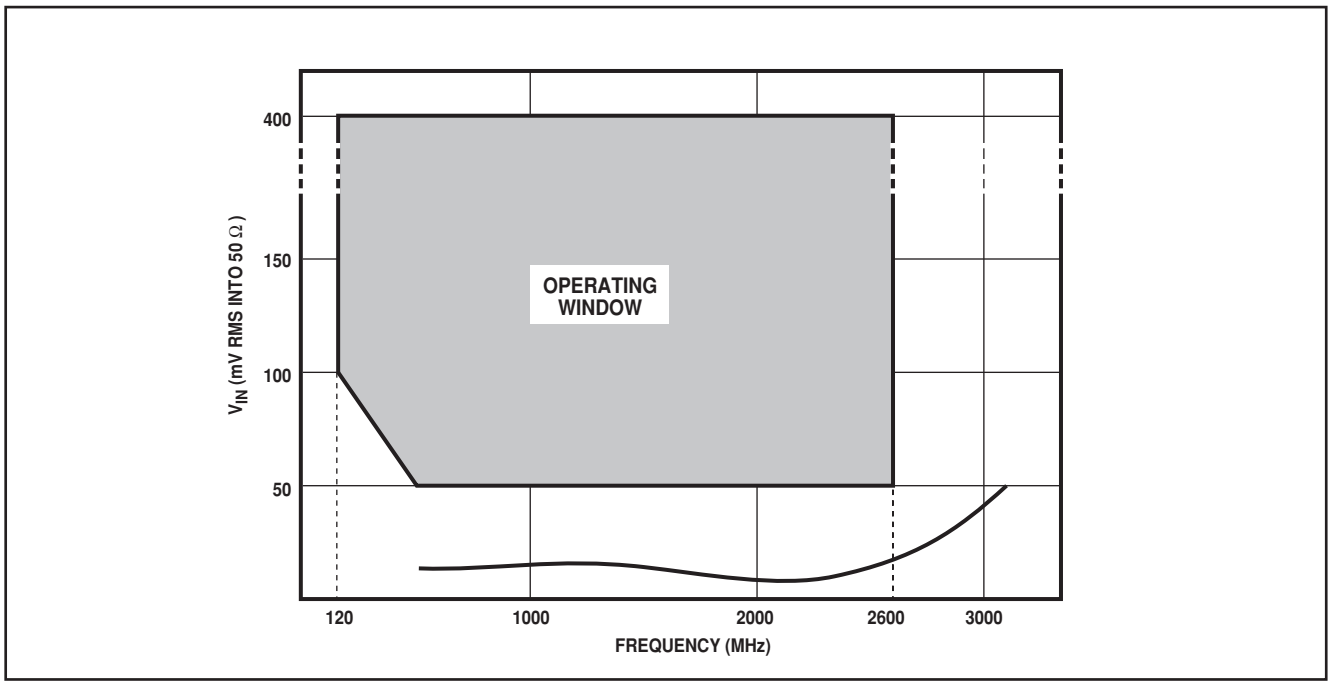


Figure 6 - Typical input sensitivity

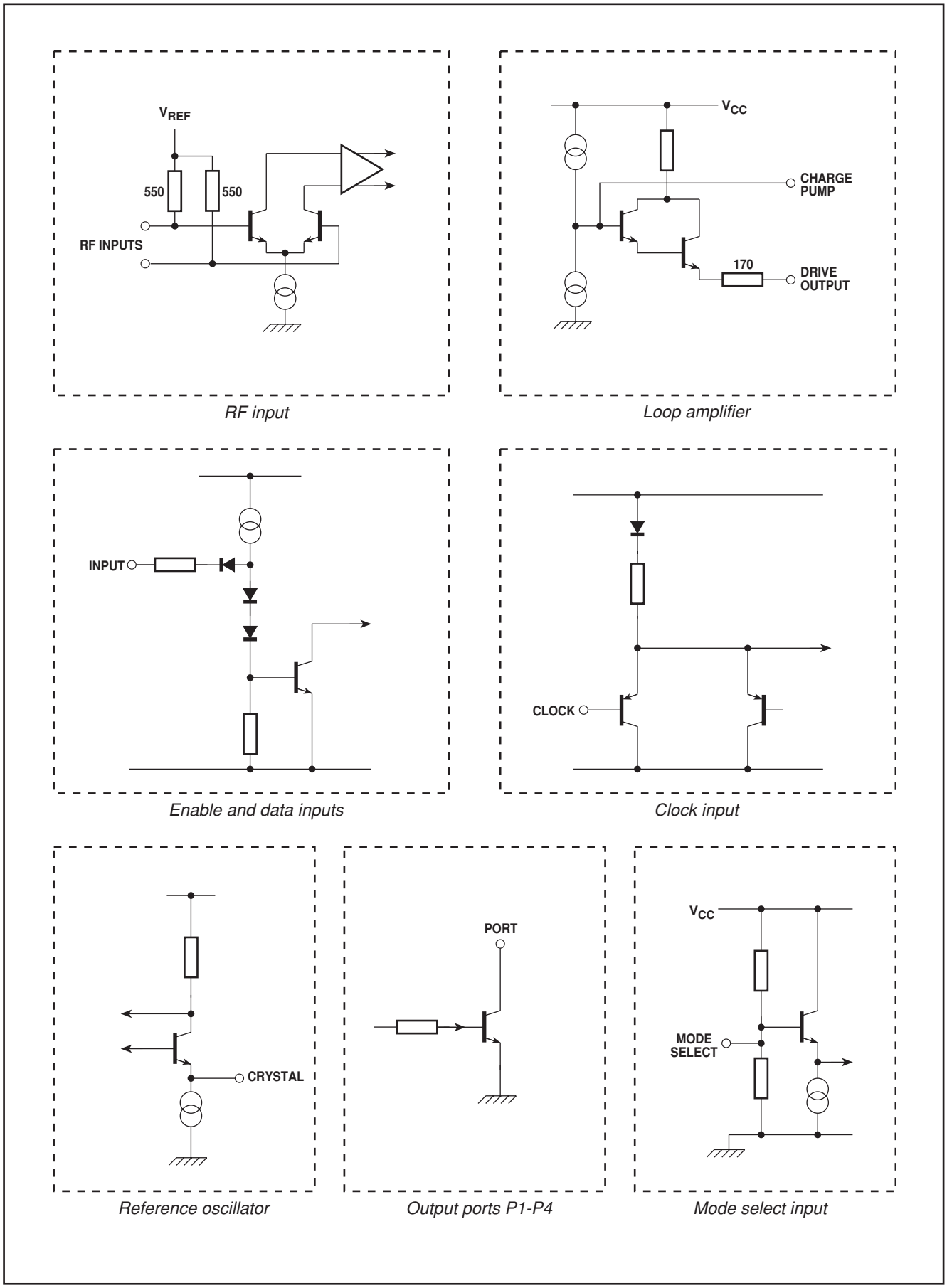
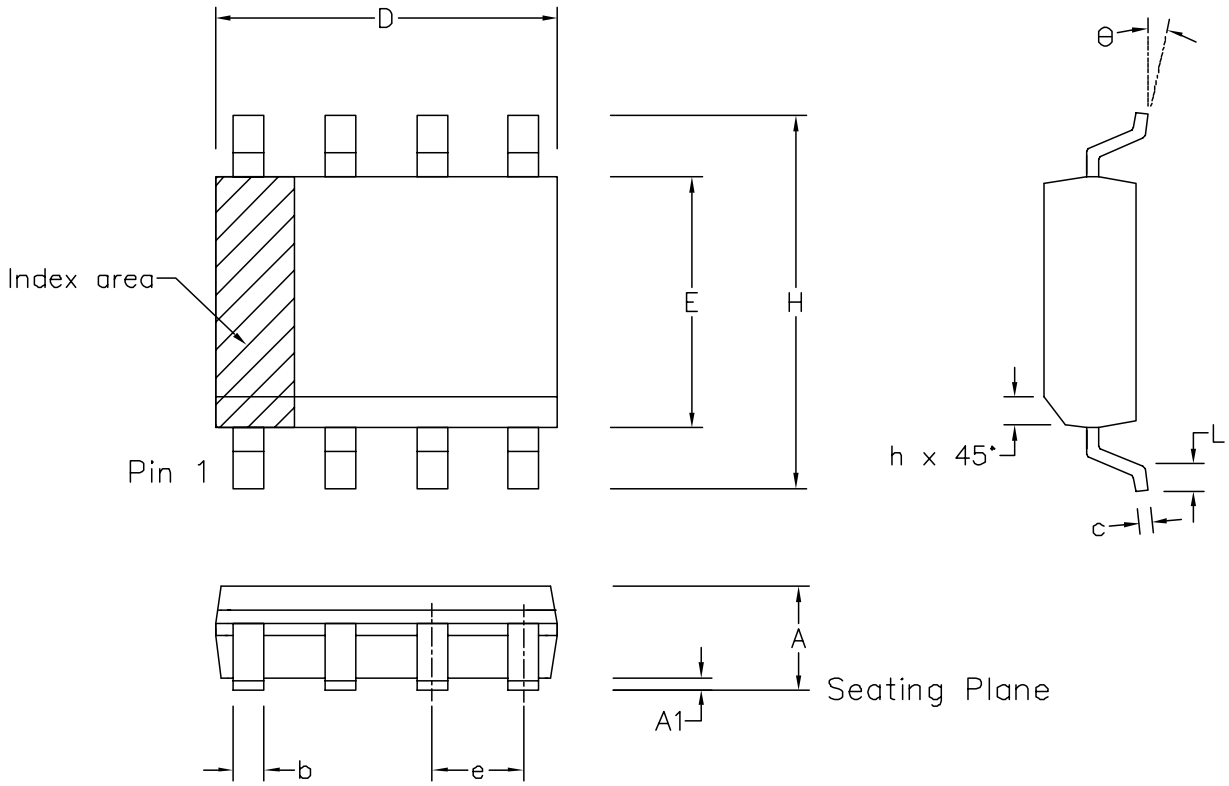


Figure 7 - SP5054 input/output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
Θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	
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DATE	7APR95	27FEB97	12JUN97	9DEC97	
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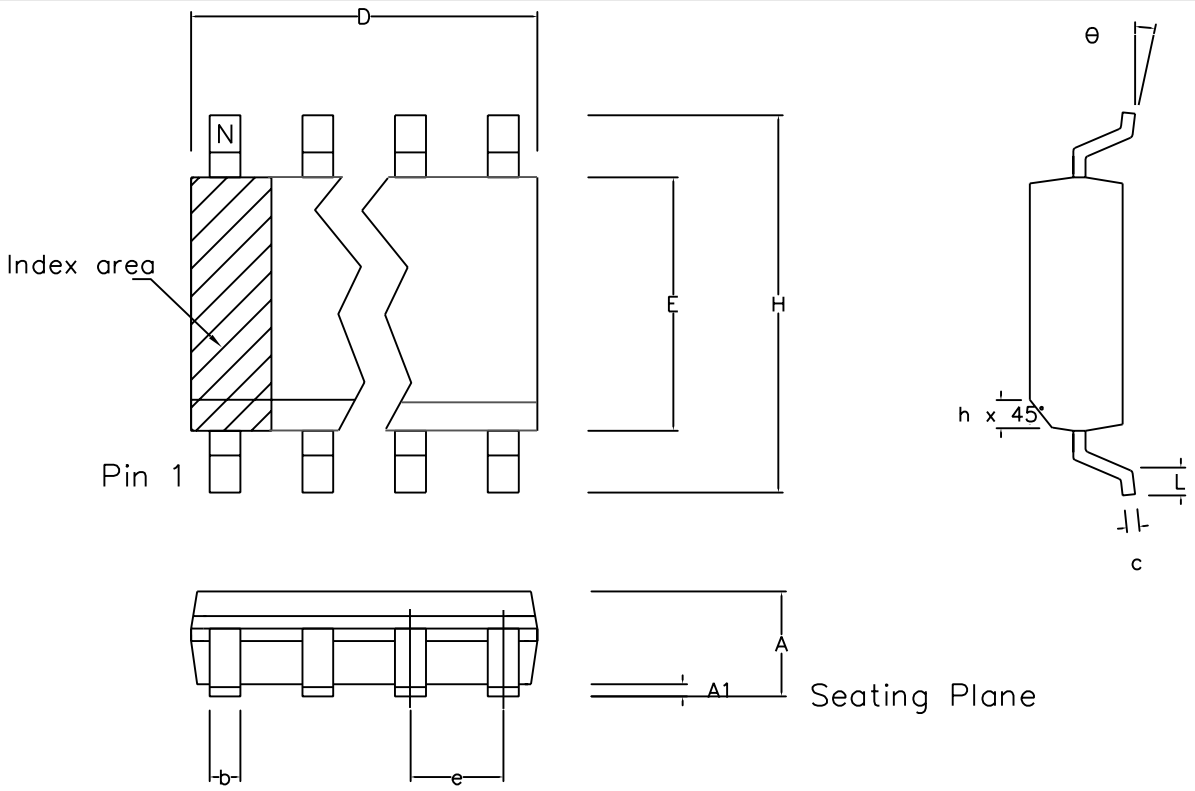
ORIGINATING SITE: SWINDON

Title: Package Outline Drawing for 16 lds SOIC(N)-0.150" Body Width (MP)

Drawing Number
GPD00012



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	Pin Features			
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Conforms to JEDEC MS-012AC Iss. C				

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ZARLINK SEMICONDUCTOR

Previous package codes
MP / S

Package Code DC

Package Outline for
16 lead SOIC
(0.150" Body Width)

GPD00012

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