CMOS IC

LC85050

Cordless Answering Machine System IC

Preliminary

Overview

The LC85050 is a cordless answering machine system IC that integrates an extensive set of functions on a single chip. These functions include a DSP that provides audio recording and playback functions, voice recognition functions, text-to-speech synthesis, and line and audio echo cancellation, a $\Delta\Sigma$ A/D converter, a $\Delta\Sigma$ D/A converter, a flash memory interface, and a host CPU interface.

The LC85050 uses the PULCOD™ (pulse code excited linear prediction) high-compression ratio compression algorithm to allow up to 19 minutes of audio recording on 4M of external flash memory. Furthermore, the optional LD-ADPCM (low-distortion ADPCM) waveform encoding algorithm allows the recording and playback of high-quality audio signals.

The LC85050's line and audio echo cancellation function allows it to implement a speakerphone function for answering machine/telephone products. It also includes ITU-T V.23 and Bell 202 conforming data transmission and reception functions to support caller ID.

The LC85050's text-to-speech synthesis function allows end products to announce the name of the calling party. Its speaker-independent voice recognition function can be used to allow users to easily enter telephone numbers in its phone book. The LC85050's speaker-dependent voice recognition function allows users to pre-register the names of people to call with the user's own voice. Then the user can then either recall any of those parties' phone number, or even call the person, simply by speaking the name. Furthermore, the LC85050 can easily implement all of the functions required by standard telephone or answering machine products, including DTMF and other tone generation and detection as well as music synthesis.
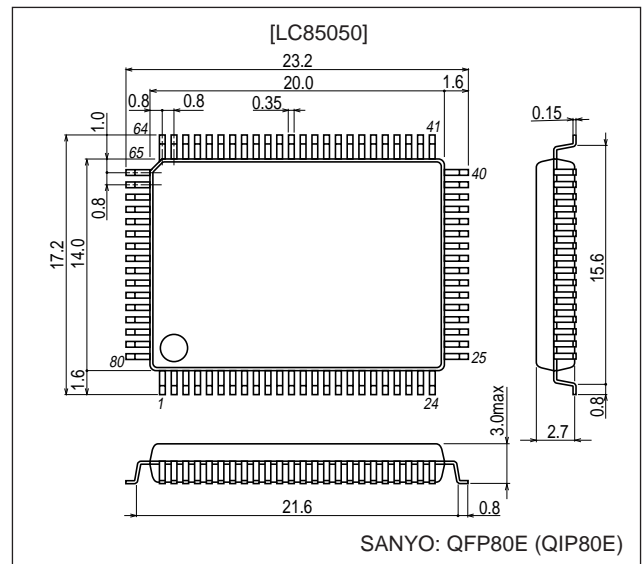
Features

• PULCOD™ (high compression ratio encoding)
   —High compression ratio: 3.6 kbps
   —Automatic input gain adjustment function
   —Voice trigger function
   —Silence removal function
   —Tail cut function
   —Variable-speed playback function

Package Dimensions

unit: mm
3174-QIP80E

SANYO: QFP80E (QIP80E)

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- LD-ADPCM function (waveform encoding) (optional function)
  —Compression ratio: 14.4, 21.6, and 28.8 kbps
  —Automatic input gain adjustment function
  —Voice trigger function
  —Tail cut function
- Text-to-speech synthesis function
  —Accent adjustment
  —Katakana input
- Voice recognition function
  —Speaker-independent recognition (15 words)
  —Speaker-dependent recognition (50 words)
- Flash memory management function (8M address space)
  —Flash memory: 4 M (×1 or ×8)
- Full-duplex hands-free function
  —Line echo canceler
  —Audio echo canceler for speakerphone operation
  —Telephone conversation recording using LD-ADPCM (option)
  —DTMF detection
  —Caller ID detection
- Modem functions
  —Bell 202 (1200 bps) send/receive
  —ITU-T V.23 (1200 bps) send/receive
  —Synchronous/asynchronous communication functions
    Start/stop synchronization, HDLC, DDI, and NTT support

- —Programmable reception sensitivity
    (–10 dBm to –47 dBm)
- Programmable tone generation and detection
  —Individually adjustable reception sensitivity
    (–10 dBm to –47 dBm)
- DTMF generation and detection
- Call progress tone detection
  —Adjustable reception sensitivity
    (–10 dBm to –47 dBm)
- Melody function (option)
- Programmable transmission level (0 dBm to –15 dBm)
- Reception dynamic range: 0 to –47 dBm
- Self-diagnostic function
- Monitor output function
- Host CPU interface
  —3-wire serial interface (clock synchronous)
  —8-bit parallel interface
- Output ports (up to 12 ports):
  3 output ports are always available.
- Low-power CMOS
- Supply voltage
  —Single 3.3 V supply, or dual 3.3 and 5.0 V supply voltages
- Package: QIP-80E

Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter		Symbol	Conditions	Ratings	Unit
Maximum supply voltage		$V_{DD}3$		–0.3 to +4.2	V
		$V_{DD}5$		–0.3 to +6.0	V
I/O voltages		V_I3, V_O3		–0.3 to $V_{DD}3$ + 0.3	V
		V_I5, V_O5		–0.3 to $V_{DD}5$ + 0.3	V
Allowable power dissipation		Pdmax	Ta ≤ 25°C	500	mW
Operating temperature		Topr		–30 to +70	°C
Storage temperature		Tstg		–55 to +125	°C
Soldering conditions	Hand soldering		3 seconds	350	°C
	Reflow soldering		10 seconds	235	°C

Allowable Operating Ranges at Ta = –30 to +70°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}3$		3.0	3.3	3.6	V
	$V_{DD}5$		3.0	5.0	5.5	V
Input voltage range	$V_{IN}3$		0		$V_{DD}3$	V
	$V_{IN}5$		0		$V_{DD}5$	V

Applicable pins

V_I3, V_O3, $V_{IN}3$: PLLI, PLLO, RIN, AUXO, AUXI, SPOUT, MIC, VREF, TXA, RXA
V_I5, V_O5, $V_{IN}5$: All pins other than the above.

DC Characteristics (1) at Ta = –30 to +70°C, GND = 0 V, $V_{DD}5$ = 4.5 to 5.5 V, $V_{DD}3$ = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	$V_{IH}1$	CMOS (1), (4)	0.7 $V_{DD}5$			V
	$V_{IH}2$	CMOS Schmitt inputs (2)	0.8 $V_{DD}5$			V
Input low-level voltage	$V_{IL}1$	CMOS (1), (4)			0.3 $V_{DD}5$	V
	$V_{IL}2$	CMOS Schmitt inputs (2)			0.2 $V_{DD}5$	V
Output high-level voltage	V_{OH}	I_{OH} = –4 mA (3), (4)	$V_{DD}5$ – 2.1			V
Output low-level voltage	V_{OL}	I_{OL} = 4 mA (3), (4)			0.4	V
Input leakage current	I_{IL}	V_I = GND, $V_{DD}5$	–10		+10	µA
Output leakage current	I_{OZ}	In the high-impedance output state	–10		+10	µA
Oscillator frequency	f_{CLK}			3.6864		MHz
Current drain	$I_{DD}1$	Operating		110	150	mA
	$I_{DD}1$	In power down mode		5		µA

DC Characteristics (2) at Ta = –30 to +70°C, GND = 0 V, $V_{DD}5$ = 3.0 to 3.6 V, $V_{DD}3$ = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	$V_{IH}1$	CMOS (1), (4)	0.7 $V_{DD}5$			V
	$V_{IH}2$	CMOS Schmitt inputs (2)	0.75 $V_{DD}5$			V
Input low-level voltage	$V_{IL}1$	CMOS (1), (4)			0.2 $V_{DD}5$	V
	$V_{IL}2$	CMOS Schmitt inputs (2)			0.15 $V_{DD}5$	V
Output high-level voltage	V_{OH}	I_{OH} = –2 mA (3), (4)	$V_{DD}5$ – 0.8			V
Output low-level voltage	V_{OL}	I_{OL} = 2 mA (3), (4)			0.4	V
Input leakage current	I_{IL}	V_I = GND, $V_{DD}5$	–10		+10	µA
Output leakage current	I_{OZ}	In the high-impedance output state	–10		+10	µA
Oscillator frequency	f_{CLK}			3.6864		MHz
Current drain	$I_{DD}1$	Operating		100	140	mA
	$I_{DD}1$	In power down mode		5		µA

The applicable pins are as follows.

(1) TESTER, TESTEN, TESTD, PS, XIN, RB1, RB0

(2) $\overline{RESET}$, $\overline{CPUCS}$, $\overline{CPUOE}$, $\overline{CPUWE}$

(3) BUSY, $\overline{IREQ}$, PLOCK, PA0 to PA2, $\overline{MCS0}$, $\overline{MCS1}$, $\overline{MWE}$, $\overline{MRE}$, CLE, ALE, $\overline{WP0}$, $\overline{WP1}$, EYECLK, EYESYNC, EYED, XOUT

(4) CD0 to CD7, MD0 to MD7

Note: The PLLI, PLLO, RIN, AUXO, AUXI, SPOUT, MIC, VREF, RXA, and TXA pins are not included in the DC characteristics ratings.

System Block Diagram

The diagram below shows a circuit that uses serial mode for the host CPU interface.
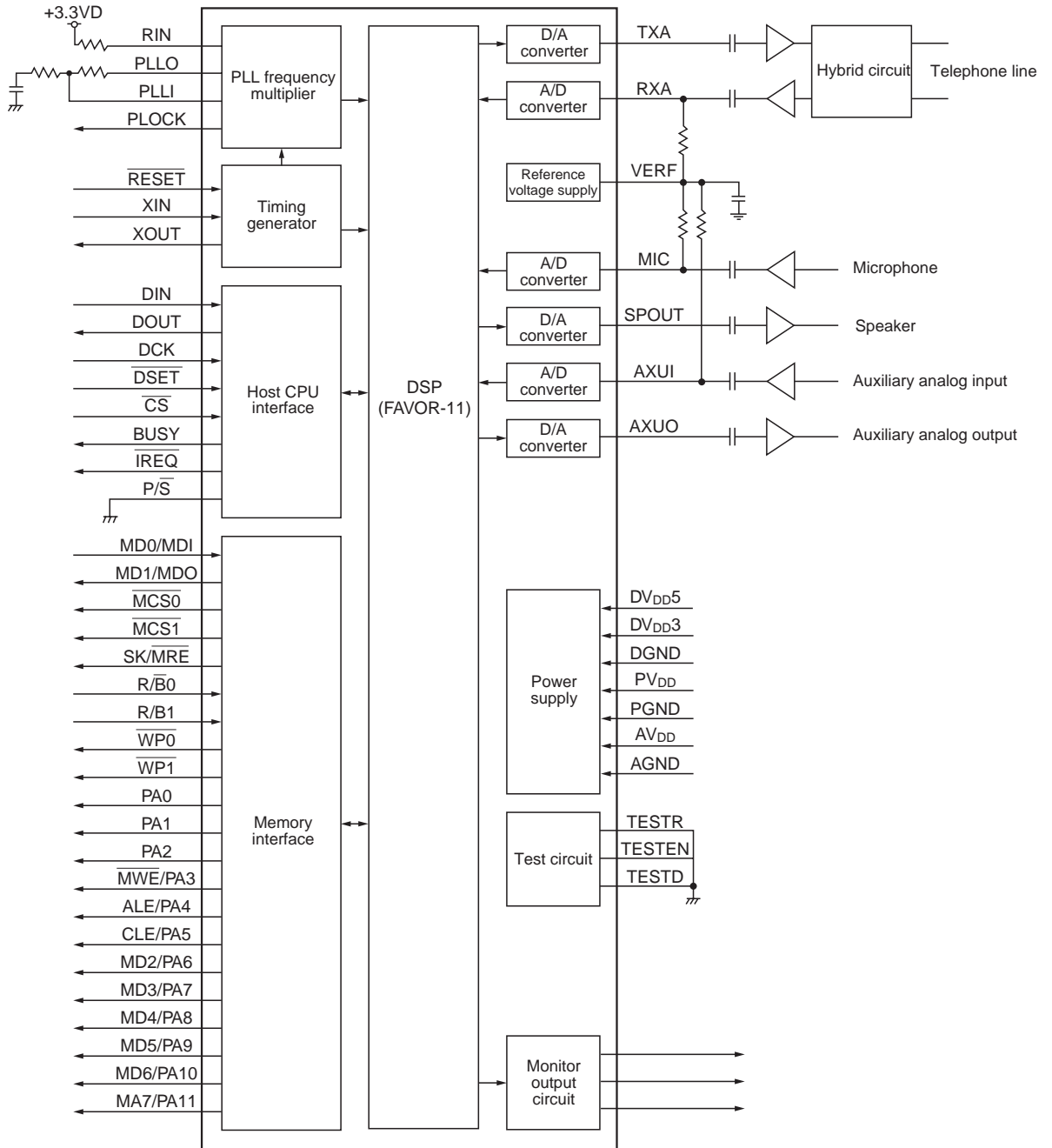
LC85050

Pin Functions

Type					
I	Input	B	Bidirectional	NC	Not connected
O	Output	P	Power supply		

Pin No.	Pin	I/O	Function
1	PV$_{DD}$	P	PLL frequency multiplier 3.3 V power supply
2	PGND	P	PLL frequency multiplier ground
3	RIN	I	PLL frequency multiplier bias input
4	PLLI	I	PLL frequency multiplier VCO input
5	PLLO	O	PLL frequency multiplier charge pump output
6	PLOCK	O	PLL frequency multiplier operating status output
7	TESTR	I	
8	TESTEN	I	Test inputs. These input must be connected to DGND during normal operation.
9	TESTD	I	
10	$\overline{\text{RESET}}$	I	Reset input
11	XIN	I	Oscillator amplifier input (3.6864 MHz)
12	XOUT	O	Oscillator amplifier output
13	DGND	P	Digital system ground
14	DV$_{DD}$3	P	Digital system 3.3 V power supply
15	P/$\overline{\text{S}}$	I	Host CPU interface selection signal
16	$\overline{\text{CPUCS}}$	I	Host CPU chip select signal
17	$\overline{\text{CPUOE}}$/DCK	I	In parallel mode: host CPU read signal In serial mode: data clock input signal
18	$\overline{\text{CPUWE}}$/$\overline{\text{DSET}}$	I	In parallel mode: host CPU write signal In serial mode: data transfer complete input
19	CD0/DIN	B	
20	CD1/DOUT	B	In parallel mode: host CPU data bus lines In serial mode: CD0 functions as host CPU serial data signal,
21	CD2	B	and CD1 functions as the host CPU serial data output.
22	CD3	B	
23	DGND	P	Digital system ground
24	DV$_{DD}$5	P	Digital system 5.0 V power supply
25	CD4	B	
26	CD5	B	In parallel mode: host CPU data bus lines
27	CD6	B	
28	CD7	B	
29	BUSY	O	Status output that indicates the host CPU interface status
30	$\overline{\text{IREQ}}$	O	Interrupt request output
31	DV$_{DD}$3	P	Digital system 3.3 V power supply
32	DGND	P	Digital system ground
33	NC		
34	NC		
35	NC		
36	PA0	O	
37	PA1	O	Output ports
38	PA2	O	
39	DV$_{DD}$5	P	Digital system 5.0 V power supply
40	DGND	P	Digital system ground
41	AV$_{DD}$	P	Analog system 3.3 V power supply
42	AGND	P	Analog system ground
43	AUXI	I	Auxiliary analog input
44	MIC	I	Analog audio input
45	RXA	I	Analog circuit input
46	VREF	O	Analog reference output
47	AUXO	O	Auxiliary analog output
48	SPOUT	O	Analog audio output
49	TXA	O	Analog circuit output
50	AGND	P	Analog system ground

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Pin No.	Pin	I/O	Function
51	AV$_{DD}$	P	Analog system 3.3 V power supply
52	DGND	P	Digital system ground
53	DV$_{DD}$3	P	Digital system 3.3 V power supply
54	EYED	O	Monitor data output
55	EYESYNC	O	Monitor sync signal output
56	SYSCLK	O	Monitor clock output
57	$\overline{\text{WP1}}$	O	Audio memory write protect output
58	R/$\overline{\text{B}}$1	I	Status input that monitors audio memory
59	MD0/MDI	B	Parallel type: audio memory data bus line Serial type: audio data input
60	MD1/MDO	B	Parallel type: audio memory data bus line Serial type: audio data output
61	MD2/PA6	B	Parallel type: audio memory data bus lines
62	MD3/PA7	B	Serial type: output ports
63	DV$_{DD}$5	P	Digital system 5.0 V power supply
64	DGND	P	Digital system ground
65	MD4/PA8	B	
66	MD5/PA9	B	Parallel type: audio memory data bus lines
67	MD6/PA10	B	Serial type: output ports
68	MD7/PA11	B	
69	$\overline{\text{WP0}}$	O	Audio memory write protect output
70	R/$\overline{\text{B}}$0	I	Status input that monitors audio memory
71	ALE/PA4	O	Parallel type: audio memory address latch enable signal Serial type: output ports
72	DGND	P	Digital system ground
73	DV$_{DD}$5	P	Digital system 5.0 V power supply
74	CLE/PA5	O	Parallel type: audio memory command latch enable signal Serial type: output ports
75	$\overline{\text{MWE}}$/PA3	O	Parallel type: audio memory write signal Serial type: output ports
76	SK/$\overline{\text{MRE}}$	O	Parallel type: audio memory read signal Serial type: audio data transfer clock
77	$\overline{\text{MCS1}}$	O	Audio memory type selection (1) signal
78	$\overline{\text{MCS0}}$	O	Audio memory type selection (0) signal
79	DV$_{DD}$3	P	Digital system 3.3 V power supply
80	DGND	P	Digital system ground