



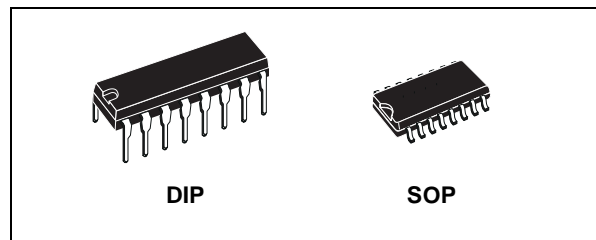
HCF4521B

24-STAGE FREQUENCY DIVIDER

- HIGH NOISE IMMUNITY
- VOLTAGE SUPPLY RANGE 3V TO 18V
- ALL STAGE ARE PRESETTABLE
- RESET DISABLES THE RC OSCILLATOR FOR LOW STANDBY POWER DRAIN
- RC AND CRYSTAL OSCILLATOR OUTPUT ARE CAPABLE OF DRIVING EXTERNAL LOADS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DESCRIPTION

HCF4521B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4521B has a chain of 24 flip-flops with an input circuit that allows three modes of operation.

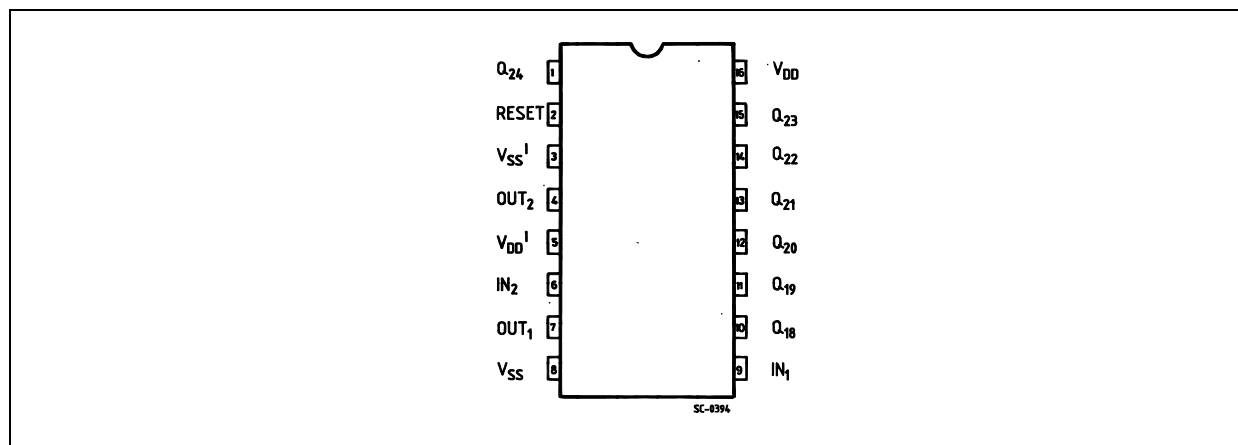


ORDER CODES

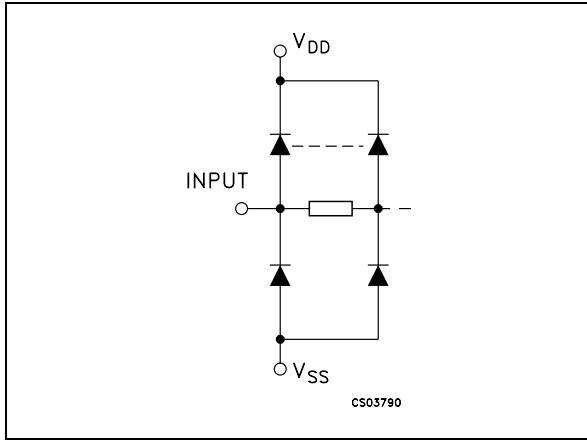
PACKAGE	TUBE	T & R
DIP	HCF4521BEY	
SOP	HCF4521BM1	HCF4521M013TR

The input circuit functions as a crystal or RC oscillator or as an input buffer for an external oscillator. Each flip-flop performs a divide-by-two function giving a total count of $2^{24} = 16,777,216$. The count advances on the negative going edge of the clock. Access is available to the final seven stages giving the device added flexibility.

PIN CONNECTION



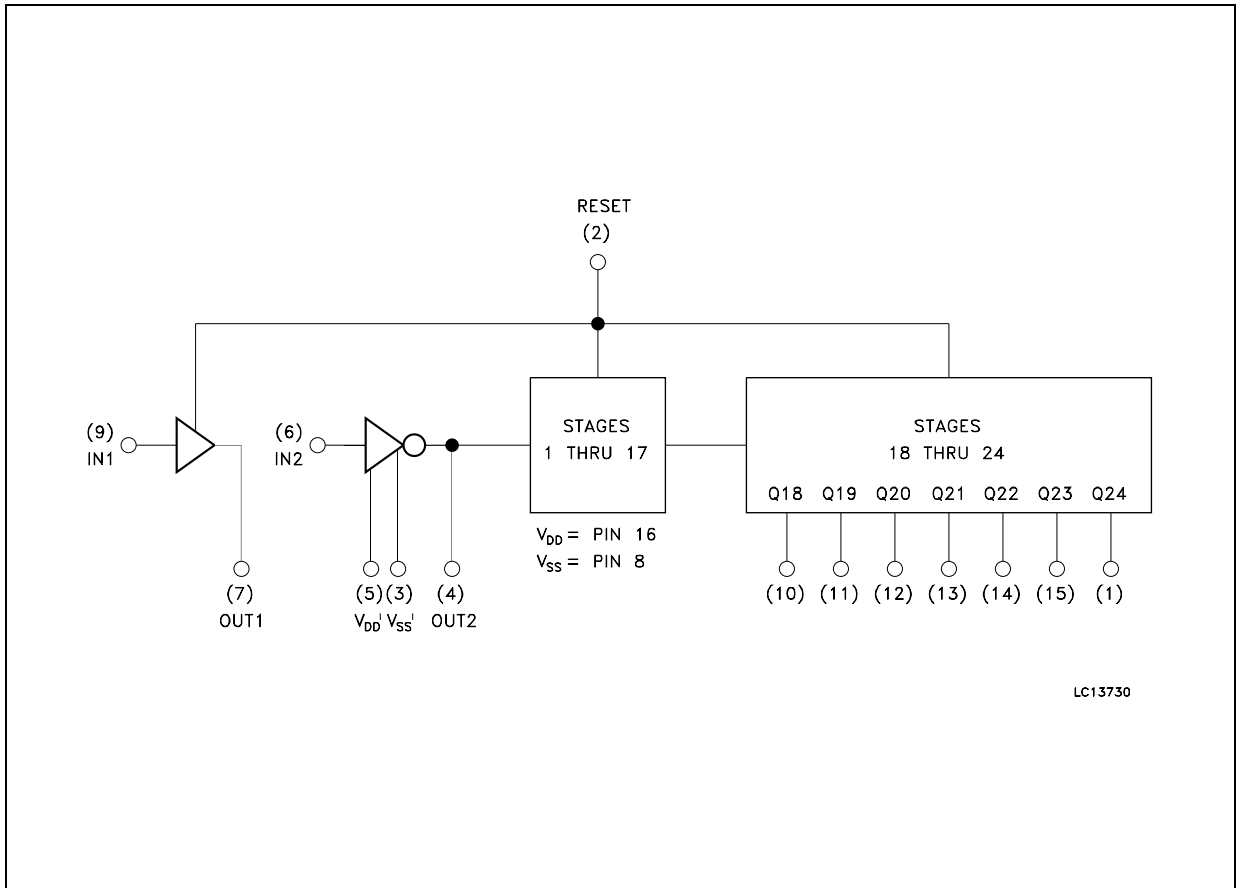
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
10, 11, 12, 13, 14, 15, 1	Q18 to Q24	Outputs Counter
2	RESET	Reset Input
4	OUT2	Output Crystal Oscillator
7	OUT1	Output RC Oscillator
9	IN1	Clock Input
6	IN2	Clock Input
3	V_{SS}^1	Ext. Neg. Supply Voltage
5	V_{DD}^1	Ext. Pos. Supply Voltage
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

BLOCK DIAGRAM

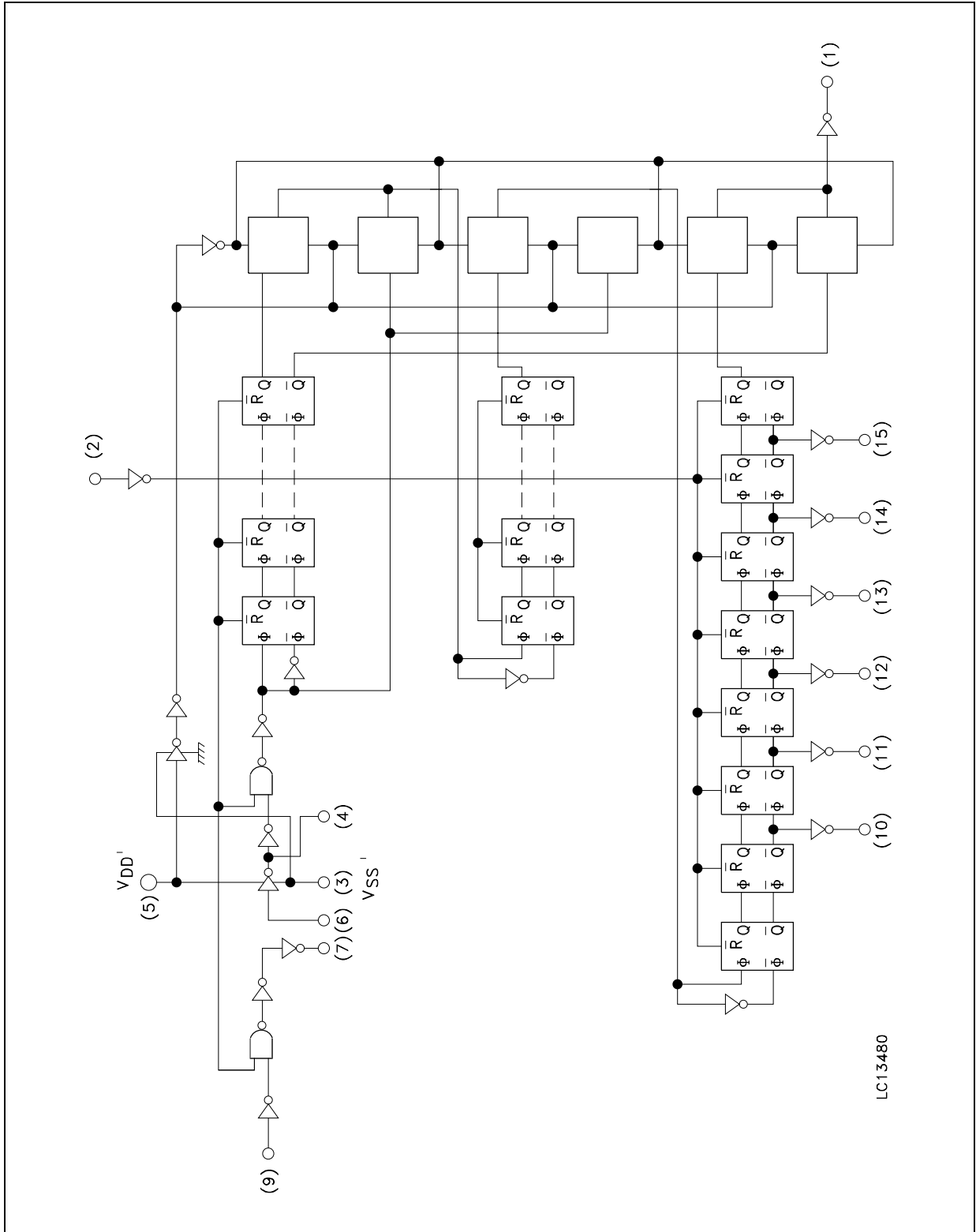


FUNCTIONAL TEST SEQUENCE

INPUTS		OUTPUTS				COMMENTS
RESET	IN 2	OUT	V _{SS} ¹	V _{DD} ¹	Q18 - Q24	
H	L	L	V _{DD}	V _{SS}	L	Counter is in three 8-stage sections in parallel mode Counter in reset. IN 2 and OUT 2 are tied together
L	H	H	V _{DD}	V _{SS}	L	First LOW-to-HIGH transition at IN 2
L	L	L	V _{DD}	V _{SS}	L	255 LOW-to-HIGH transition are clocked in at IN 2
L	H	H	V _{DD}	V _{SS}	L	
L	H	H	V _{DD}	V _{SS}	H	The 255th LOW-to-HIGH transition
L	L	L	V _{DD}	V _{SS}	H	
L	L	L	V _{SS}	V _{SS}	H	
L	H	L	V _{SS}	V _{DD}	H	Counter Converted Back to 24-Stage in Series Mode
L	H	L	V _{SS}	V _{DD}	H	OUT 2 reverts to output operation
L	L	H	V _{SS}	V _{DD}	L	Counter ripples from an all-HIGH state to an all-LOW state

A test function (see Functional Test Circuit) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flop are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In2) which will cause the counter to ripple from an all "1" state to an all "0" state.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V _I (V)	V _O (V)	I _{OL} (μ A)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I _L	Quiescent Current	0/5			5		0.04	5		150		150	μ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I _I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	± 0.1		± 1		± 1	μ A
C _I	Input Capacitance		Any Input				5	7.5					pF

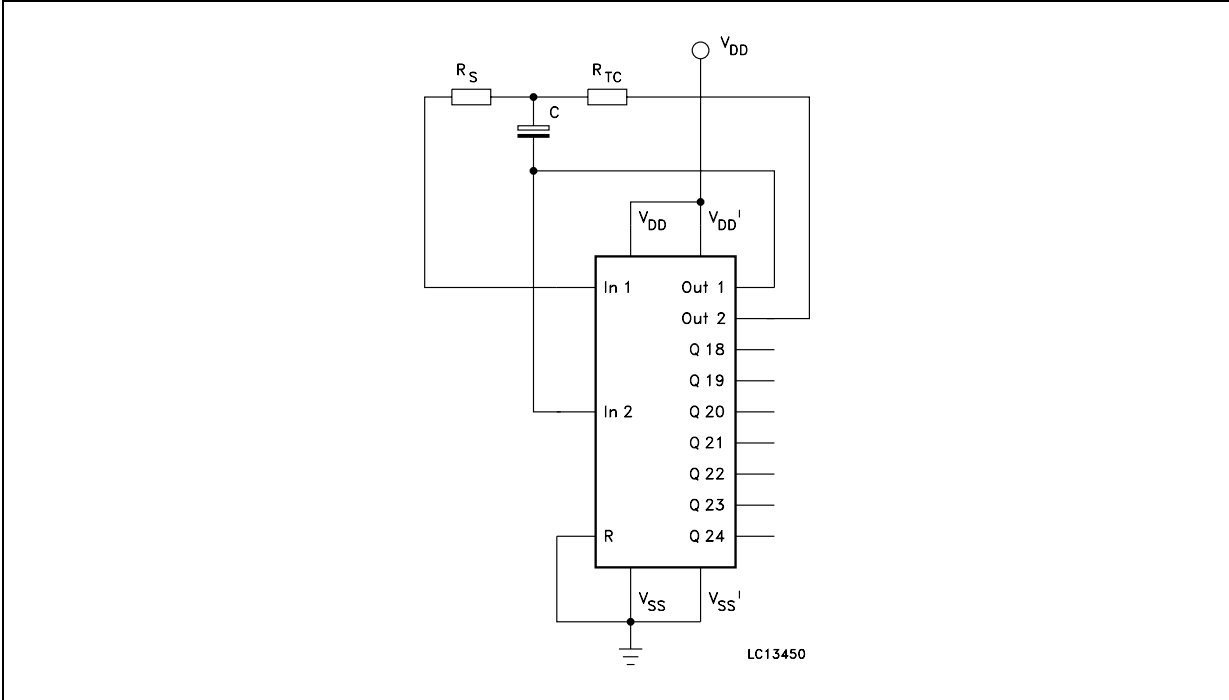
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{K}\Omega$, $t_r = t_f = 20\text{ ns}$)

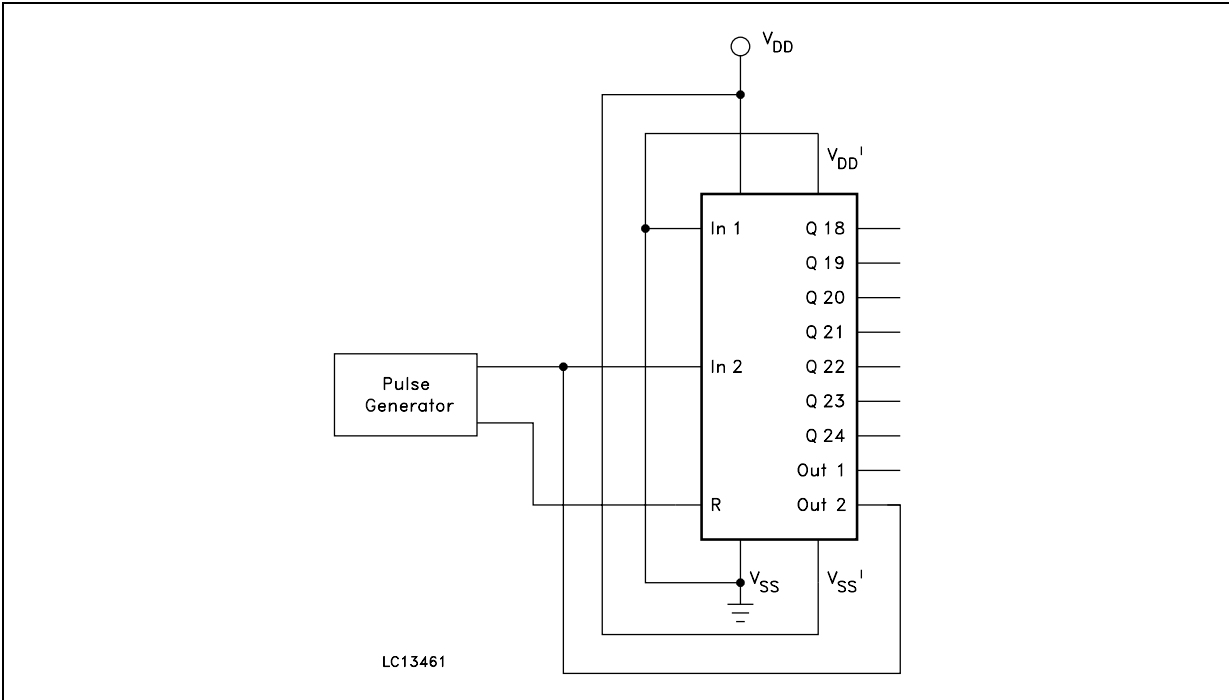
Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH}	Output Rise Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{PHL}	Output Fall Time	5			100	200	ns
		10			50	100	
		15			40	80	
t_{PHL} , t_{PLH}	Propagation Delay Time Clock to Q18	5			4.5	9.0	μs
		10			1.7	3.5	
		15			1.3	2.7	
t_{PHL} , t_{PLH}	Propagation Delay Time Clock to Q24	5			6.0	12	μs
		10			2.2	4.5	
		15			1.7	3.5	
t_{PHL}	Propagation Delay Time RESET to Qn	5			1300	2600	ns
		10			500	1000	
		15			375	750	
$t_{WH(d)}$	Clock Pulse Width	5		385	140		ns
		10		150	55		
		15		120	40		
f_{cl}	Clock Pulse Frequency	5			3.5	2	MHz
		10			9	5	
		15			12	6.5	
t_{THL} , t_{TLH}	Clock Rise and Fall Time	5				15	μs
		10				15	
		15				15	
$t_{W(R)}$	Reset Pulse Width	5		1400	700		ns
		10		600	300		
		15		450	225		

(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

RC OSCILLATOR CIRCUIT



FUNCTIONAL TEST CIRCUIT

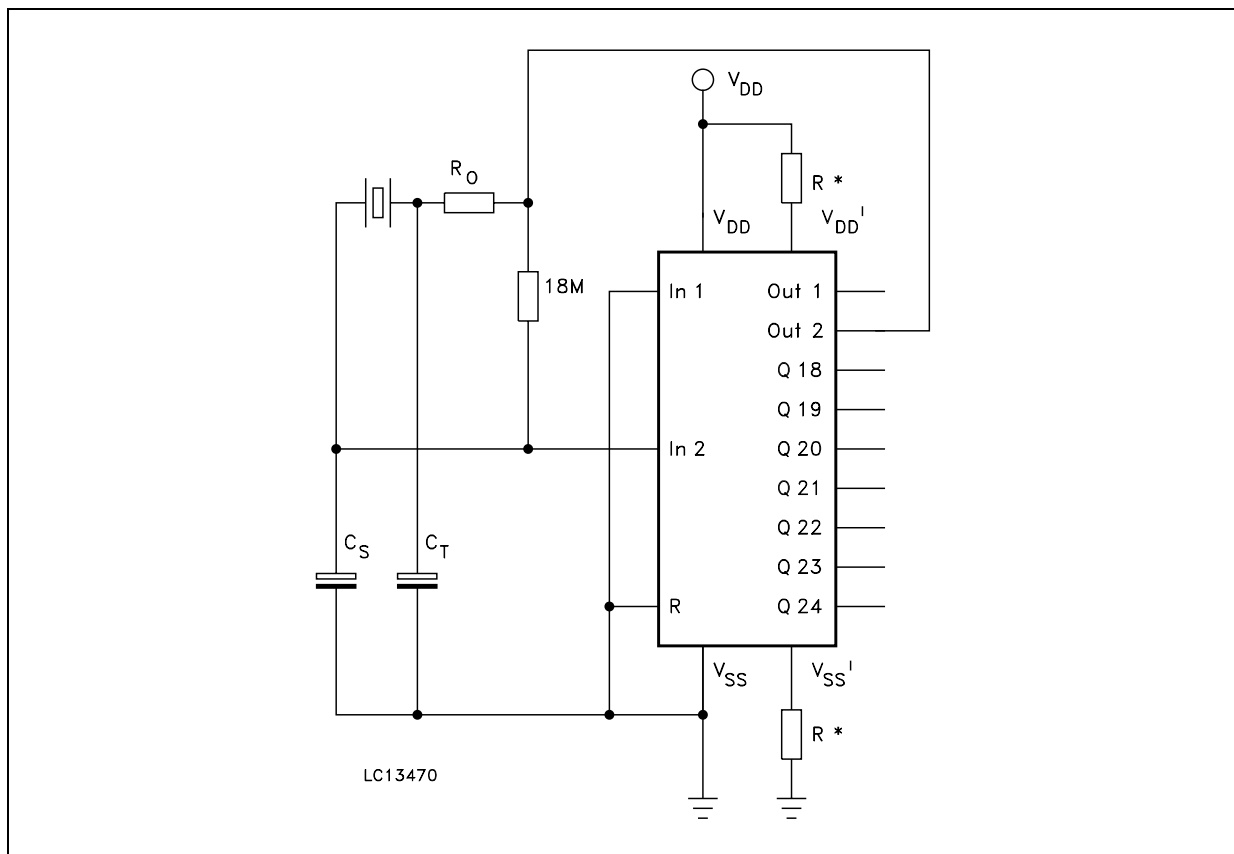


TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC		500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics	Resonant Frequency	500	50	kHz
	Equivalent Resistance, R_s	1	6.2	$k\Omega$
External Resistor/Capacitor Values	R_O	47	750	$k\Omega$
	C_T	82	82	pF
	C_S	20	20	pF
Frequency Stability Frequency Change as a Function of V_{DD} ($T_A = 25^\circ C$)	V_{DD} Change from 5V to 10V	6	2	ppm
	V_{DD} Change from 10V to 15V	2	2	ppm
Frequency Change as a Function of temperature $V_{DD} = 10V$ T_A Change from $-55^\circ C$ to $25^\circ C$	HCF4521B only	-4	-2	ppm
	Complete Oscillator *	100	120	ppm
T_A Change from $25^\circ C$ to $125^\circ C$	HCF4521B only	-2	-2	ppm
	Complete Oscillator *	160	-560	ppm

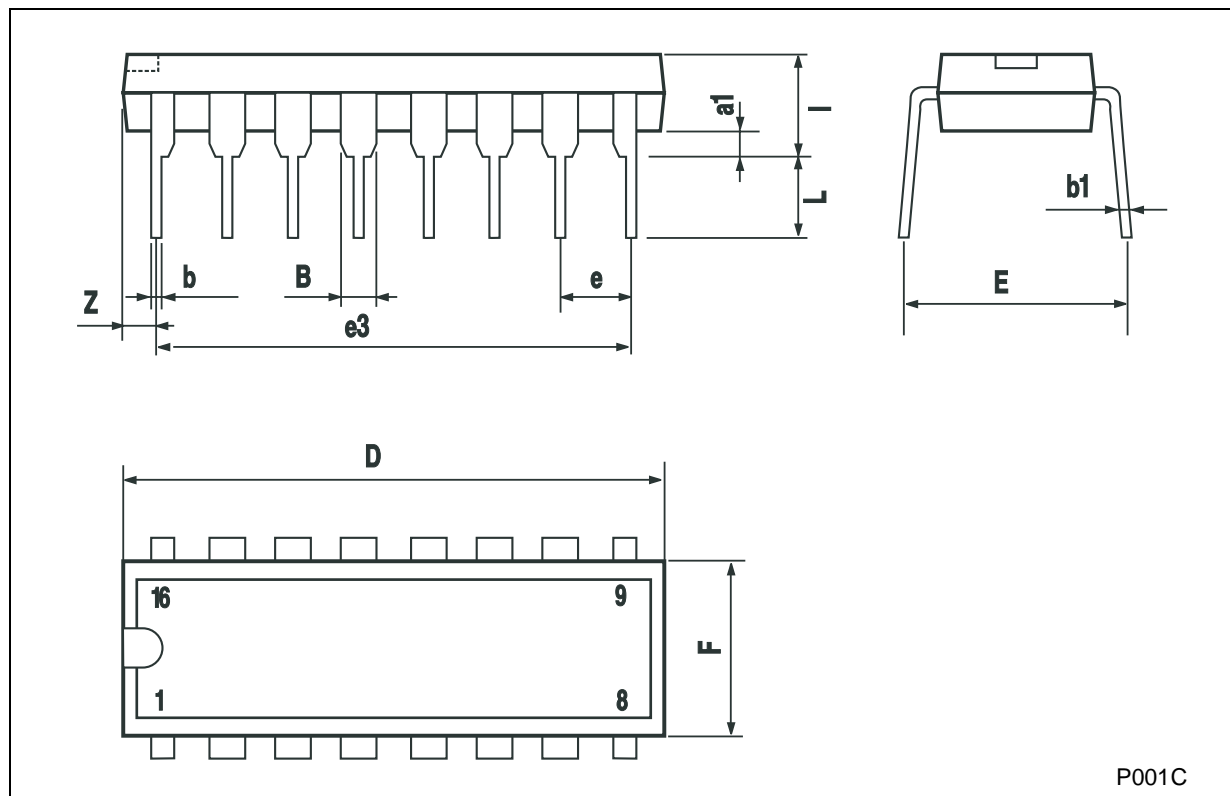
* Complete oscillator includes crystal, capacitors and resistors.

CRYSTAL OSCILLATOR CIRCUIT



Plastic DIP-16 (0.25) MECHANICAL DATA

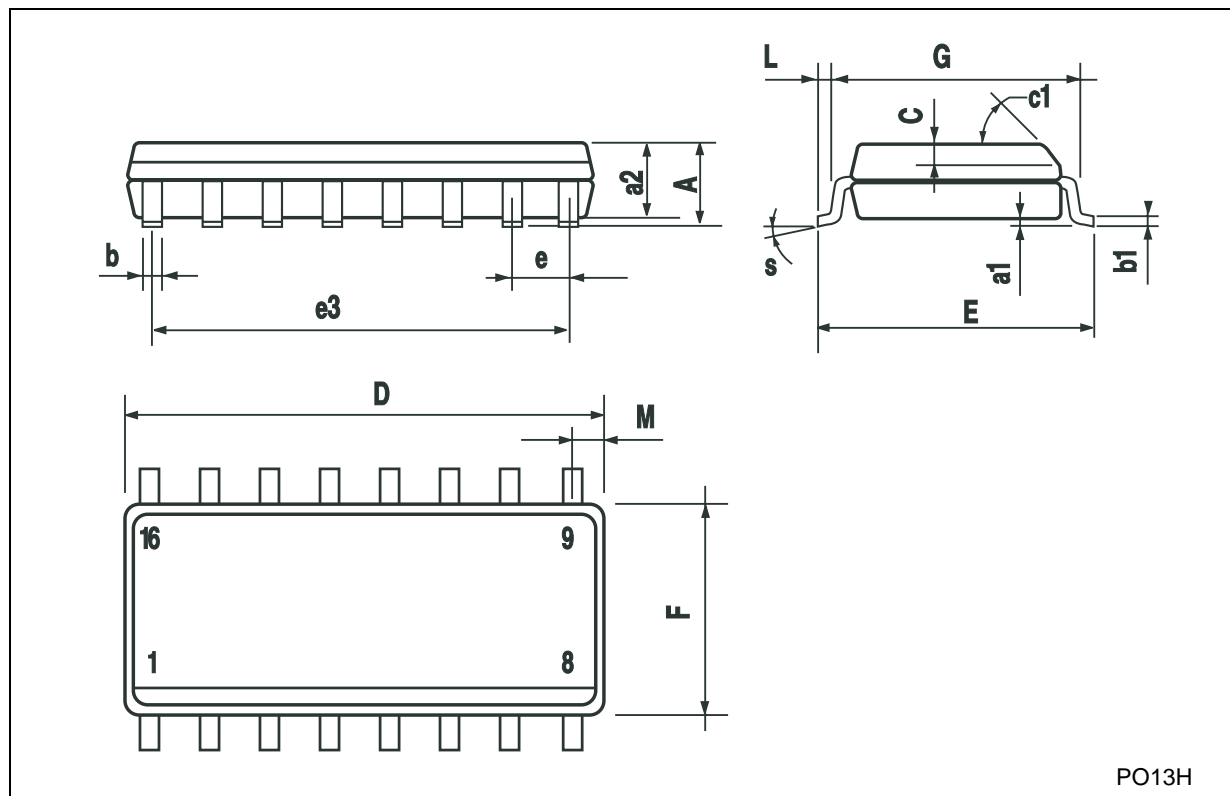
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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